ISL54060, ISL54061

Negative Signal Swing, Sub-ohm, Dual SPST Single Supply Switch

FN6580
Rev.2.01
Feb 20, 2020

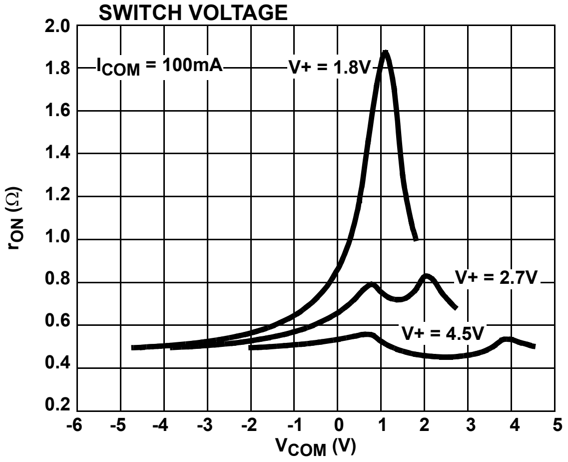
The ISL54060 and ISL54061 devices are a low ON-resistance, low voltage, bi-directional, dual single-pole/single-throw (SPST) analog switch. It is designed to operate from a single +1.8V to +6.5V supply and pass signals that swing down to 6.5V below the positive supply rail. Targeted applications include battery powered equipment that benefit from low r_{ON} (0.56Ω), low power consumption (8nA) and fast switching speeds (t_{ON} = 55ns, t_{OFF} = 18ns). The digital inputs are 1.8V logic-compatible up to a +3V supply. The ISL54060, ISL54061 are offered in a small form factor package, alleviating board space limitations. It is available in a tiny 10 Ld 1.8 x 1.4mm µTQFN or 10 Ld 3x3mm TDFN package.

The ISL54060 is a committed dual single-pole/single-throw (SPST) that consist of two normally open (NO) switches with independent logic control. The ISL54061 is a committed dual single-pole/single-throw (SPST) that consist of two normally closed (NC) switches with independent logic control.

TABLE 1. FEATURES AT A GLANCE

	ISL54060	ISL54061
Number of Switches	2	2
SW	SPST NO	SPST NC
4.3V r_{ON}	0.65Ω	0.65Ω
4.3V t_{ON}/t_{OFF}	43ns/23ns	43ns/23ns
2.7V r_{ON}	0.9Ω	0.9Ω
2.7V t_{ON}/t_{OFF}	55ns/18ns	55ns/18ns
1.8V r_{ON}	1.8Ω	1.8Ω
1.8V t_{ON}/t_{OFF}	145ns/28ns	145ns/28ns
Packages	10 Ld µTQFN, 10 Ld TDFN	

ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE



Features

- Pb-Free (RoHS Compliant)
- Negative Signal Swing (Max 6.5V Below V+)
- ON-Resistance (r_{ON})
  - V+ = +4.5V 0.52Ω
  - V+ = +4.3V 0.65Ω
  - V+ = +2.7V 0.9Ω
  - V+ = +1.8V 1.8Ω
- r_{ON} Matching Between Channels 10mΩ
- r_{ON} Flatness Across Signal Range 0.33Ω
- Low THD+N at 32Ω Load 0.02%
- Single Supply Operation . . . . +1.8V to +6.5V
- Low Power Consumption at 3V (P_D) 24nW
- Fast Switching Action (V+ = +4.3V)
  - t_{ON} 43ns
  - t_{OFF} 23ns
- ESD HBM Rating . . . . >6kV
- Guaranteed Break-before-Make
- 1.8V Logic Compatible (+3V supply)
- Low I+ Current when V_{INH} is not at the V+ Rail
- Available in 10 Ld µTQFN 1.8x1.4mm and 10 Ld 3x3mm TDFN

Applications

- Audio and Video Switching
- Battery powered, Handheld, and Portable Equipment
  - MP3 and Multimedia Players
  - Cellular/mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment

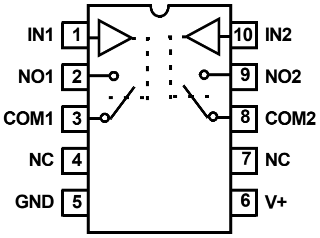
Related Literature

For a full list of related documents, visit our website:

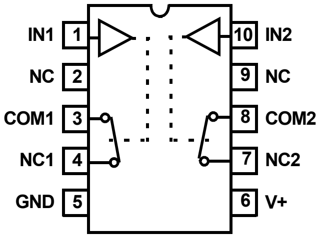
- ISL54060, ISL54061 device pages

Pinouts (Note 1)

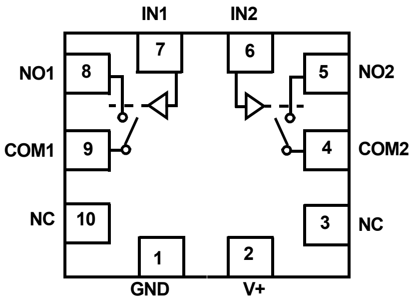
ISL54060
(10 LD TDFN)
TOP VIEW



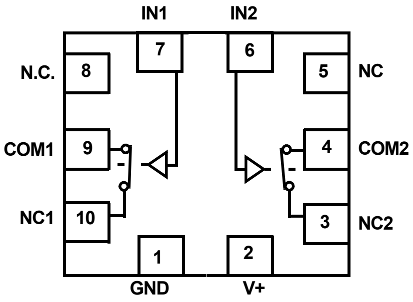
ISL54061
(10 LD TDFN)
TOP VIEW



ISL54060
(10 LD µTQFN)
TOP VIEW



ISL54061
(10 LD µTQFN)
TOP VIEW



NOTE:

1. Switches Shown for INx = Logic "0".

Truth Table

INx	ISL54060 NOx to COMx	ISL54061 NCx to COMx
0	OFF	ON
1	ON	OFF

NOTE: Logic "0" ≤0.5V. Logic "1" ≥1.4V with a 3V supply.

Pin Descriptions

PIN	FUNCTION
V+	IC Power Supply (+1.8V to +6.5V). Decouple V+ to ground by placing a 0.1µF capacitor at the V+ and GND supply lines as near as the IC as possible.
GND	Ground Connection
INx	Digital Control Input
COM	Analog Switch Common Pin
NOx	Analog Switch Normally Open Pin
NCx	Analog Switch Normally Closed Pin
NC	No Connect

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 2)	PACKAGE (RoHS Complaint)	PKG. DWG. #
ISL54060IRTZ (Note 3) **(Not recommended for new design, recommended replacement: ISL54065IRUZ-T)**	4060	-40 to +85	-	10 Ld 3x3 TDFN	L10.3x3A
ISL54060IRTZ-T (Note 3) **(Not recommended for new design, recommended replacement: ISL54065IRUZ-T)**	4060	-40 to +85	6k	10 Ld 3x3 TDFN	L10.3x3A
ISL54060IRUZ-T (Note 4) **(Not recommended for new design, recommended replacement: ISL54065IRUZ-T)**	Y	-40 to +85	3k	10 Ld Thin µTQFN	L10.1.8x1.4A
ISL54061IRTZ (Note 3)	4061	-40 to +85	-	10 Ld 3x3 TDFN	L10.3x3A
ISL54061IRTZ-T (Note 3)	4061	-40 to +85	6k	10 Ld 3x3 TDFN	L10.3x3A
ISL54061IRUZ-T (Note 4)	W	-40 to +85	3k	10 Ld Thin µTQFN	L10.1.8x1.4A

NOTES:

2. Please see TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

Absolute Maximum Ratings

V+ to GND	-0.5 to 7.0V
Input Voltages	
NOx, NCx (Note 5)	(V+ - 7V) to ((V+) + 0.5V)
INx (Note 5)	-0.5 to ((V+) + 0.5V)
Output Voltages	
COMx (Note 5)	(V+ - 7V) to ((V+) + 0.5V)
Continuous Current NOx, NCx, or COMx	±300mA
Peak Current NOx, NCx, or COMx (Pulsed 1ms, 10% Duty Cycle, Max)	±500mA
ESD Rating:	
Human Body Model	>6kV
Machine Model	>400V
Charged Device Model	>1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 TDFN Package (Notes 6 and 8)	52	18
10 Ld µTQFN Package (Note 7)	154	N/A

Maximum Junction Temperature (Plastic Package)	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile	see TB493

Operating Conditions

Temperature Range	-40°C to +85°C
Power Supply Range	+1.8V to +6.5V

AUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Signals on NC, NO, IN, or COM exceeding V+ or GND by the specified amount are clamped by internal diodes. Limit forward diode current to maximum current ratings.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.
8. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 9), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 10, 11)	TYP	MAX (Notes 10, 11)	UNIT
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5) to V+, (See Figure 4)	25	-	0.52	-	Ω
		Full	-	0.68	-	Ω
r_{ON} Matching Between Channels, ΔR_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON}, (Note 13)	25	-	10	-	mΩ
		Full	-	13.1	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5) to V+, (Note 12)	25	-	0.11	-	Ω
		Full	-	0.14	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5V, V_{COM} = -1.5V, 5V, V_{NO} or V_{NC} = 5V, -1.5V	25	-	-8.13	-	nA
		Full	-	-0.4	-	µA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5V, V_{COM} = -1.5V, 5V, V_{NO} or V_{NC} = Float	25	-	-4.42	-	nA
		Full	-	-0.33	-	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	35	-	ns
		Full	-	30	-	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	10	-	ns
		Full	-	15	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (see Figure 2)	25	-	170	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (see Figure 3)	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{RMS}$ (see Figure 5)	25	-	-75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 32Ω	25	-	0.02	-	%
-3dB Bandwidth	V_{COM} = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF	25	-	60	-	MHz
NO x or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 6)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (See Figure 6)	25	-	88	-	pF

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 9), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 10, 11)	TYP	MAX (Notes 10, 11)	UNIT
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+	25	-	0.008	0.1	µA
		Full	-	1.41	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	25	-0.1	-	0.1	µA
		Full	-	0.3	-	µA

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Note 9), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 10, 11)	TYP	MAX (Notes 10, 11)	UNIT
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 4.3V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+ (see Figure 4)	25	-	0.65	-	Ω
		Full	-	0.72	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.3V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON}, (Note 13)	25	-	10	-	mΩ
		Full	-	15	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.3V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+, (Note 12)	25	-	0.1	-	Ω
		Full	-	0.14	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 4.3V, V_{COM} = -1.2V, 4.3V, V_{NO} or V_{NC} = 4.3V, -1.2V	25	-0.1	-	0.1	µA
		Full	-1	-0.33	1	µA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.3V, V_{COM} = -1.2V, 4.3V, V_{NO} or V_{NC} = Float	25	-0.1	-	0.1	µA
		Full	-1	-0.33	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	43	-	ns
		Full	-	50	-	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	23.1	-	ns
		Full	-	23.2	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	200	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (see Figure 3)	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{RMS}$ (see Figure 5)	25	-	-75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.04	-	%
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 6)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 6)	25	-	88	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = +4.5V, V_{IN} = 0V or V+	25	-	0.003	0.1	µA
		Full	-	0.9	-	µA
Positive Supply Current, I+	V+ = +4.2V, V_{IN} = 2.85V	25	-	0.78	12	µA

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Note 9), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 10, 11)	TYP	MAX (Notes 10, 11)	UNIT
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.6	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+	25	-0.5	-	0.5	µA
		Full	-	0.2	-	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 9), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 10, 11)	TYP	MAX (Notes 10, 11)	UNIT
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+ (see Figure 4)	25	-	0.9	-	Ω
		Full	-	0.96	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON}, (Note 13)	25	-	10	-	mΩ
		Full	-	17	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ - 6.5V) to V+, (Notes 12, 14)	25	-	0.33	0.5	Ω
		Full	-	0.35	0.55	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	50	-	ns
		Full	-	60	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	27	-	ns
		Full	-	35	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	94	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (see Figure 3)	25	-	68	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (see Figure 5)	25	-	-95	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 32Ω	25	-	0.04	-	%
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 6)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 6)	25	-	88	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.5	V
Input Voltage High, V_{INH}		25	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.3V, V_{IN} = 0V or V+	25	-0.5	-	0.5	µA
		Full	-	0.2	-	µA

Electrical Specifications - 1.8V Supply

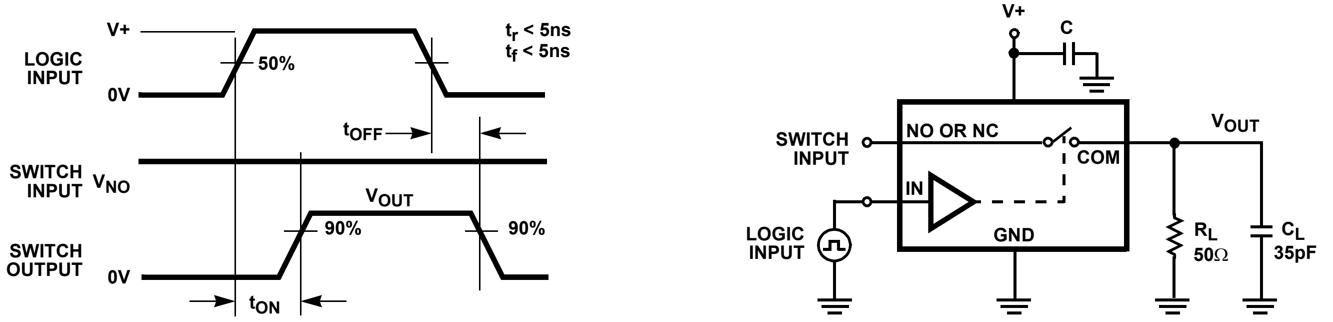
Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.4V (Note 9), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 10, 11)	TYP	MAX (Notes 10, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+ (see Figure 4)	25	-	1.87	-	Ω
		Full	-	1.97	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON}, (Note 13)	25	-	16	-	mΩ
		Full	-	30	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+, (Note 12)	25	-	1.34	-	Ω
		Full	-	1.43	-	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.8V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	145	-	ns
		Full	-	150	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} or V_{NC} = 1.8V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	20	-	ns
		Full	-	22	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	40	-	pC
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 6)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 6)	25	-	88	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.4	V
Input Voltage High, V_{INH}		25	1.0	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+	25	-0.5	-	0.5	µA
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+	Full	-	0.19	-	µA

NOTES:

9. V_{IN} = input voltage to perform proper function.
10. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
12. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
13. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between NC1 and NC2 or between NO1 and NO2.
14. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

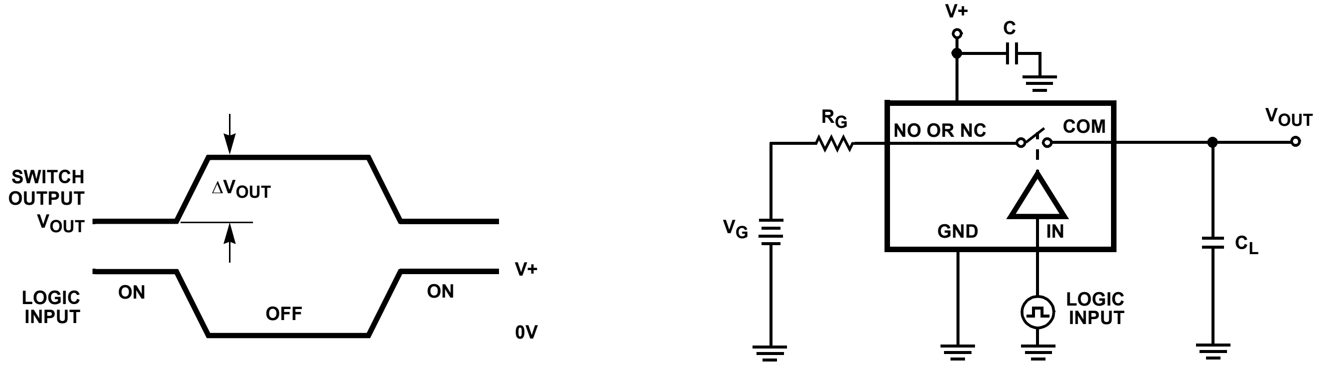
Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1A. MEASUREMENT POINTS

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



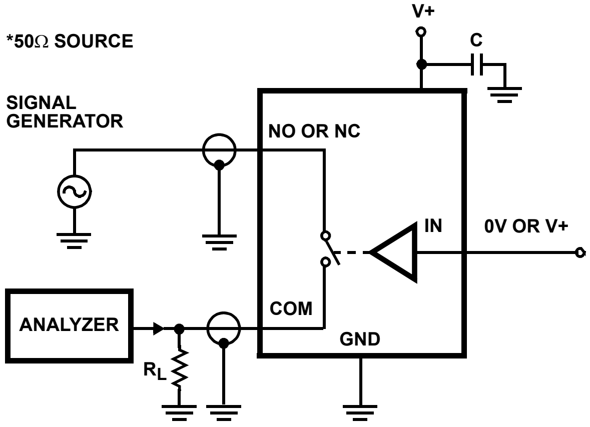
$Q = \Delta V_{OUT} \times C_L$

Repeat test for all switches.

FIGURE 2A. MEASUREMENT POINTS

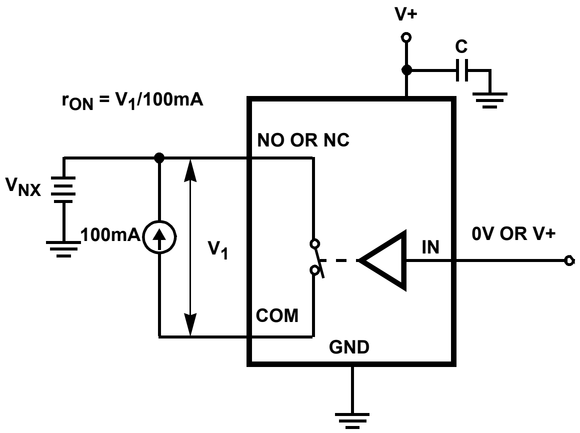
FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

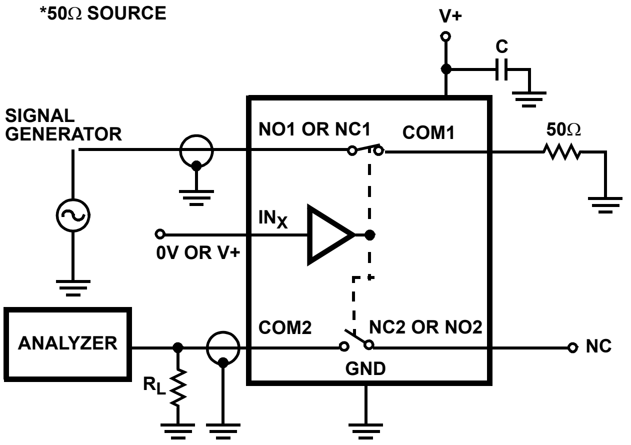
FIGURE 3. OFF-ISOLATION TEST CIRCUIT



Repeat test for all switches.

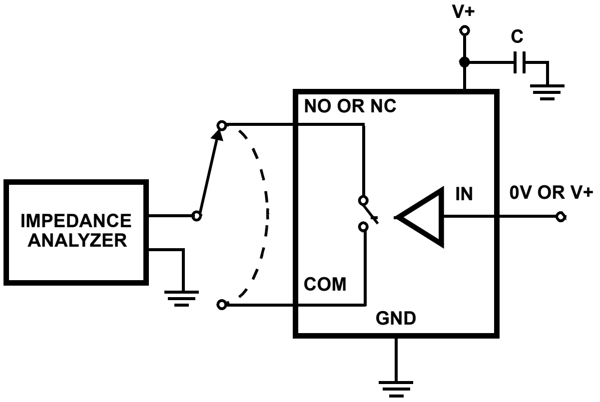
FIGURE 4. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 5. CROSSTALK TEST CIRCUIT



COM is connected to NO or NC during ON capacitance measurement.

FIGURE 6. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL54060 and ISL54061 are bidirectional, dual single pole-single throw (SPST) analog switches that offers precise switching from a single 1.8V to 6.5V supply with low ON-resistance (0.83Ω) and high speed operation (t_{ON} = 55ns, t_{OFF} = 18ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.8V), low power consumption (8nA), and a tiny 1.8x1.4mm µTQFN package or a 3x3mm TDFN package. The low ON-resistance and r_{ON} flatness provide very low insertion loss and signal distortion for applications that require signal switching with minimal interference by the switch.

The ISL54060 is a normally open (NO) SPST analog switch. The ISL54061 is a normally closed (NC) SPST analog switch.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. The ISL54060 and ISL54061 contains ESD protection diodes on each pin of the IC (see Figure 7). These diodes connect to either a +Ring or -Ring for ESD protection. To prevent forward biasing the ESD diodes to the +Ring, V+ must be applied before any input signals, and the input signal voltages must remain between recommended operating range.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a logic pin or switch terminal goes above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting external Schottky diodes to the signal pins will shunt the fault current to the V+ supply instead of through the internal ESD diodes thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current..

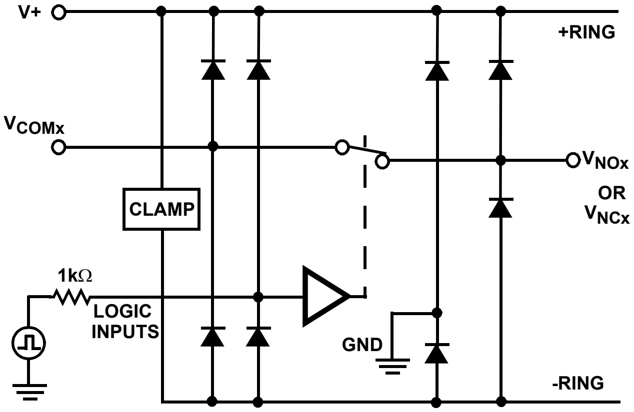


FIGURE 7. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL54060 and ISL54061 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 5.5V maximum supply voltage, the ISL54060 and ISL54061 have a 6.5V maximum supply voltage providing plenty of head room for the 10% tolerance of 5V supplies due to overshoot and noise spikes.

The minimum recommended supply voltage is 1.8V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the “Electrical Specifications” tables, beginning on page 4, and “Typical Performance Curves”, beginning on page 11, for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to V+ and GND signals levels to drive the analog switch gate terminals. A high frequency decoupling capacitor placed as close to the V+ and GND pin as possible is recommended for proper operation of the switch. A value of 0.1µF is highly recommended.

Negative Signal Swing Capability

The ISL54060 and ISL54061 contains circuitry that allows the analog switch signal to swing below ground. The device has an analog signal range of 6.5V below V+ up to the V+ rail (see Figure 13) while maintaining low r_{ON} performance. For example, if V+ = 5V, then the analog input signal range is from -1.5V to +5V. If V+ = 2.7V then the range is from -3.8V to +2.7V.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.45V V_{OLMAX} and 1.35V V_{OHMIN}) over a supply range of 1.8V to 3.3V (see Figure 15). At 3.3V the V_{IL} level is 0.5V maximum. This is still below the 1.8V CMOS guaranteed low output maximum level of 0.45V, but noise margin is reduced. At 3.3V the V_{IH} level is 1.4V minimum. While this is above the 1.8V CMOS guaranteed high output minimum of 1.35V under most operating conditions the switch will recognize this as a valid logic high.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL54060, ISL54061 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic high while operating with a 4.2V supply the device draws only 1µA of current.

High-Frequency Performance

In 50Ω systems, the ISL54060, ISL54061 has an ON switch -3dB bandwidth of 60MHz (see Figure 18). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor across the open terminals and AC couples higher frequencies, resulting in signal feed-through from a switch’s input to its output. Off-Isolation is the resistance to this feed-through. Crosstalk indicates the amount of feed-through from one switch channel to another switch channel. Figure 19 details the high Off-Isolation and Crosstalk rejection provided by this part. At 100kHz, Off-Isolation is about 60dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. At 1MHz, Crosstalk is about -75dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin, V+ and GND. One of these diodes conducts if any analog signal exceeds the recommended analog signal range.

Virtually all the analog switch leakage current comes from the ESD diodes and reversed biased junctions in the switch cell. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased to either the +Ring or -Ring and the analog input signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the +Ring or -Ring and the reverse biased junctions at the internal switch cell constitutes the analog-signal-path leakage current.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

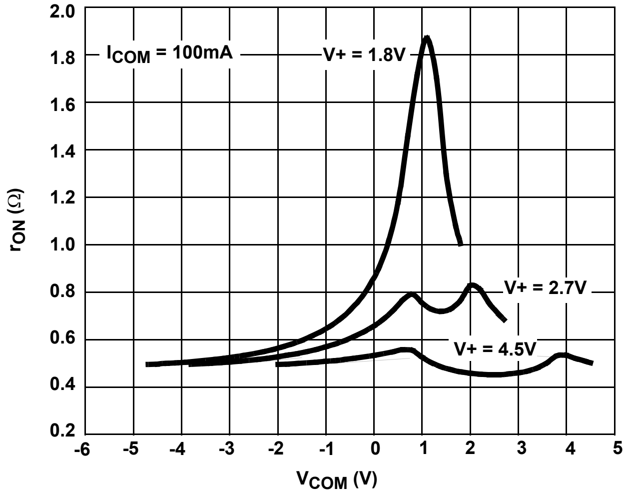


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

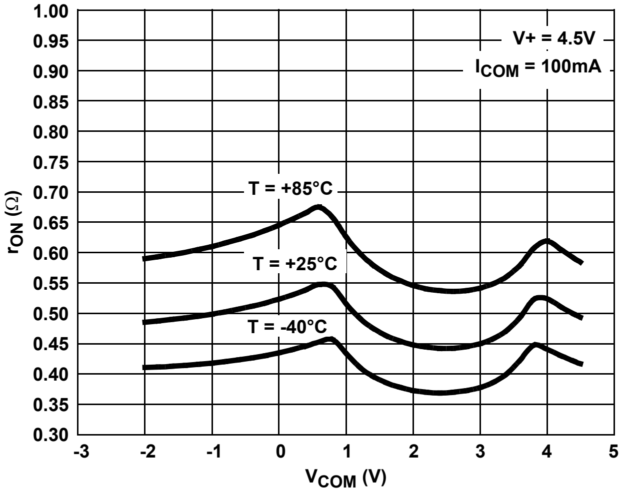


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

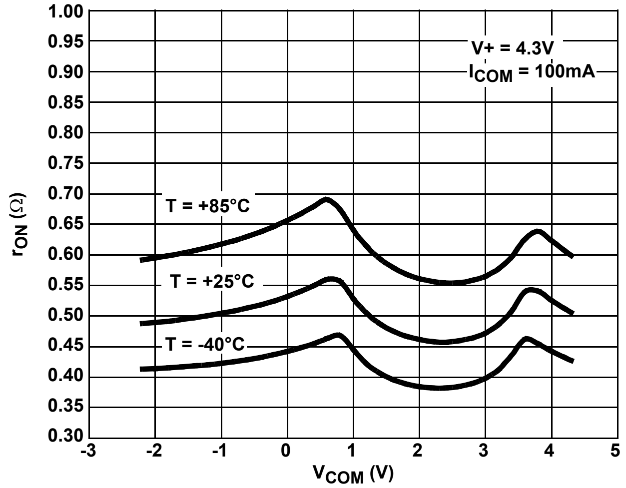


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

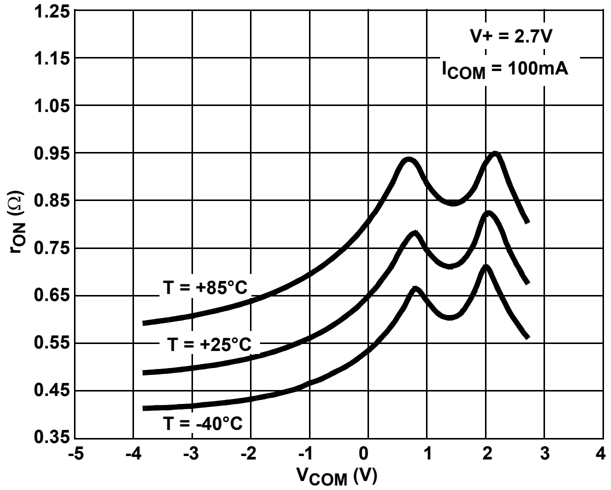


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

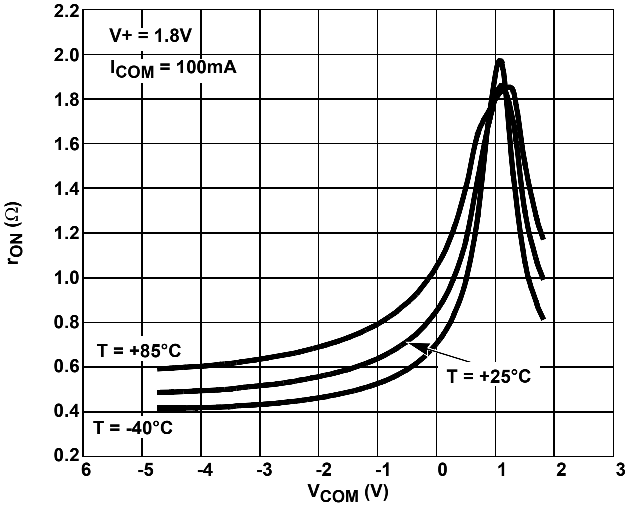


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

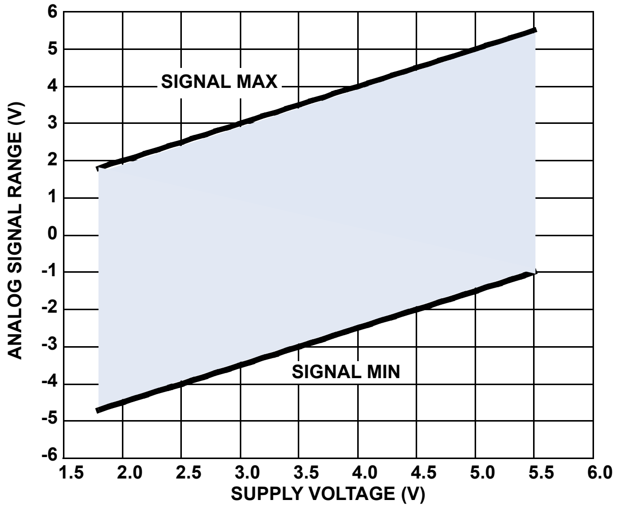


FIGURE 13. ANALOG SIGNAL RANGE vs SUPPLY VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

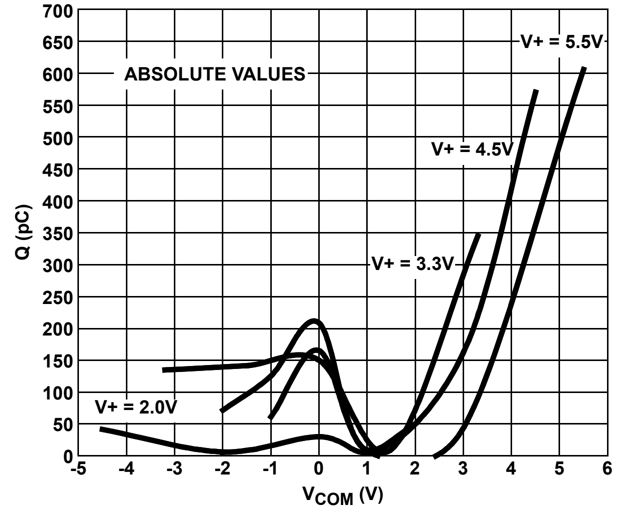


FIGURE 14. CHARGE INJECTION vs SWITCH VOLTAGE

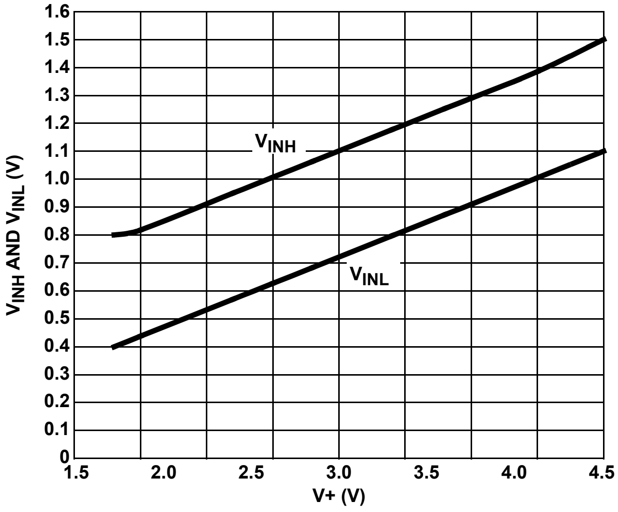


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

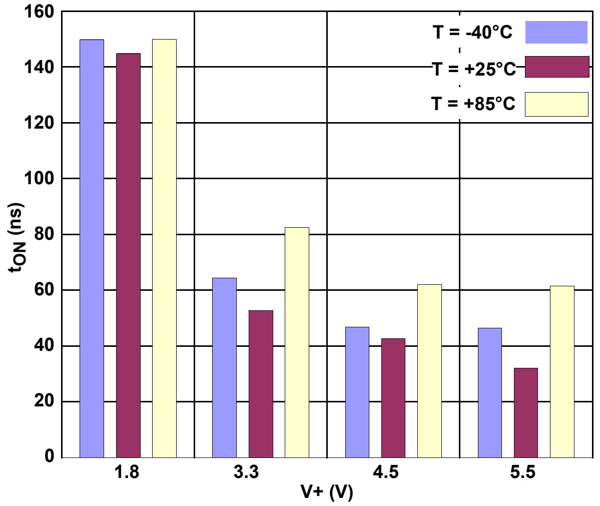


FIGURE 16. TURN - ON TIME vs SUPPLY VOLTAGE

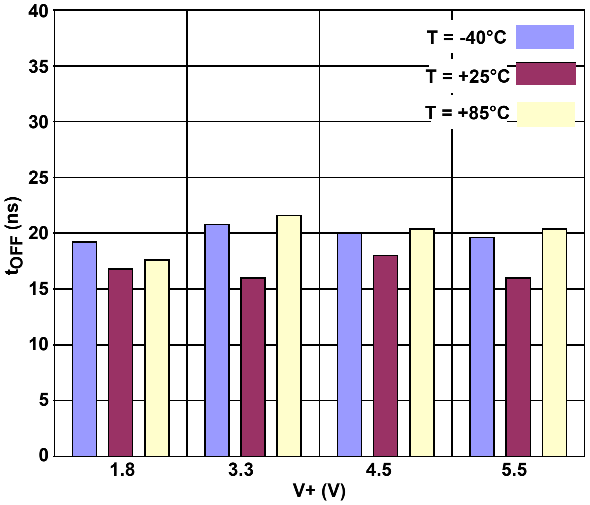


FIGURE 17. TURN - OFF TIME vs SUPPLY VOLTAGE

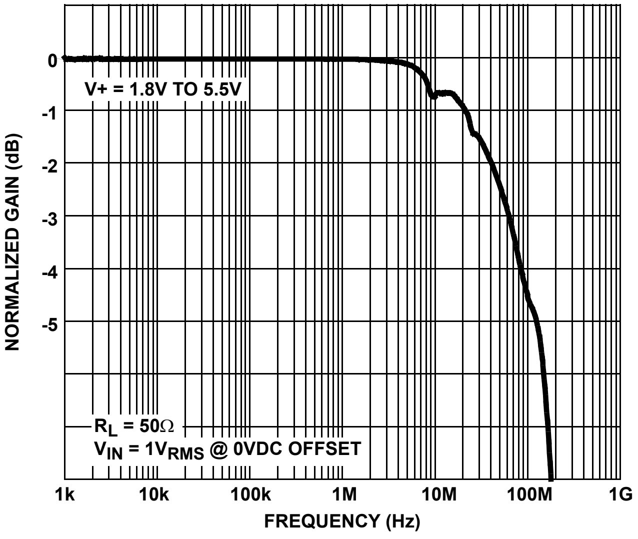


FIGURE 18. FREQUENCY RESPONSE

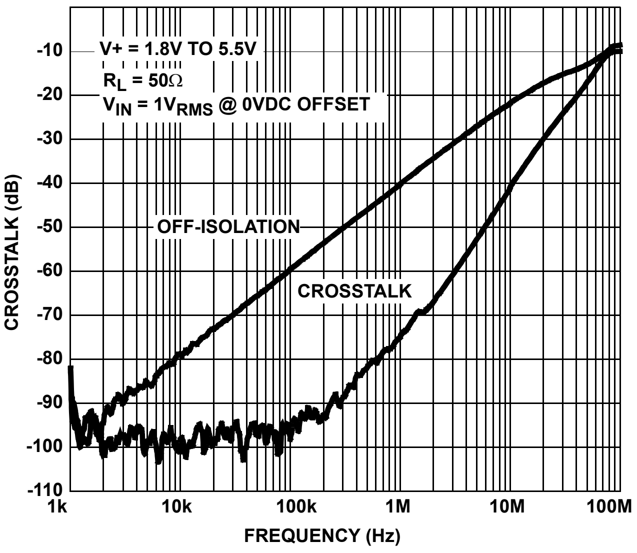


FIGURE 19. CROSSTALK AND OFF-ISOLATION

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified (Continued)

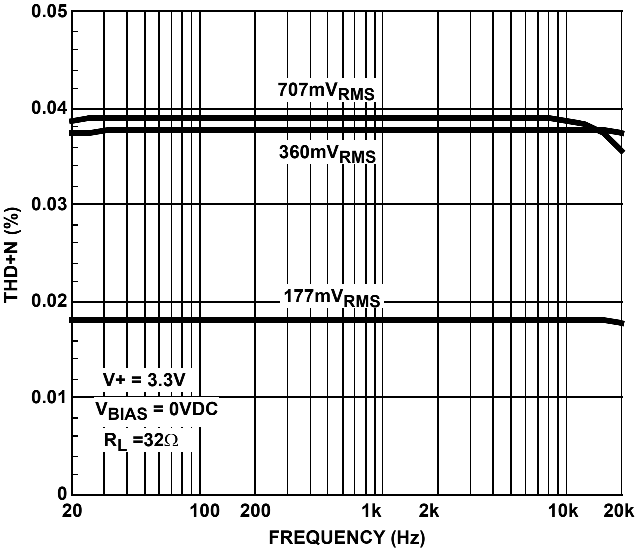


FIGURE 20. TOTAL HARMONIC DISTORTION vs FREQUENCY

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (DFN Paddle Connection: Tie to GND or Float)

TRANSISTOR COUNT:

432

PROCESS:

Submicron CMOS

Revision History

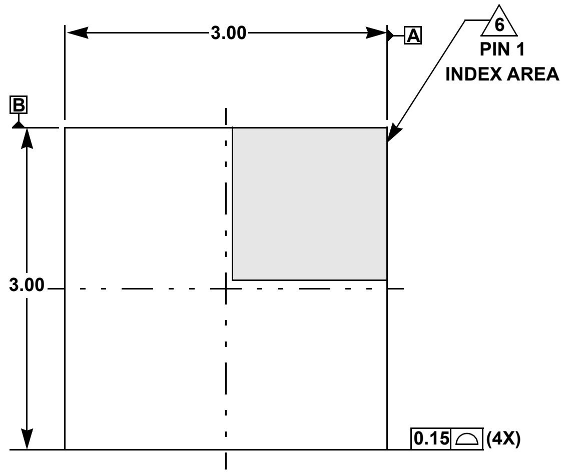
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Feb 20, 2020	2.01	Updated Ordering information table by adding not recommended statement. Added revision history. Updated POD **L10.3x3A to the latest revision changes were as follows:** - Added Typical Recommended Land Pattern -Converted to new format by moving dimensions from table onto drawing (no dimension changes) -Tiebar Note 5 updated -Removed Note 7 -Added detail X indicator. Updated POD L10.1.8x1.4A to the latest revision changes were as follows: -Conversion to New Format -2010-03-30: Pkg thkness in side view changed from "Max 0.50" to "Max 0.55." Lead thkness in detail X changed from "0.2 REF" to "0.127 REF." -2010-03-29: Removed "N" (number of leads) in drawing and replaced with actual number of leads. Deleted previous notes 2, 3,7, 8, 10. Changes Detail X drawing to new standard and removed tie bars in drawing. This is COL package with no tie bars used. Placed reference triangles on notes 4 & 6. Corrected .015 typo to 0.15 in note 4. -2010-03-22: Removed mention of "b" from Note 5 since it does not exist in the drawing. -Bottom view- added chamfer dimension C0.10. -Land pattern – removed the chamfer lead footprint, added footprint tip to tip dimension (2.20 & 1.80). Updated disclaimer.

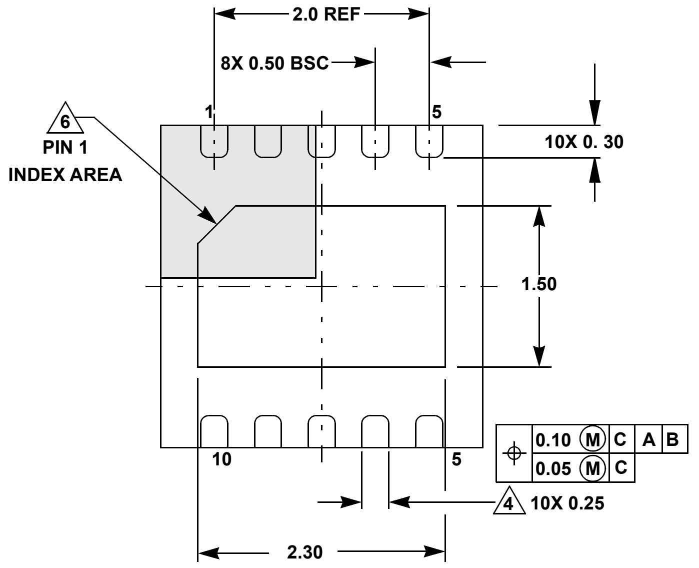
Package Outline Drawings

For the most recent package outline drawing, see L10.3x3A.

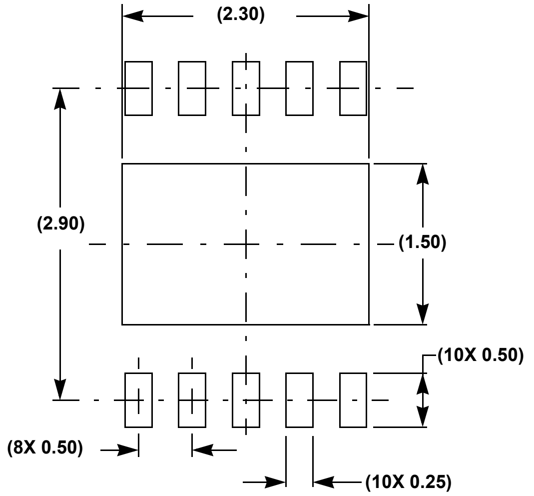
L10.3x3A
10 Lead Thin Dual Flat No-Lead Plastic Package
Rev 7, 1/17



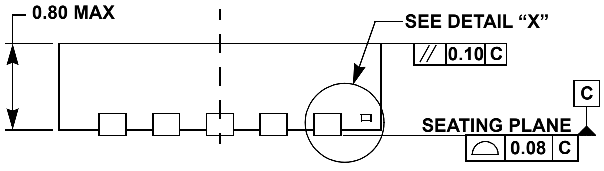
TOP VIEW



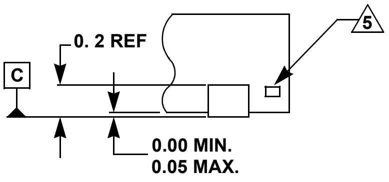
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



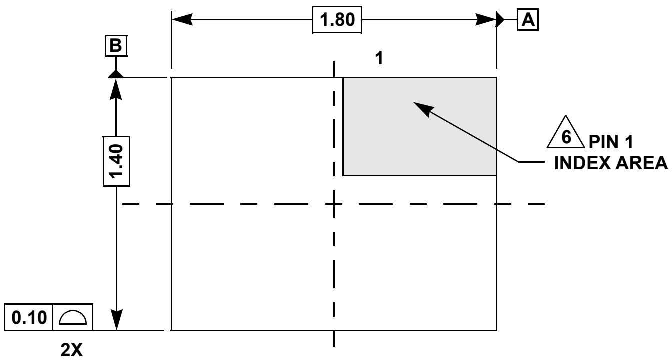
DETAIL "X"

NOTES:

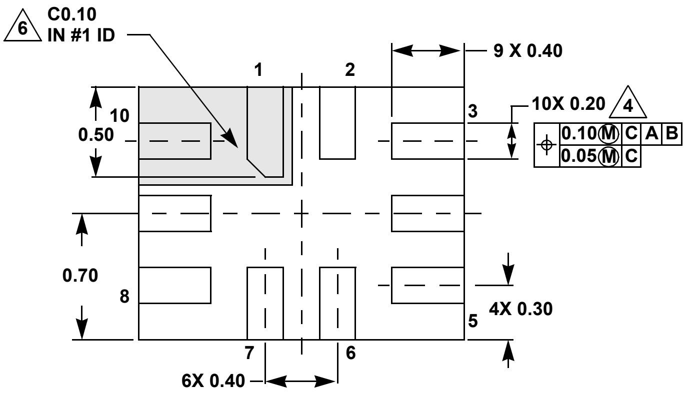
1. **Dimensions are in millimeters.**
   Dimensions in ( ) for Reference Only.
2. **Dimensioning and tolerancing conform to ASME Y14.5m-1994.**
3. **Unless otherwise specified, tolerance: Decimal ±0.05**
   Angular ±2.50°.
4. **Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.**
5. **Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).**
6. **The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.**

L10.1.8x1.4A
10 Lead Ultra Thin Quad Flat No-Lead Plastic Package
Rev 6, 8/13

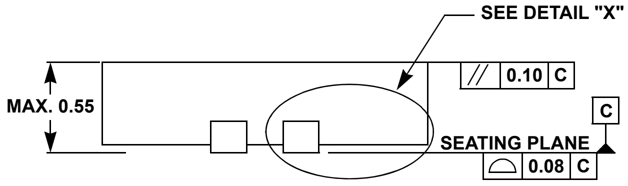
For the most recent package outline drawing, see L10.1.8x1.4A.



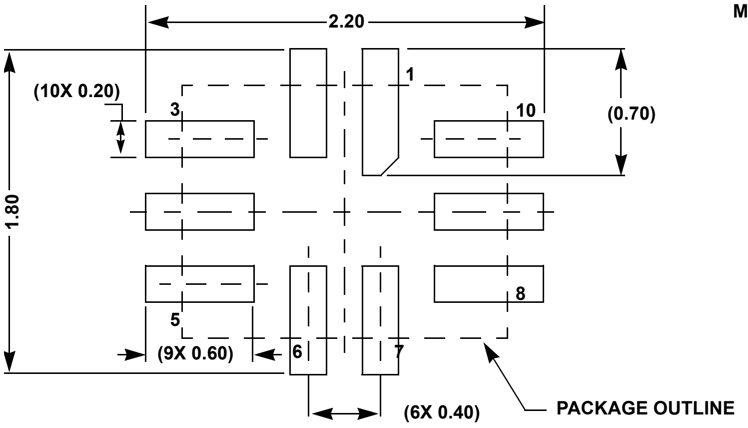
TOP VIEW



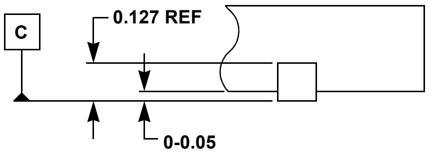
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. JEDEC reference MO-255.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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(Rev.4.0-1 November 2017)

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