

Dual P-Channel NexFET™ Power MOSFET

Check for Samples: [CSD75204W15](#)

FEATURES

- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1.5-mm × 1.5-mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3kV
- Pb Free
- RoHS Compliant
- Halogen Free

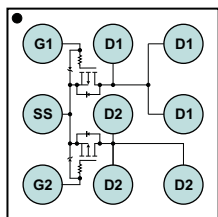
APPLICATIONS

- Battery Management
- Battery Protection

DESCRIPTION

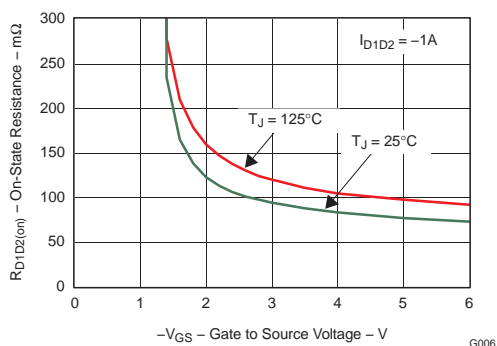
The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View



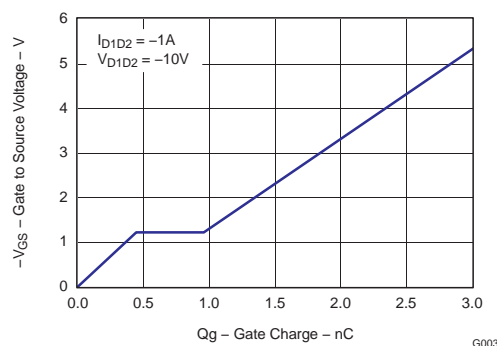
P0109-01

$R_{D1D2(on)}$ vs V_{GS}



G006

Gate Charge (Per MOSFET)



G003



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|----------------------------------|--|------|------|------|------|
| Static Characteristics | | | | | | |
| BV _{D1D2} | Drain to Drain Voltage | V _{GS} = 0V, I _{D1D2} = -250μA | -20 | | | V |
| BV _{GSS} | Gate to Source Voltage | V _{D1D2} = 0V, I _G = -250μA | -6.1 | | -7.2 | V |
| I _{DDS} | Drain to Drain Leakage Current | V _{GS} = 0V, V _{D1D2} = -16V | | | -1 | μA |
| I _{GSS} | Gate to Source Leakage Current | V _{D1D2} = 0V, V _{GS} = -6V | | | -100 | nA |
| V _{GS(th)} | Gate to Source Threshold Voltage | V _{D1D2} = V _{GS} , I _{DS} = -250μA | -0.5 | -0.7 | -0.9 | V |
| R _{D1D2(on)} | Drain to Drain On Resistance | V _{GS} = -1.8V, I _{D1D2} = -1A | 140 | | 175 | mΩ |
| | | V _{GS} = -2.5V, I _{D1D2} = -1A | 105 | | 130 | mΩ |
| | | V _{GS} = -4.5V, I _{D1D2} = -1A | 80 | | 100 | mΩ |
| g _{fs} | Transconductance | V _{D1D2} = -10V, I _{D1D2} = -1A | 5.3 | | | S |
| Dynamic Characteristics | | | | | | |
| C _{ISS} | Input Capacitance | V _{GS} = 0V, V _{D1D2} = -10V, f = 1MHz | 315 | | 410 | pF |
| C _{OSS} | Output Capacitance | | 128 | | 165 | pF |
| C _{RSS} | Reverse Transfer Capacitance | | 43 | | 55 | pF |
| Q _g | Gate Charge Total (-4.5V) | V _{D1D2} = -10V, I _{D1D2} = -1A | 2.8 | | 3.9 | nC |
| Q _{gd} | Gate Charge - Gate to Drain | | 0.6 | | | nC |
| Q _{gs} | Gate Charge - Gate to Source | | 0.5 | | | nC |
| Q _{g(th)} | Gate Charge at V _{th} | | 0.2 | | | nC |
| Q _{OSS} | Output Charge | V _{D1D2} = -9.5V, V _{GS} = 0V | 2.2 | | | nC |
| t _{d(on)} | Turn On Delay Time | V _{D1D2} = -10V, V _{GS} = -4.5V, I _{D1D2} = -1A, R _G = 30Ω | 7.8 | | | ns |
| t _r | Rise Time | | 6.7 | | | ns |
| t _{d(off)} | Turn Off Delay Time | | 45 | | | ns |
| t _f | Fall Time | | 26 | | | ns |
| Diode Characteristics | | | | | | |
| V _{SD} | Diode Forward Voltage | I _{D1D2} = -1A, V _{GS} = 0V | 0.75 | | 1 | V |
| Q _{rr} | Reverse Recovery Charge | V _{dd} = -9.5V, I _F = -1A, di/dt = 200A/μs | 10.5 | | | nC |
| t _{rr} | Reverse Recovery Time | V _{dd} = -9.5V, I _F = -1A, di/dt = 200A/μs | 23 | | | ns |

THERMAL CHARACTERISTICS

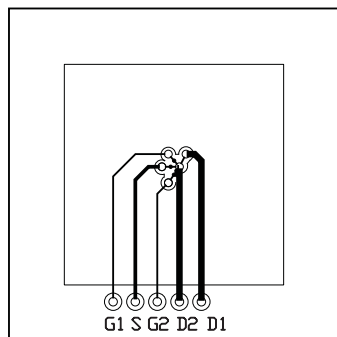
($T_A = 25^\circ\text{C}$ unless otherwise stated)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-----------------|---|-----|-----|-----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient ^{(1) (2)} | | | 200 | $^\circ\text{C/W}$ |
| | Thermal Resistance Junction to Ambient ^{(3) (2)} | | | 94 | $^\circ\text{C/W}$ |

(1) Device mounted on FR4 material with Minimum Cu mounting area.

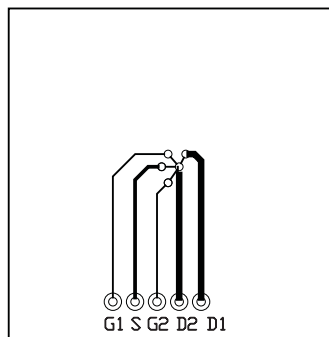
(2) Measured with both devices biased in a parallel condition.

(3) Device mounted on FR4 material with 1-inch² of Cu (2oz).



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Max $R_{\theta JA} = 94^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

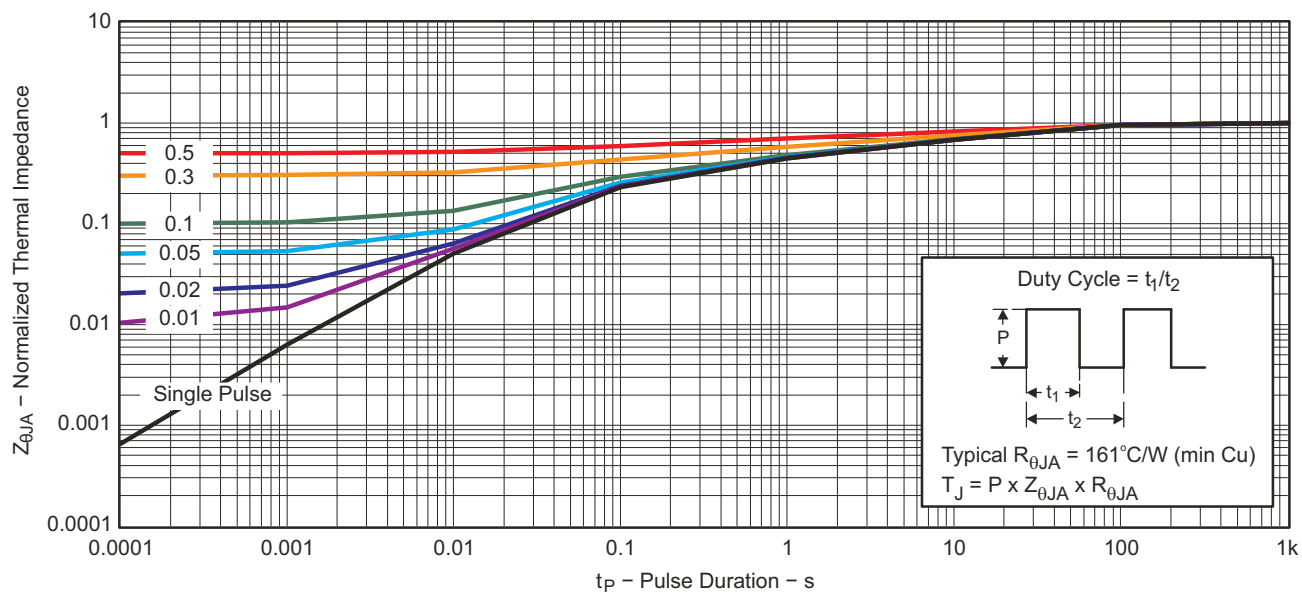


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Max $R_{\theta JA} = 200^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

Graphs are Per MOSFET at $T_A = 25^{\circ}\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at $T_A = 25^\circ\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

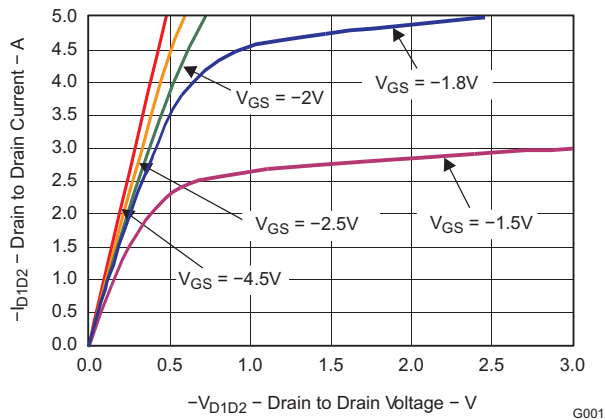


Figure 2. Saturation Characteristics

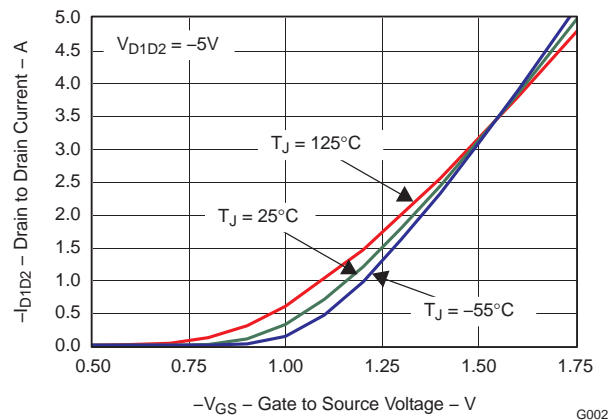


Figure 3. Transfer Characteristics

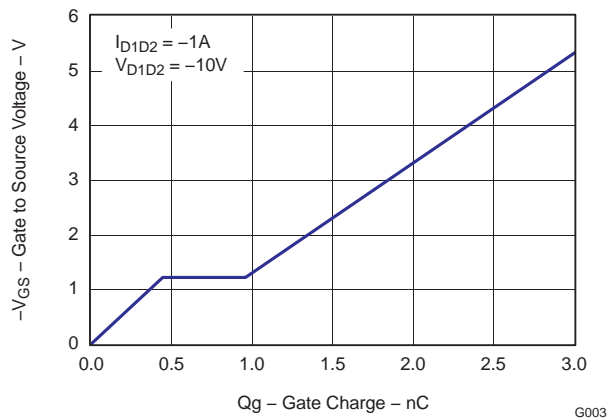


Figure 4. Gate Charge

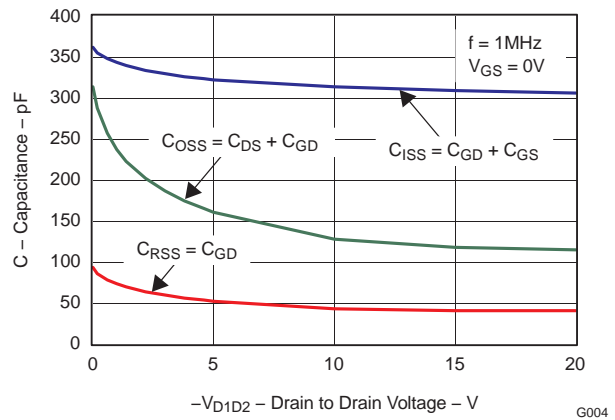


Figure 5. Capacitance

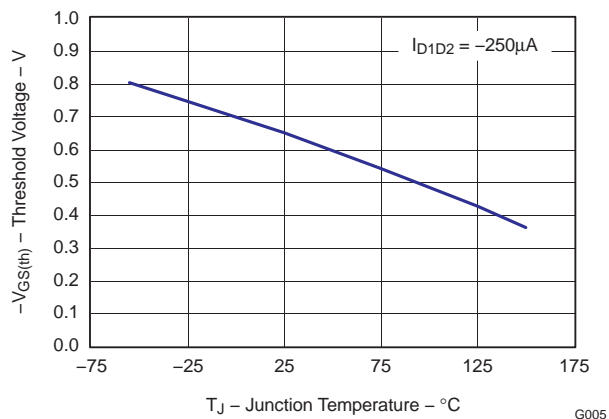


Figure 6. Threshold Voltage vs. Temperature

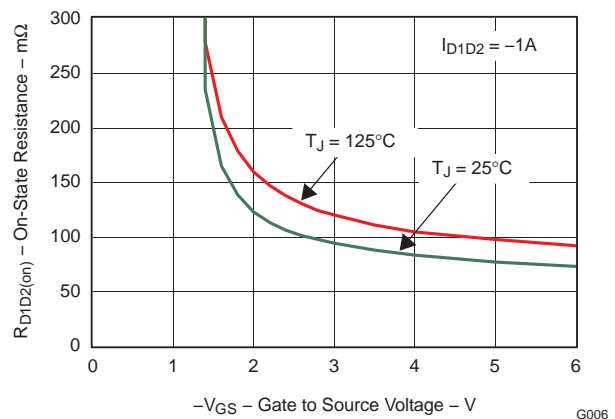


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at $T_A = 25^\circ\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

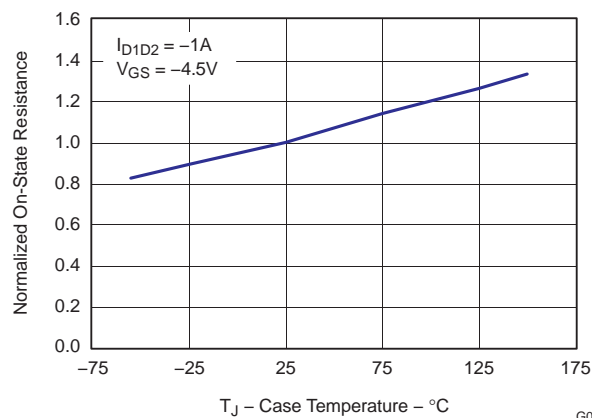


Figure 8. Normalized On-State Resistance vs. Temperature

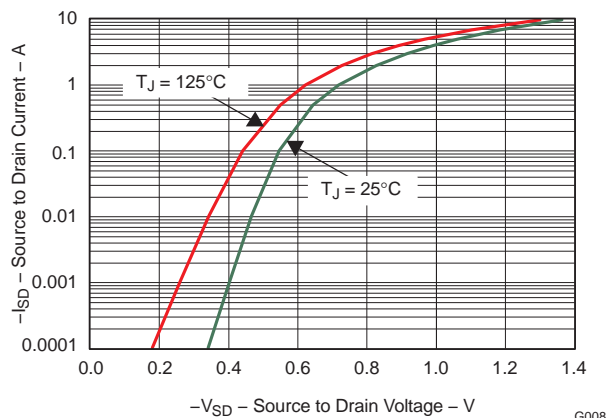


Figure 9. Typical Diode Forward Voltage

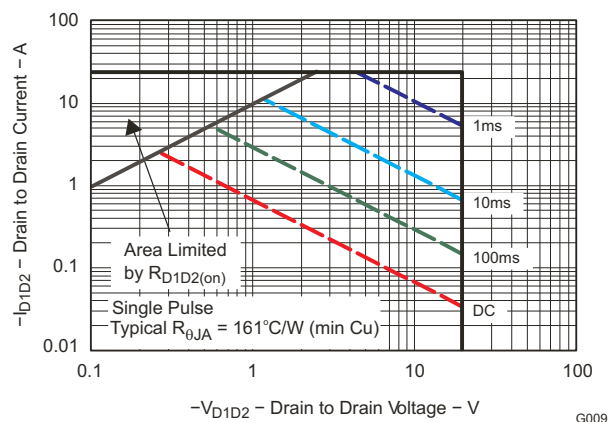


Figure 10. Maximum Safe Operating Area

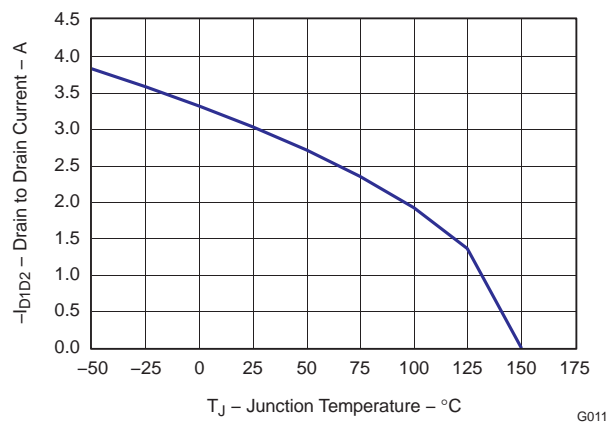
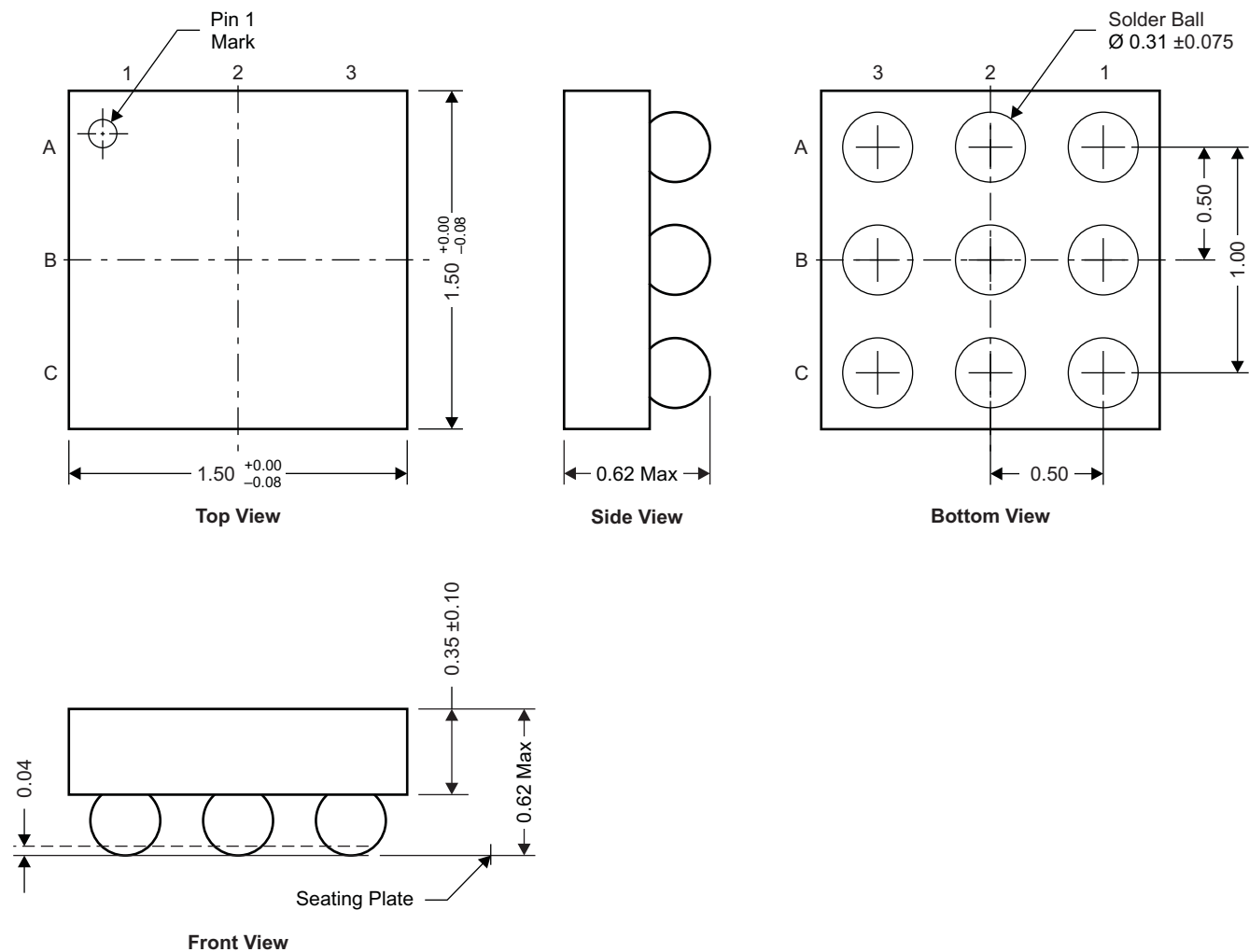


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA**CSD75204W15 Package Dimensions**

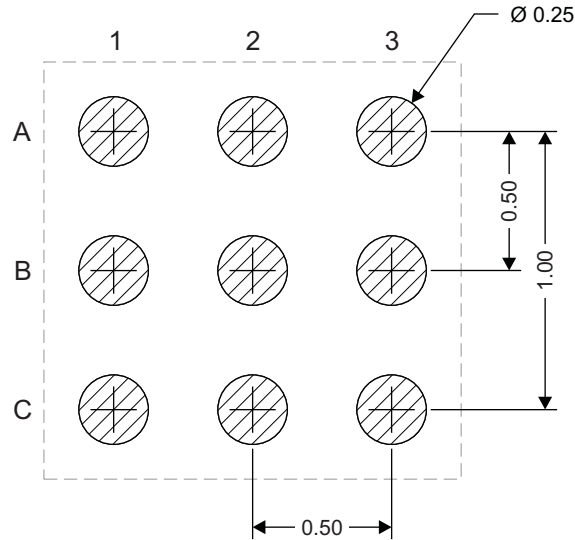
NOTE: All dimensions are in mm (unless otherwise specified)

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Pinout

| POSITION | DESIGNATION |
|------------|--------------|
| A1 | Gate1 |
| A2, A3, B3 | Drain1 |
| C1 | Gate2 |
| C2, C3, B2 | Drain2 |
| B1 | Source Sense |

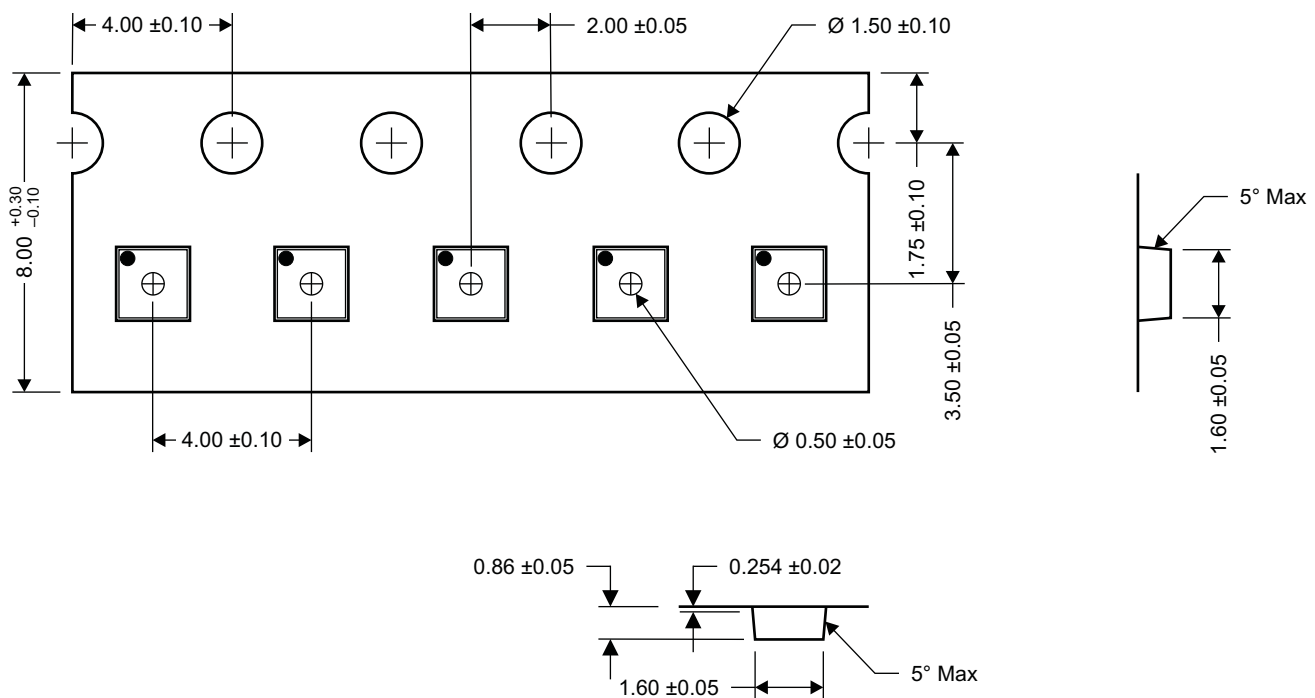
Land Pattern Recommendation



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0173-01

NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

| Changes from Original (October 2009) to Revision A | Page |
|---|-------------------|
| • Deleted the Package Marking Information section | 7 |

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