

## 2.5 V or 3.3 V, 200 MHz, 1:9 Clock Distribution Buffer

### Features

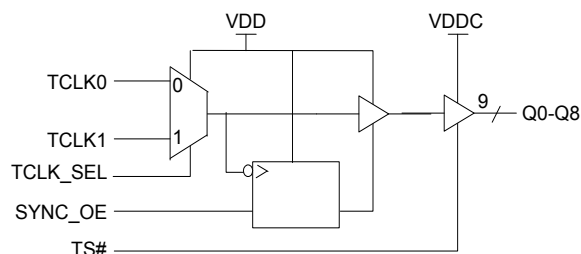
- 2.5 V or 3.3 V operation
- 200 MHz clock support
- LVCMOS-/LVTTTL-compatible inputs
- 9 clock outputs: drive up to 18 clock lines
- Synchronous Output Enable
- Output three-state control
- 250 ps max. output-to-output skew
- Pin compatible with MPC947, MPC9447
- Available in Industrial and Commercial temp. range
- 32-pin TQFP package

### Description

The CY29947 is a low-voltage 200 MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTTL compatible clock inputs. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTTL compatible. The 9 outputs are LVCMOS or LVTTTL compatible and can drive 50  $\Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:18. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the CY29947 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The CY29947 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

### Block Diagram



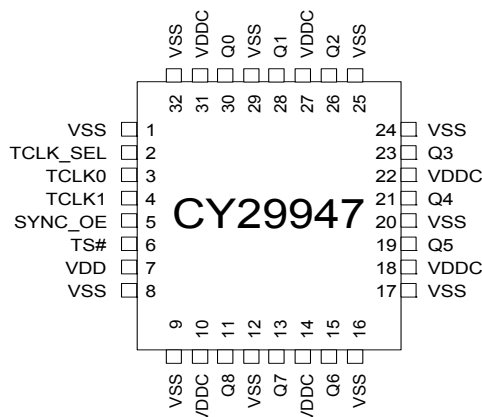
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## Pinouts

**Figure 1. 32-pin TQFP pinout**



## Pin Definitions <sup>[1]</sup>

Pin	Name	PWR	I/O	Description
3	TCLK0		I, PU	<b>Test Clock Input</b>
4	TCLK1		I, PU	<b>Test Clock Input</b>
2	TCLK_SEL		I, PU	<b>Test Clock Select Input.</b> When LOW, TCLK0 is selected. When asserted HIGH, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q(8:0)	VDDC	O	<b>Clock Outputs</b>
5	SYNC_OE		I, PU	<b>Output Enable Input.</b> When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	<b>Three-state Control Input.</b> When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 27, 31	VDDC			<b>3.3 V or 2.5 V Power Supply for Output Clock Buffers</b>
7	VDD			<b>3.3 V or 2.5 V Power Supply</b>
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	VSS			<b>Common Ground</b>

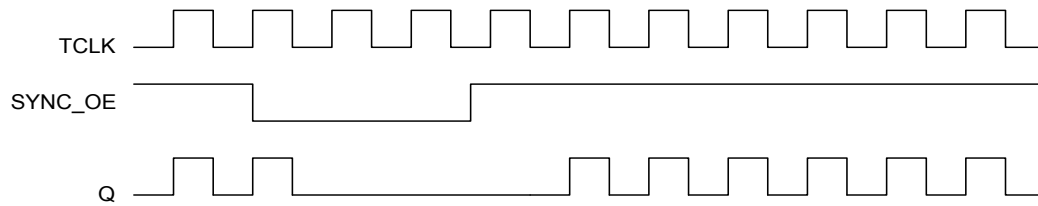
### Note

1. PD = internal pull-down, PU = internal pull-up.

## Output Enable/Disable

The CY29947 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC\_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC\_OE is set HIGH, the outputs are enabled as shown in [Figure 2](#).

**Figure 2. SYNC\_OE Timing Diagram**



## Maximum Ratings

Exceeding maximum ratings <sup>[2]</sup> may shorten the useful life of the device. User guidelines are not tested.

Maximum Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3\text{ V}$

Maximum Input Voltage Relative to  $V_{DD}$ : .....  $V_{DD} + 0.3\text{ V}$

Storage Temperature: .....  $-65\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$

Operating Temperature: .....  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Maximum ESD protection .....  $2\text{ kV}$

Maximum Power Supply: .....  $5.5\text{ V}$

Maximum Input Current: .....  $\pm 20\text{ mA}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

## DC Parameters

$V_{DD} = V_{DDC} = 3.3\text{ V} \pm 10\%$  or  $2.5\text{ V} \pm 5\%$ , Over the specified temperature range

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input Low Voltage		$V_{SS}$	–	0.8	V
$V_{IH}$	Input High Voltage		2.0	–	$V_{DD}$	V
$I_{IL}$	Input Low Current <sup>[3]</sup>		–	–	–100	$\mu\text{A}$
$I_{IH}$	Input High Current <sup>[3]</sup>		–	–	10	$\mu\text{A}$
$V_{OL}$	Output Low Voltage <sup>[4]</sup>	$I_{OL} = 20\text{ mA}$	–	–	0.4	V
$V_{OH}$	Output High Voltage <sup>[4]</sup>	$I_{OH} = -20\text{ mA}$ , $V_{DD} = 3.3\text{ V}$	2.5	–	–	V
		$I_{OH} = -20\text{ mA}$ , $V_{DD} = 2.5\text{ V}$	1.8	–	–	
$I_{DDQ}$	Quiescent Supply Current		–	5	7	mA
$I_{DD}$	Dynamic Supply Current	$V_{DD} = 3.3\text{ V}$ , Outputs @ 100 MHz, $CL = 30\text{ pF}$	–	120	–	mA
		$V_{DD} = 3.3\text{ V}$ , Outputs @ 160 MHz, $CL = 30\text{ pF}$	–	200	–	
		$V_{DD} = 2.5\text{ V}$ , Outputs @ 100 MHz, $CL = 30\text{ pF}$	–	85	–	
		$V_{DD} = 2.5\text{ V}$ , Outputs @ 160 MHz, $CL = 30\text{ pF}$	–	140	–	
$Z_{out}$	Output Impedance	$V_{DD} = 3.3\text{ V}$	12	15	18	$\Omega$
		$V_{DD} = 2.5\text{ V}$	14	18	22	
$C_{in}$	Input Capacitance		–	4	–	pF

### Notes

- Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Inputs have pull-up/pull-down resistors that effect input current.
- Driving series or parallel terminated  $50\text{ }\Omega$  (or  $50\text{ }\Omega$  to  $V_{DD}/2$ ) transmission lines.

## AC Parameters

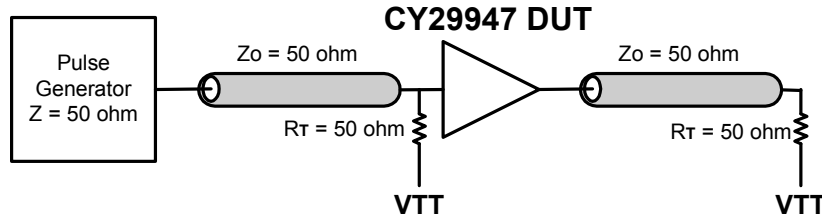
$V_{DD} = V_{DDC} = 3.3 \text{ V} \pm 10\%$  or  $2.5 \text{ V} \pm 5\%$ , Over the specified temperature range

Parameter <sup>[5]</sup>	Description	Conditions	Min	Typ	Max	Unit
Fmax	Input Frequency <sup>[6]</sup>	$V_{DD} = 3.3 \text{ V}$	–	–	200	MHz
		$V_{DD} = 2.5 \text{ V}$	–	–	170	
Tpd	TCLK To Q Delay <sup>[6]</sup>	$V_{DD} = 3.3 \text{ V}$	4.75	–	9.25	ns
		$V_{DD} = 2.5 \text{ V}$	6.50	–	10.50	
FoutDC	Output Duty Cycle <sup>[6, 7]</sup>	Measured at $V_{DD}/2$	45	–	55	%
tpZL, tpZH	Output Enable Time (all outputs)		2	–	10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2	–	10	ns
Tskew	Output-to-Output Skew <sup>[6, 8]</sup>		–	150	250	ps
Tskew(pp)	Part-to-Part Skew <sup>[9]</sup>		–	–	2.0	ns
Ts	Set-up Time <sup>[6, 10]</sup>	SYNC_OE to TCLK	0.0	–	–	ps
Th	Hold Time <sup>[6, 10]</sup>	TCLK to SYNC_OE	1.0	–	–	ps
Tr/Tf	Output Clocks Rise/Fall Time <sup>[8]</sup>	0.8 V to 2.0 V, $V_{DD} = 3.3 \text{ V}$	0.20	–	1.0	ns
		0.6 V to 1.8 V, $V_{DD} = 2.5 \text{ V}$	0.20	–	1.3	

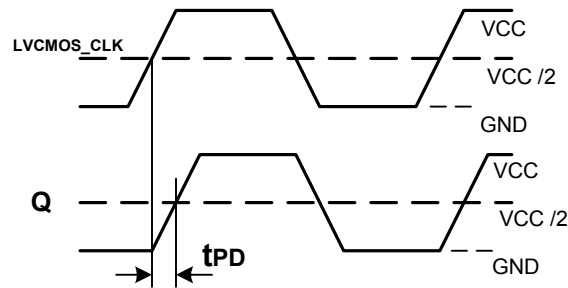
### Notes

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving  $50 \Omega$  transmission lines.
7. 50% input duty cycle.
8. See [Figure 3 on page 7](#).
9. Part-to-Part skew at a given temperature and voltage.
10. Set-up and hold times are relative to the falling edge of the input clock.

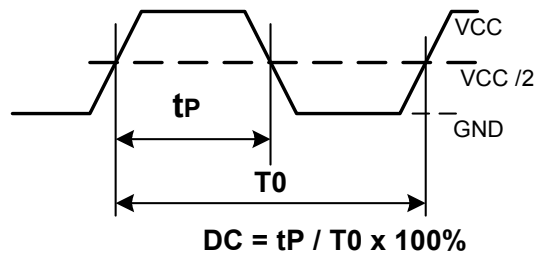
**Figure 3. LVCMOS\_CLK CY29947 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$**



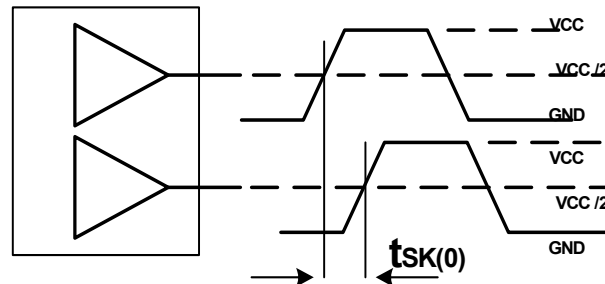
**Figure 4. LVCMOS Propagation Delay (TPD) Test Reference**



**Figure 5. Output Duty Cycle (FoutDC)**



**Figure 6. Output-to-Output Skew tsk(0)**





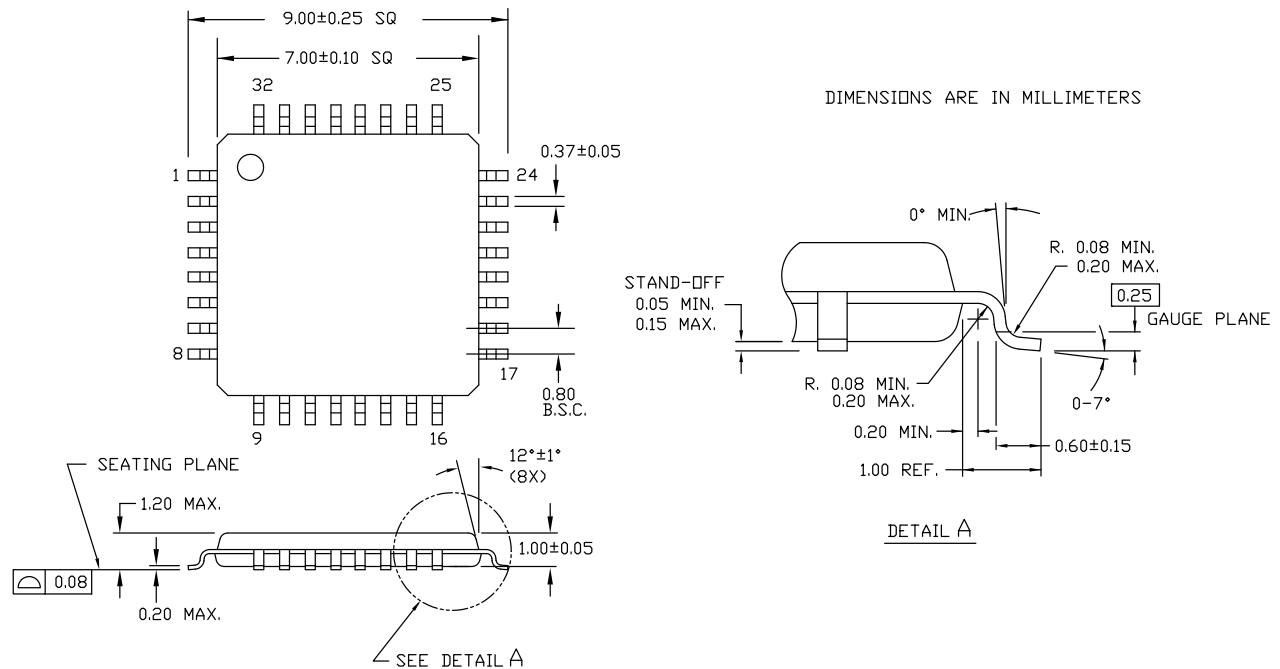
Part Number	Package Type	Production Flow
CY29947AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29947AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to +85 °C
CY29947AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29947AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to +70 °C

CY 29947 A X X T  
 \_\_\_\_\_ T = Tape and Reel  
 \_\_\_\_\_ Temperature Range: X = C or I  
 C = Commercial; I = Industrial  
 \_\_\_\_\_ Pb-free  
 \_\_\_\_\_ Package Type:  
 A = 32-pin TQFP  
 \_\_\_\_\_ Base Device Part Number  
 \_\_\_\_\_ Company ID: CY = Cypress



## Package Drawing and Dimension

**Figure 7. 32-pin TQFP (7 × 7 × 1.0 mm) Package Outline, 51-85063**



51-85063 \*D

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
I/O	Input/Output
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	Phase Locked Loop
TQFP	Thin Quad Flat Pack
VCO	Voltage-Controlled Oscillator

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kV	kilovolt
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

## Revision History

Document Title: CY29947, 2.5 V or 3.3 V, 200 MHz, 1:9 Clock Distribution Buffer Document Number: 38-07287				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	111098	02/07/02	BRK	New data sheet
*A	116781	08/14/02	HWT	Added Commercial Temperature Range in the ordering information
*B	118462	09/09/02	HWT	Corrected the Package Drawing and Dimension in page 6 from 32 LQFP to 32 TQFP
*C	122879	12/22/02	RBI	Added power up requirements to Maximum Ratings
*D	2899714	03/26/10	BASH	Removed inactive parts from the ordering table. Replaced with active parts. Updated package diagram
*E	3163585	02/05/2011	CXQ	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.
*F	4311272	03/17/2014	CINM	Updated <a href="#">Package Drawing and Dimension</a> : spec 51-85063 – Changed revision from *C to *D.  Updated in new template.  Completing Sunset Review.

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