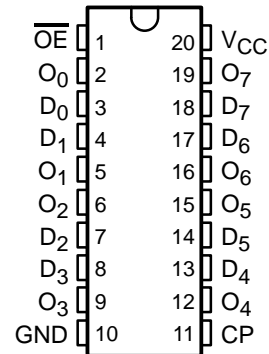


# CY54FCT374T, CY74FCT374T 8-BIT REGISTERS WITH 3-STATE OUTPUTS

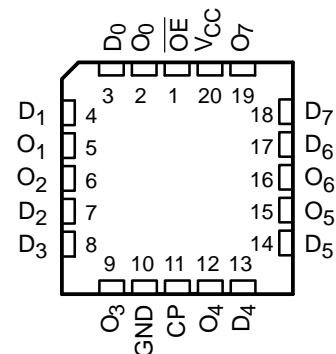
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- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Edge-Triggered D-Type Inputs
- 250-MHz Typical Switching Rate
- CY54FCT374T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT374T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

CY54FCT374T . . . D PACKAGE  
CY74FCT374T . . . P, Q, OR SO PACKAGE  
(TOP VIEW)



CY54FCT374T . . . L PACKAGE  
(TOP VIEW)



## description

The 'FCT374T devices are high-speed, low-power, octal D-type flip-flops, featuring separate D-type inputs for each flip-flop. These devices have 3-state outputs for bus-oriented applications. A buffered clock (CP) and output-enable ( $\overline{OE}$ ) inputs are common to all flip-flops. The eight flip-flops in the 'FCT374T store the state of their individual D inputs that meet the setup-time and hold-time requirements on the low-to-high CP transition. When  $\overline{OE}$  is low, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. The state of  $\overline{OE}$  does not affect the state of the flip-flops.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT374T, CY74FCT374T
8-BIT REGISTERS
WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.2	CY74FCT374CTQCT	FCT374C
	SOIC – SO	Tube	5.2	CY74FCT374CTSOC	FCT374C
		Tape and reel	5.2	CY74FCT374CTSOCT	
	DIP – P	Tube	6.5	CY74FCT374ATPC	CY74FCT374ATPC
	QSOP – Q	Tape and reel	6.5	CY74FCT374ATQCT	FCT374A
	SOIC – SO	Tube	6.5	CY74FCT374ATSOC	FCT374A
		Tape and reel	6.5	CY74FCT374ATSOCT	
	QSOP – Q	Tape and reel	10	CY74FCT374TQCT	FCT374
–55°C to 125°C	SOIC – SO	Tube	10	CY74FCT374TSOC	FCT374
		Tape and reel	10	CY74FCT374TSOCT	
	CDIP – D	Tube	6.2	CY54FCT374CTDMB	
	LCC – L	Tube	6.2	CY54FCT374CTLMB	
	CDIP – D	Tube	7.2	CY54FCT374ATDMB	
	LCC – L	Tube	7.2	CY54FCT374ATLMB	
	CDIP – D	Tube	11	CY54FCT374TDMB	
	LCC – L	Tube	11	CY54FCT374TLMB	

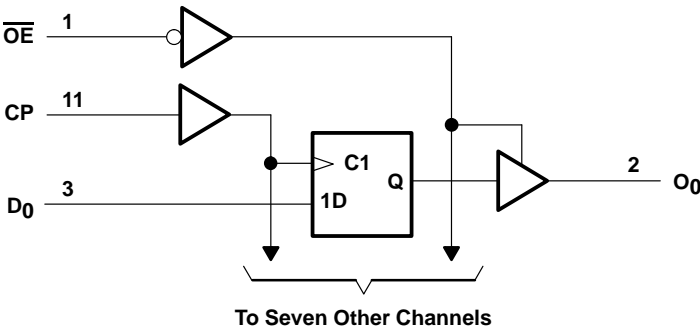
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE

INPUTS			OUTPUT
D	CP	$\overline{OE}$	O
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = High logic level, L = Low logic level,  
X = Don't care, Z = High-impedance state,  
↑ = Low-to-high clock transition

logic diagram (positive logic)



**CY54FCT374T, CY74FCT374T**  
**8-BIT REGISTERS**  
**WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): P package	69°C/W
Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, $T_A$	–65°C to 135°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	CY54FCT374T			CY74FCT374T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current			–12			–32	mA
$I_{OL}$ Low-level output current			32			64	mA
$T_A$ Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



# CY54FCT374T, CY74FCT374T

## 8-BIT REGISTERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT374T			CY74FCT374T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_{IN} = -18 \text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75 \text{ V}$ , $I_{IN} = -18 \text{ mA}$				-0.7	-1.2		
$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$				2			
					2.4	3.3		
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 32 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$ , $I_{OL} = 64 \text{ mA}$				0.3	0.55		
$V_{hys}$	All inputs	0.2			0.2			V
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = V_{CC}$			5				$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = V_{CC}$						5	
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.7 \text{ V}$			$\pm 1$				$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 2.7 \text{ V}$						$\pm 1$	
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.5 \text{ V}$			$\pm 1$				$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 0.5 \text{ V}$						$\pm 1$	
$I_{off}$	$V_{CC} = 0 \text{ V}$ , $V_{OUT} = 4.5 \text{ V}$			$\pm 1$			$\pm 1$	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_{CC} = 5.5 \text{ V}$ , $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$ , $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
$I_{OZH}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.7 \text{ V}$			10				$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 2.7 \text{ V}$						10	
$I_{OZL}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.5 \text{ V}$			-10				$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 0.5 \text{ V}$						-10	
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} \leq 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} \leq 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
$\Delta I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 3.4 \text{ V}^\S$ , $f_1 = 0$ , Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 3.4 \text{ V}^\S$ , $f_1 = 0$ , Outputs open				0.5	2		

† Typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4 \text{ V}$ ); all other inputs at  $V_{CC}$  or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT374T			CY74FCT374T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I <sub>CCD</sub> ††	V <sub>CC</sub> = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.06	0.12				mA/ MHz
	V <sub>CC</sub> = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V							0.06	0.12	
I <sub>C</sub>	V <sub>CC</sub> = 5.5 V, f <sub>0</sub> = 10 MHz, Outputs open, $\overline{OE}$ = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V		0.7	1.4				mA
			V <sub>IN</sub> = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V		1.6	3.2				
			V <sub>IN</sub> = 3.4 V or GND		3.9	12.2				
	V <sub>CC</sub> = 5.25 V, f <sub>0</sub> = 10 MHz, Outputs open, $\overline{OE}$ = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V					0.7	1.4	
			V <sub>IN</sub> = 3.4 V or GND					1.2	3.4	
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V					1.6	3.2	
			V <sub>IN</sub> = 3.4 V or GND					3.9	12.2	
C <sub>i</sub>					5	10		5	10	pF
C <sub>O</sub>					9	12		9	12	pF

† Typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

†† This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4$  V)

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

# CY54FCT374T, CY74FCT374T

## 8-BIT REGISTERS

## WITH 3-STATE OUTPUTS

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		CY54FCT374T		CY54FCT374AT		CY54FCT374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, CP high or low	7		6		6		ns
t <sub>su</sub>	Setup time, data before CP↑	2		2		2		ns
t <sub>h</sub>	Hold time, data after CP↑	1.5		1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		CY74FCT374T		CY74FCT374AT		CY74FCT374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, CP high or low	7		5		5		ns
t <sub>su</sub>	Setup time, data before CP↑	2		2		2		ns
t <sub>h</sub>	Hold time, data after CP↑	1.5		1.5		1.5		ns

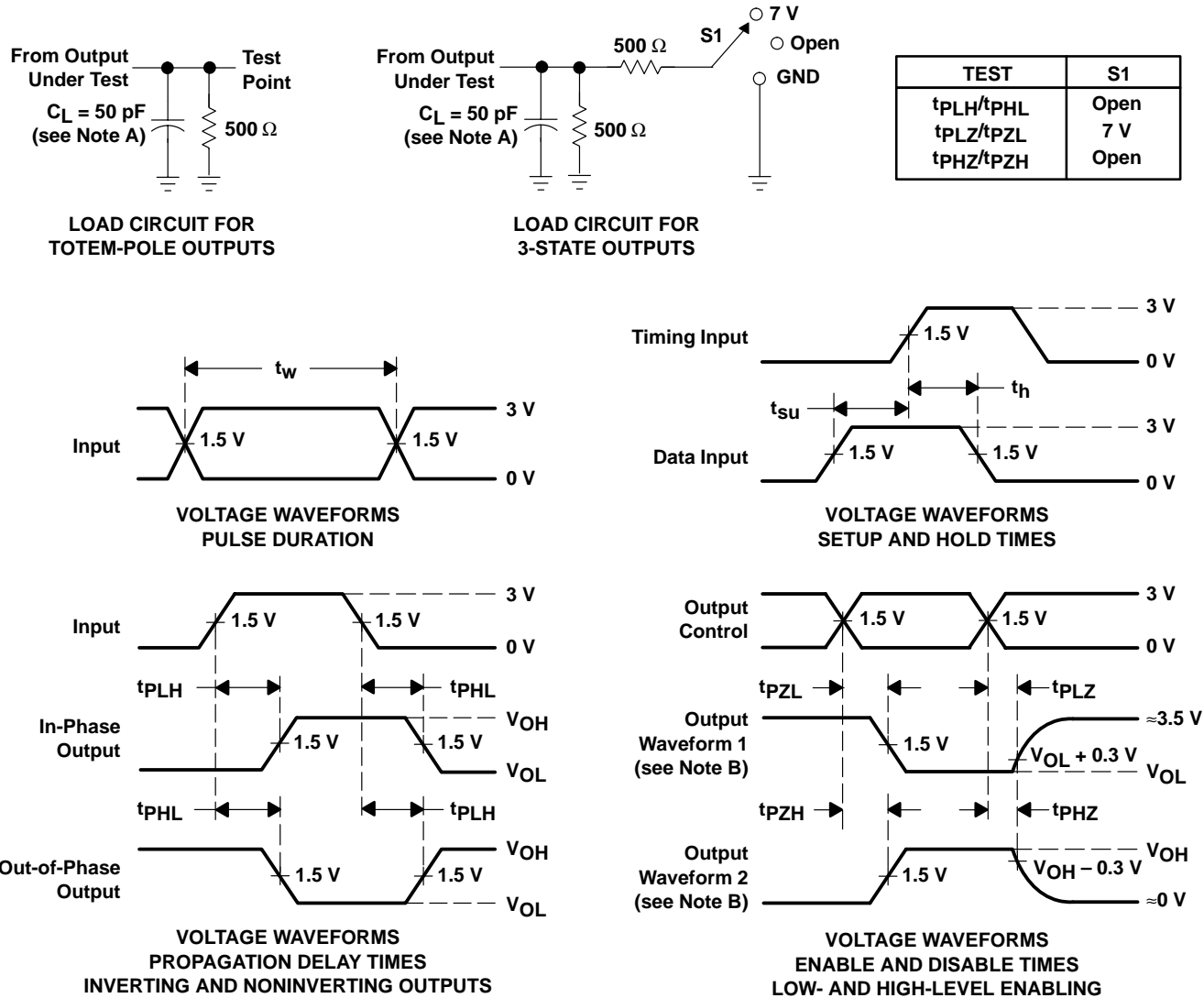
**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT374T		CY54FCT374AT		CY54FCT374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CP	O	2	11	2	7.2	2	6.2	ns
t <sub>PHL</sub>			2	11	2	7.2	2	6.2	
t <sub>PZH</sub>	$\overline{OE}$	O	1.5	14	1.5	7.5	1.5	6.2	ns
t <sub>PZL</sub>			1.5	14	1.5	7.5	1.5	6.2	
t <sub>PHZ</sub>	$\overline{OE}$	O	1.5	8	1.5	6.5	1.5	5.7	ns
t <sub>PLZ</sub>			1.5	8	1.5	6.5	1.5	5.7	

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT374T		CY74FCT374AT		CY74FCT374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CP	O	2	10	2	6.5	2	5.2	ns
t <sub>PHL</sub>			2	10	2	6.5	2	5.2	
t <sub>PZH</sub>	$\overline{OE}$	O	1.5	12.5	1.5	6.5	1.5	5.5	ns
t <sub>PZL</sub>			1.5	12.5	1.5	6.5	1.5	5.5	
t <sub>PHZ</sub>	$\overline{OE}$	O	1.5	8	1.5	5.5	1.5	5	ns
t <sub>PLZ</sub>			1.5	8	1.5	5.5	1.5	5	

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9221802M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9221802M2A CY54FCT 374TLMB	<a href="#">Samples</a>
5962-9221802MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221802MR A CY54FCT374TDMB	<a href="#">Samples</a>
5962-9221804M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9221804M2A CY54FCT 374ATLMB	<a href="#">Samples</a>
5962-9221804MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221804MR A CY54FCT374ATDM B	<a href="#">Samples</a>
5962-9221806M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9221806M2A CY54FCT 374CTLMB	<a href="#">Samples</a>
5962-9221806MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221806MR A	<a href="#">Samples</a>
5962-9222203M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9222203M2A CY54FCT 574ATLMB	<a href="#">Samples</a>
5962-9222203MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9222203MR A	<a href="#">Samples</a>
5962-9222205MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9222205MR A	<a href="#">Samples</a>
CY54FCT374ATDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221804MR A CY54FCT374ATDM B	<a href="#">Samples</a>
CY54FCT374ATLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type		5962- 9221804M2A CY54FCT 374ATLMB	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY54FCT374CTLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9221806M2A CY54FCT 374CTLMB	<a href="#">Samples</a>
CY54FCT374TDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9221802MR A CY54FCT374TDMB	<a href="#">Samples</a>
CY54FCT374TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9221802M2A CY54FCT 374TLMB	<a href="#">Samples</a>
CY54FCT574ATLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9222203M2A CY54FCT 574ATLMB	<a href="#">Samples</a>
CY74FCT374ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	CY74FCT374ATPC	<a href="#">Samples</a>
CY74FCT374ATQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374A	<a href="#">Samples</a>
CY74FCT374ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374A	<a href="#">Samples</a>
CY74FCT374ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374A	<a href="#">Samples</a>
CY74FCT374CTQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374C	<a href="#">Samples</a>
CY74FCT374CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374C	<a href="#">Samples</a>
CY74FCT374TQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374	<a href="#">Samples</a>
CY74FCT374TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374	<a href="#">Samples</a>
CY74FCT374TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374	<a href="#">Samples</a>
CY74FCT574ATQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT574A	<a href="#">Samples</a>
CY74FCT574ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT574A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT574ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT574A	<a href="#">Samples</a>
CY74FCT574ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT574A	<a href="#">Samples</a>
CY74FCT574CTQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT574C	<a href="#">Samples</a>
CY74FCT574CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT574C	<a href="#">Samples</a>
CY74FCT574CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT574C	<a href="#">Samples</a>
CY74FCT574TQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT574	<a href="#">Samples</a>
CY74FCT574TQCTG4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT574	<a href="#">Samples</a>
CY74FCT574TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT574	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT374ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT374ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT374CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT374TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT374TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT574ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT574ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT574CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT574CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT574TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT374ATQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT374ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT374CTQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT374TQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT374TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT574ATQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT574ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT574CTQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT574CTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT574TQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0

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