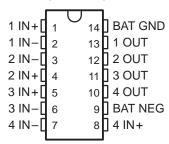
- Designed for –52-V Battery Operation
- 50-mA Output Current Capability
- Input Compatible With TTL and CMOS
- High Common-Mode Input Voltage Range
- Very Low Input Current
- Fail-Safe Disconnect Feature
- Built-in Output Clamp Diode
- Direct Replacement for National DS3680 and Fairchild μA3680

#### description

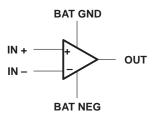
The DS3680 telephone relay driver is a monolithic integrated circuit designed to interface -48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard -52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output is off as a fail-safe condition when either output is open.

The DS3680 is characterized for operation from 0°C to 70°C.

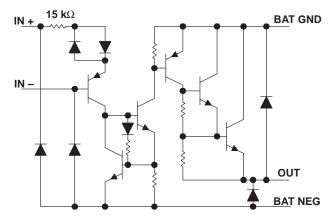
#### D OR N PACKAGE (TOP VIEW)



#### symbol (each driver)



#### schematic diagram (each driver)



All resistor values shown are nominal.

SLRS014C - MARCH 1986 - REVISED SEPTEMBER 1995

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V <sub>BAT</sub> (see Note 1)	–70 V to 0.5 V
Input voltage range with respect to BAT GND	–70 V to 20 V
Input voltage range with respect to BAT NEG	0.5 V to 70 V
Differential input voltage, V <sub>ID</sub> (see Note 2)	±20 V
Output current, IO: Resistive load	–100 mA
Inductive load	–50 mA
Inductive output load	5 H
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub>	0°C to 70°C
Storage temperature range, T <sub>stq</sub>	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	260°C

NOTES: 1. All voltages are with respect to BAT GND, unless otherwise specified.

2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN-.

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING		
D	950 mW	7.6 mW/°C	608 mW		
N	1150 mW	9.2 mW/°C	736 mW		

#### recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, VBAT-	-10	-60	V
Input voltage, either input	-20†	20	V
High-level differential input voltage, V <sub>IDH</sub>	2	20	V
Low-level differential input voltage, V <sub>IDL</sub>	-20†	0.8	V
Operating free-air temperature, T <sub>A</sub>	0	70	°C

<sup>†</sup> The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

# electrical characteristics over recommended operating free-air temperature range, $V_{BAT-} = -52 \text{ V}$ (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	MIN TY	<b>p</b> ‡	MAX	UNIT
1	High-level input current (into IN+)	V <sub>ID</sub> = 2 V			40	100	μΑ
lΉ	nigh-level input current (into in+)	V <sub>ID</sub> = 7 V		3	75	1000	μΑ
1	Low level input current (into IN L.)	V <sub>ID</sub> = 0.4 V		0.	01	5	^
lir	Low-level input current (into IN+)	$V_{ID} = -7 V$		-1	-100	μΑ	
V <sub>O(on)</sub>	On-stage output voltage	$I_O = 50 \text{ mA},$	V <sub>ID</sub> = 2 V	-1	.6	-2.1	V
la ( m	Off stage output ourrent	\/a \/a	V <sub>ID</sub> = 0.8 V		-2	-100	^
IO(off)	Off-stage output current	VO = VBAT-	Inputs open	-	- 2	-100	μΑ
I <sub>R</sub>	Clamp diode reverse current	V <sub>O</sub> = 0			2	100	μΑ
Vall	Output clamp voltage	I <sub>O</sub> = 50 mA	(	0.9	1.2	V	
Vок	Output clamp voltage	$I_{O} = -50 \text{ mA},  V_{BAT} = 0$		-(	).9	-1.2	V
I <sub>BAT(on)</sub>	On-state battery current	All drivers on		-	-2	-4.4	mA
I <sub>BAT</sub> (off)	Off-state battery current	All drivers off		-	-1	-100	μΑ

<sup>‡</sup> All typical values are at T<sub>A</sub> = 25°C.



# switching characteristics $V_{BAT-}$ = -52 V, $T_A$ = 25°C

	PARAMETER	TEST CON	MIN	TYP	MAX	UNIT	
ton	Turn-on time	V <sub>ID</sub> = 3-V pulse,	$R_L = 1 k\Omega$ ,		1	10	μs
toff	Turn-off time	L = 1 H,	See Figure 2		1	10	μs

### PARAMETER MEASUREMENT INFORMATION

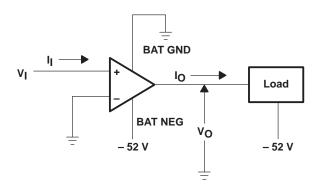


Figure 1. Generalized Test Circuit, Each Driver

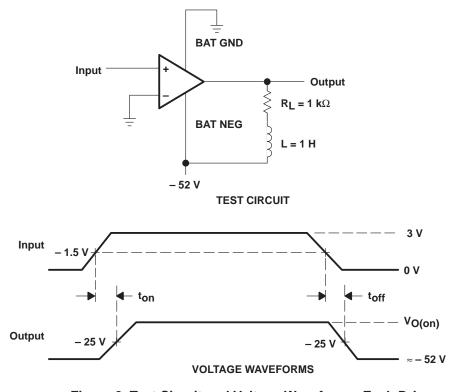


Figure 2. Test Circuit and Voltage Waveforms, Each Driver

#### **APPLICATION INFORMATION**

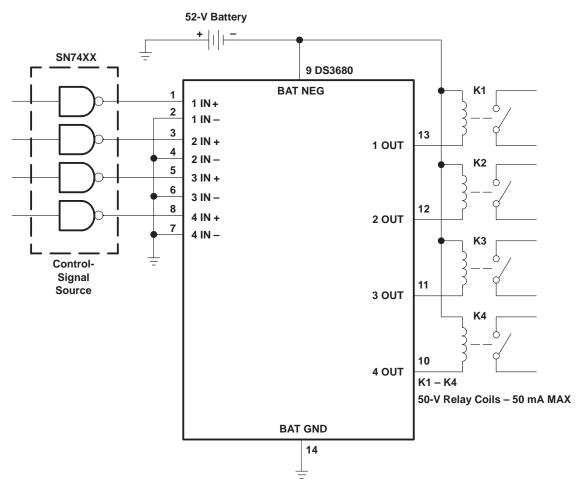


Figure 3. Relay Driver





10-Jun-2014

#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	<b>Device Marking</b> (4/5)	Samples
DS3680D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS3680	Samples
DS3680DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS3680	Samples
DS3680DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS3680	Samples
DS3680DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS3680	Samples
DS3680N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	DS3680N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



#### **PACKAGE OPTION ADDENDUM**

10-Jun-2014

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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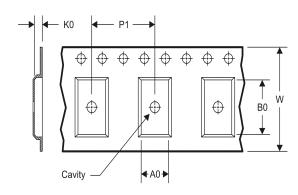
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#### TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

#### \*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3680DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 14-Jul-2012



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3680DR	SOIC	D	14	2500	367.0	367.0	38.0

# N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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