LM96530 Ultrasound Transmit/Receive Switch

Check for Samples: LM96530

FEATURES

- **8-Channel High-Voltage Receive Side Switches without Charge-Injection**
- **Can be Used for Receive Protection and/or Receive Multiplexing with SPI™ Compatible Bus Control**
- **Channel Bandwidth Supports 1MHz to 20MHz Transducers**
- **Input Accepts Pulses and Continuous-Wave Signals within ±60V**
- **Integrated Output Clamping Diodes Limit Output to ±0.7V**
- **Low Harmonic Distortion HD2 at -75dBc at 5MHz**
- **Continuous-Wave Operation**
- **Soft-Switcher Based on a Diode Bridge Architecture Yielding Better Noise Performance and Faster Turn-On and -Off Times than Competing T-Gate Switch Architectures**
- **2.5V to 3.3V CMOS SPI™ Compatible Logic Interface with Daisy Chain Capability**
- **Bias Current Source (I_S) can be Scaled between 0 and 8mA via an External Resistor**

APPLICATIONS

- **Ultrasound Imaging**

DESCRIPTION

The LM96530 is an eight-channel monolithic high-voltage, high-speed T/R (Transmit/Receive) switch for multi-channel medical ultrasound applications. It is well-suited for use with Texas Instrument's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96530 contains eight high-voltage T/R switches with integrated clamping diodes. This chip protects the inputs of the receive channel's LNA (Low Noise Amplifier) from the high-voltage pulses of the transmit channel. Advanced features include a diode bridge with internal current sources that are programmable via an external resistor. Low-power operation is enabled via per-channel-selectable switching.

Texas Instruments also offers a development package for sale which includes a driver hardware and software package with a graphical user interface for configuration and monitoring.

Table 1. Key Specifications

	VALUE	UNIT
Input voltage	±60	V
Output voltage clamp (I_S= 1mA)	±0.7	V
On-resistance	18	Ω
Off-isolation at 5MHz	-58	dB
Noise spectral density at 5MHz	0.5	nV/√Hz
Harmonic distortion		
HD2	-75	dB
HD3	-75	dB
Channel crosstalk at 5MHz	-73	dB
Operating Temp.	0 to +70	°C

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Block Diagram

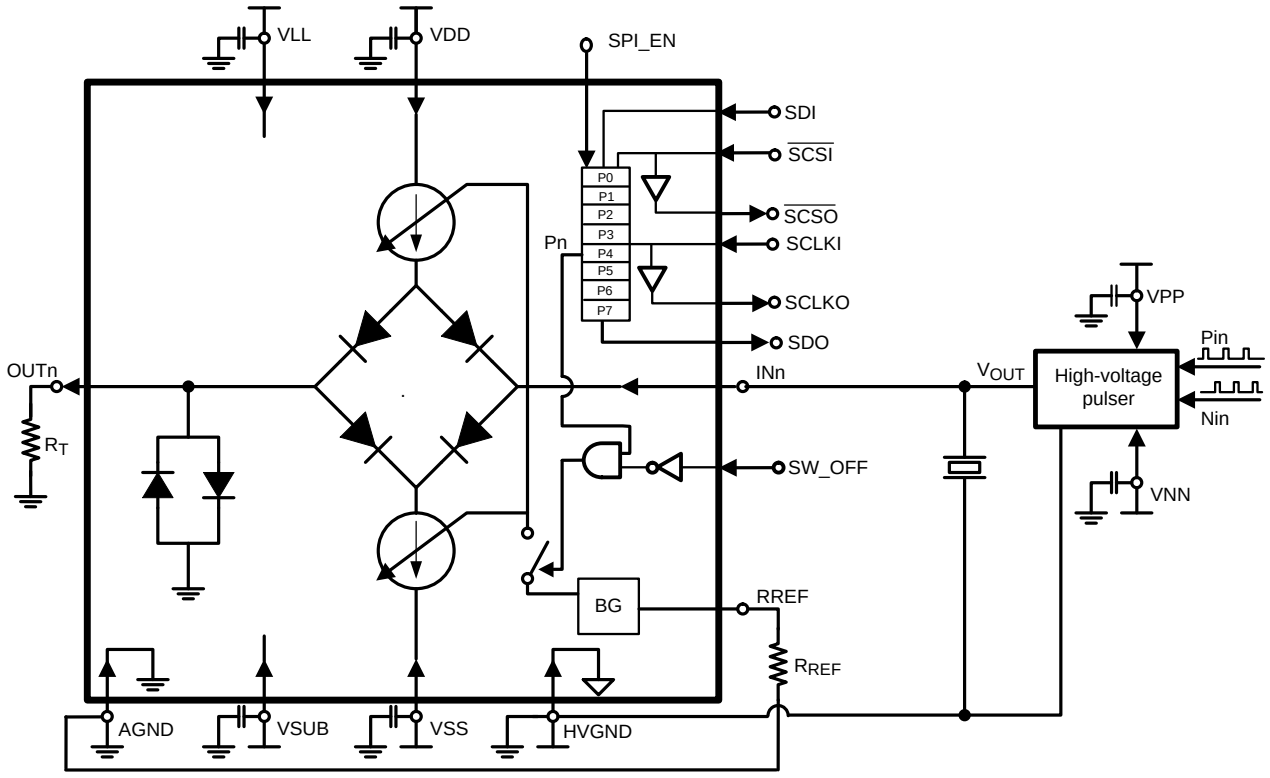

Figure 1.

Typical Application

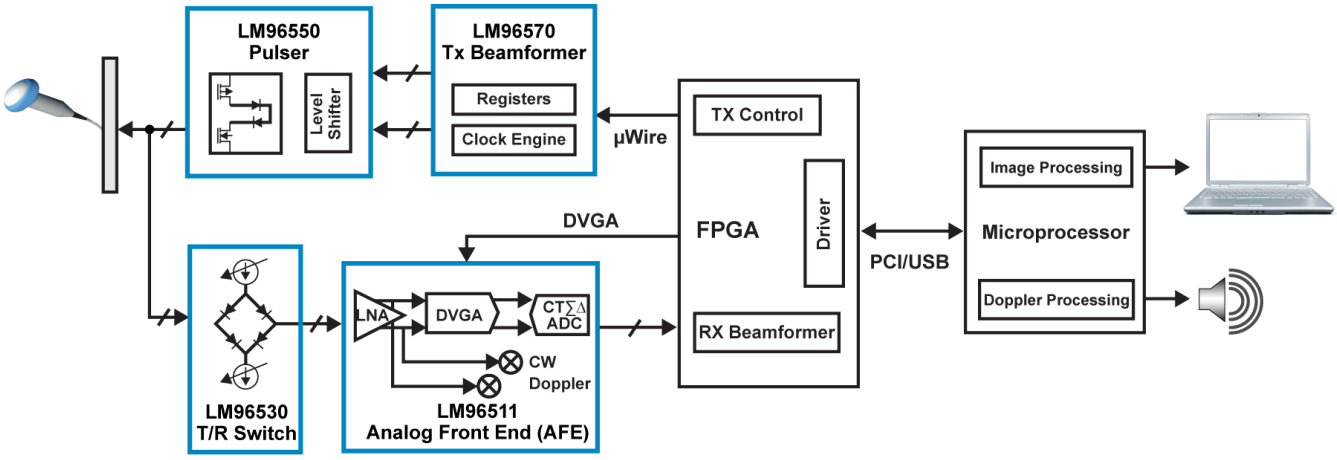

Figure 2. 8-Channel Transmit/Receive Chipset

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Pin Diagram

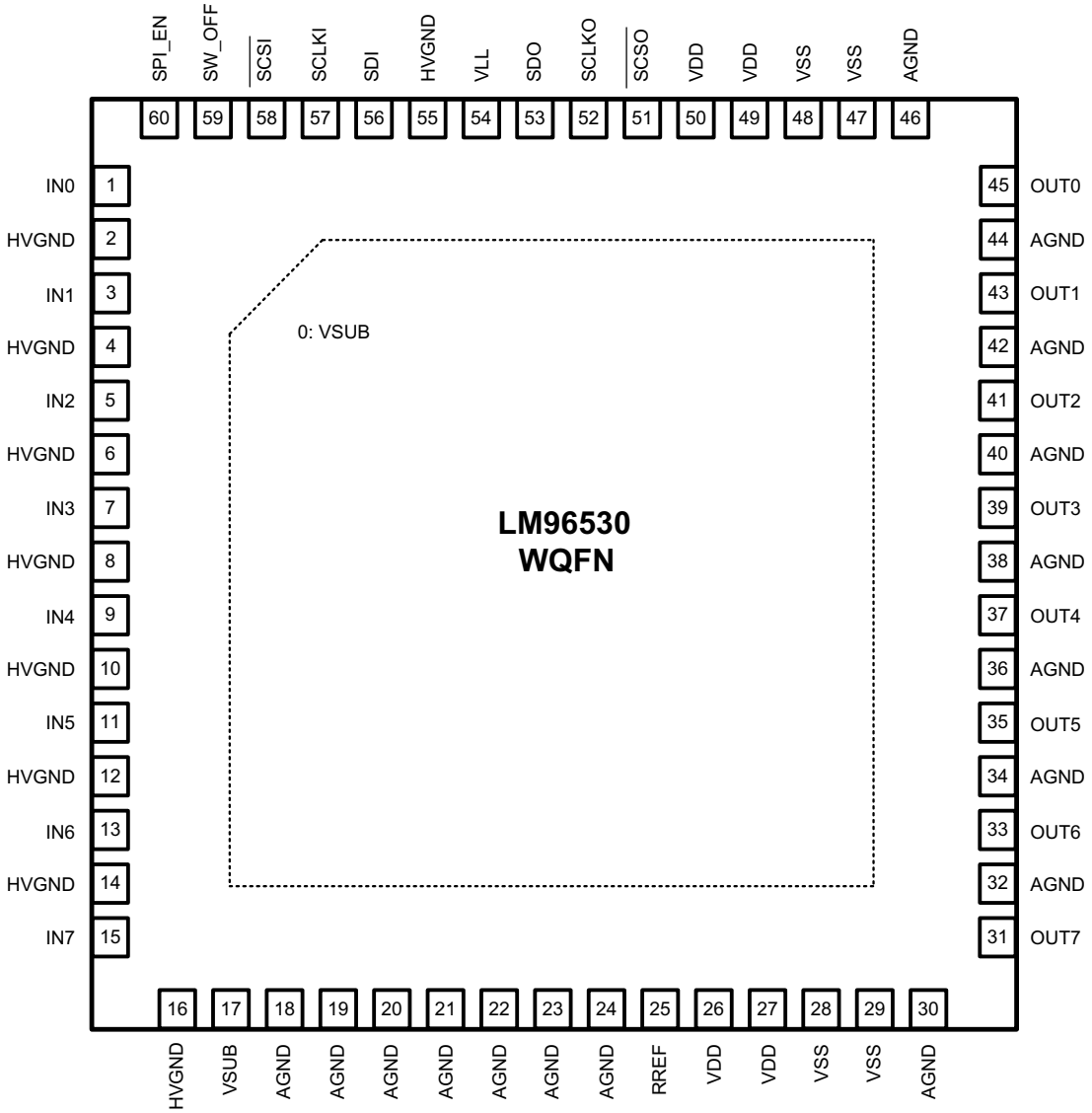

Figure 3. WQFN Package
See Package Number NKA0060A

PIN DESCRIPTIONS

Pin No.	Name	Type	Function and Connection
1, 3, 5, 7, 9, 11, 13, 15	INn n=0,...,7	Input	High-voltage input
45, 43, 41, 39, 37, 35, 33, 31	OUTn n=0,...	Output	Low-voltage output
25	RREF	Output	External resistor to AGND. Used to set internal current sources. R_{REF} = 6.25 kΩ → I_S = 8mA; R_{REF} = 12.5 kΩ → I_S = 4mA; R_{REF} = 25 kΩ → I_S = 2mA; R_{REF} = 50 kΩ → I_S = 1mA
59	SW_OFF	Input	1 = Switch all channels OFF 0 = Use SPI™ to control switch

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PIN DESCRIPTIONS (continued)

Pin No.	Name	Type	Function and Connection
60	SPI_EN	Input	1 = Enable the SPI™ Interface 0 = Disable the SPI™ Interface and presets SPI™ registers for all switches ON.
58	$\overline{SCSI}$	Input	SPI™ chip select input, 0 = Chip Select
57	SCKI	Input	SPI™ compatible clock input
56	SDI	Input	SPI™ compatible data input
53	SDO	Output	SPI™ compatible data buffered output
52	SCKO	Output	SPI™ compatible clock buffered output
51	$\overline{SCSO}$	Output	SPI™ chip select buffered output
26, 27, 49, 50	VDD	Power	Positive analog supply voltage (+5V)
28, 29, 47, 48	VSS	Power	Negative analog supply voltage (-5V)
54	VLL	Power	Logic voltage supply (+2.5 to 3.3V)
0, 17	VSUB	Power	Negative high voltage supply (-65V)
2, 4, 6, 8, 10, 12, 14, 16, 55	HVGND	Ground	High voltage reference potential (0V)
All others	AGND	Ground	Analog and logic low voltage reference input, logic ground (0V)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Maximum Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	−40°C to +125°C
Supply Voltage (VDD)	+0.3V to +5.5V
Supply Voltage (VSS)	+0.3V and −5.5V
Supply Voltage (VSUB)	−70V (Must always be most negative voltage)
IO Supply Voltage (VLL)	−0.3V to +3.6V
Voltage at High Voltage Analog Inputs	−70V to 70V
Voltage at Logic Inputs (SCLKI, SDI $\overline{SCSI}$, SW_OFF)	−0.3V to VLL+0.3v

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings

Operation Junction Temperature		0°C to + 70°C
VDD, −VSS, Analog Supply		+4.7V to 5.3V
VLL, Logic Supply		+2.4V to 3.5V
High Voltage Analog Inputs		−60V to +60V, VSUB must be most negative supply
VSUB, Substrate bias supply		−50V to −65V
Package Thermal Resistance (θ_{JA})		20°C/W
ESD Tolerance	Human Body Model(1)	2kV
	Machine Model	150V
	Charge Device Model	750V

(1) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

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Analog Characteristics

Unless otherwise stated, the following conditions apply.
VLL = +2.5V, VDD = −VSS = 5V, VSUB = −60V, R_{REF} = 50 kΩ, R_T = 50Ω, f_{IN} = 5 MHz, SW_OFF = SPI_EN = 0V, T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IN}	High Voltage Analog Inputs	VSUB must be most negative voltage. See (2)	-60		+60	V
e_n	Voltage Noise	at 5MHz		0.8		nV/√Hz
BW	-3dB Bandwidth			150		MHz
HD2	Second harmonic distortion	$0.1V_{PP}$ 5MHz tone applied as input		-60		dBc
HD3	Third harmonic distortion			-65		dBc
X_{TALK}	Channel crosstalk			-69		dB
T_{ON}	Turn-on time			2		µs
T_{OFF}	Turn-off time			0.2		µs
Iso_off	Off isolation	0.1Vpp 5MHz tone is applied as input		-55		dB
R_{ON}	On resistance of TR switch			125		Ω
I_L	Insertion Loss	f_{IN} = 5MHz		-5.5		dB
V_{CLAMP}	Output clamped voltage			±0.7		V
$I_{MISMATCH}$	Current source mis-match			0.03	0.2	mA
VDD, VSS	Power Supply Current			14	20	mA
VLL				5		µA
VSUB				0.45		mA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Total input signal levels, including any transient voltage overshoots, must be within this maximum voltage range.

Unless otherwise stated, the following conditions apply
VLL = +2.5V, VDD = −VSS = 5V, VSUB = −60V, R_{REF} = 25 kΩ, R_T = 50Ω, f_{IN} = 5MHz, SW_OFF = SPI_EN = 0V, T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IN}	High Voltage Analog Inputs	VSUB must be most negative voltage. See (2)	-60		+60	V
e_n	Voltage Noise	at 5MHz		0.7		nV/√Hz
BW	-3dB Bandwidth			150		MHz
HD2	Second harmonic distortion	$0.1V_{PP}$ 5MHz tone applied as input		-67		dBc
HD3	Third harmonic distortion			-70		dBc
X_{TALK}	Channel crosstalk			-73		dB
T_{ON}	Turn-on time			2		µs
T_{OFF}	Turn-off time			0.2		µs
Iso_off	Off isolation	0.1Vpp 5MHz tone is applied as input		-58		dB
R_{ON}	On resistance of TR switch			48		Ω
I_L	Insertion Loss	f_{IN} = 5MHz		-4		dB
V_{CLAMP}	Output clamped voltage			±0.75		V
$I_{MISMATCH}$	Current source mis-match			0.1	0.35	mA
VDD, VSS	Power Supply Current			23	30	mA
VLL				5		µA
VSUB				1		mA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Total input signal levels, including any transient voltage overshoots, must be within this maximum voltage range.

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Unless otherwise stated, the following conditions apply
VLL = +2.5V, VDD = −VSS = 5V, VSUB = −60V, R_{REF} = 12.5 kΩ, R_T = 50Ω, f_{IN} = 5MHz, SW_OFF = SPI_EN = 0V, T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IN}	High Voltage Analog Inputs	VSUB must be most negative voltage. See (2)	-60		+60	V
e_n	Voltage Noise	at 5MHz		0.55		nV/√Hz
BW	-3dB Bandwidth			180		MHz
HD2	Second harmonic distortion	0.1V_{PP} 5MHz tone applied as input		-73		dBc
HD3	Third harmonic distortion			-75		dBc
X_{TALK}	Channel crosstalk			-73		dB
T_{ON}	Turn-on time			2		µs
T_{OFF}	Turn-off time			0.2		µs
Iso_off	Off isolation	0.1Vpp 5MHz tone is applied as input		-58		dB
R_{ON}	On resistance of TR switch			27		Ω
I_L	Insertion Loss	f_{IN} = 5MHz		-3		dB
V_{CLAMP}	Output clamped voltage			±0.78		V
$I_{MISMATCH}$	Current source mis-match			0.25	0.6	mA
VDD, VSS	Power Supply Current			40	49	mA
VLL				5		µA
VSUB				2.2		mA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Total input signal levels, including any transient voltage overshoots, must be within this maximum voltage range.

Unless otherwise stated, the following conditions apply
VLL = +2.5V, VDD = −VSS = 5V, VSUB = −60V, R_{REF} = 6.25 kΩ, R_T = 50Ω, f_{IN} = 5MHz, SW_OFF = SPI_EN = 0V, T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IN}	High Voltage Analog Inputs	VSUB must be most negative voltage. See (2)	-60		+60	V
e_n	Voltage Noise	at 5MHz		0.5		nV/√Hz
BW	-3dB Bandwidth			180		MHz
HD2	Second harmonic distortion	0.1V_{PP} 5MHz tone applied to input		-75		dBc
HD3	Third harmonic distortion			-75		dBc
X_{TALK}	Channel crosstalk			-73		dB
T_{ON}	Turn-on time			2		µs
T_{OFF}	Turn-off time			0.2		µs
Iso_off	Off isolation	0.1Vpp 5MHz tone is applied as input		-58		dB
R_{ON}	On resistance of TR switch			18		Ω
I_L	Insertion Loss	f_{IN} = 5MHz		-2.5		dB
V_{CLAMP}	Output clamped voltage			±0.8		V
$I_{MISMATCH}$	Current source mis-match			0.6	1.2	mA
VDD, VSS	Power Supply Current			75	86	mA
VLL				5		µA
VSUB				5		mA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Total input signal levels, including any transient voltage overshoots, must be within this maximum voltage range.

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Digital Characteristics

Unless otherwise stated, the following conditions apply.

VLL = +2.5V, VDD = −VSS = 5V, VSUB = −60V, R_{REF} = 50 kΩ, R_T = 50Ω, SW_OFF = 0V, SPI_EN = 2.5V, T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logical Input “HI” Voltage		2			V
V_{IL}	Logical Input “LO” Voltage				0.5	V
$I_{IN-H/L}$	Logic Input Current		-1	0.2	+1	µA
V_{OH}	Logical Output “HI” Voltage		2.2			V
V_{OL}	Logical Output “LO” Voltage				0.3	V
t_{SSELS}	SPI™ SCSI Setup Time		11			ns
t_{SSELH}	SPI™ SCSI Hold Time		11			ns
t_{SSELHI}	SPI™ SCSI HI Time			250		ns
t_{WS}	SPI™ SDI Setup Time		11			ns
t_{WH}	SPI™ SDI Hold Time		11			ns
t_{OD}	SPI™ SCLKI to SDO Propagation Delay	C_L = 5 pF			25	ns
t_{VALID}	SPI™ SCSI to T/R Switch State Change Delay			30		ns
t_{SCLK}	SPI™ SCLKI Period		100			ns
	SPI™ SCLKI Duty Cycle	See (2)	45		55	% of CLK Period
$t_{SCLKOD-H}$	SPI™ SCLKI-HI to SCLKO-HI Propagation Delay				12	ns
$t_{SCLKOD-L}$	SPI™ SCLKI-LO to SCLKO-LO Propagation Delay				12	ns
$t_{SCSOD-H}$	SPI™ SCSI-HI to SCSO-HI Propagation Delay				12	ns
$t_{SCSOD-L}$	SPI™ SCLSI-LO to SCLSO-LO Propagation Delay				12	ns
	Maximum Number of Daisy-Chained devices	SCLKI Freq. = 10MHz		16		

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) Specified by design.

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SPI™ Timing

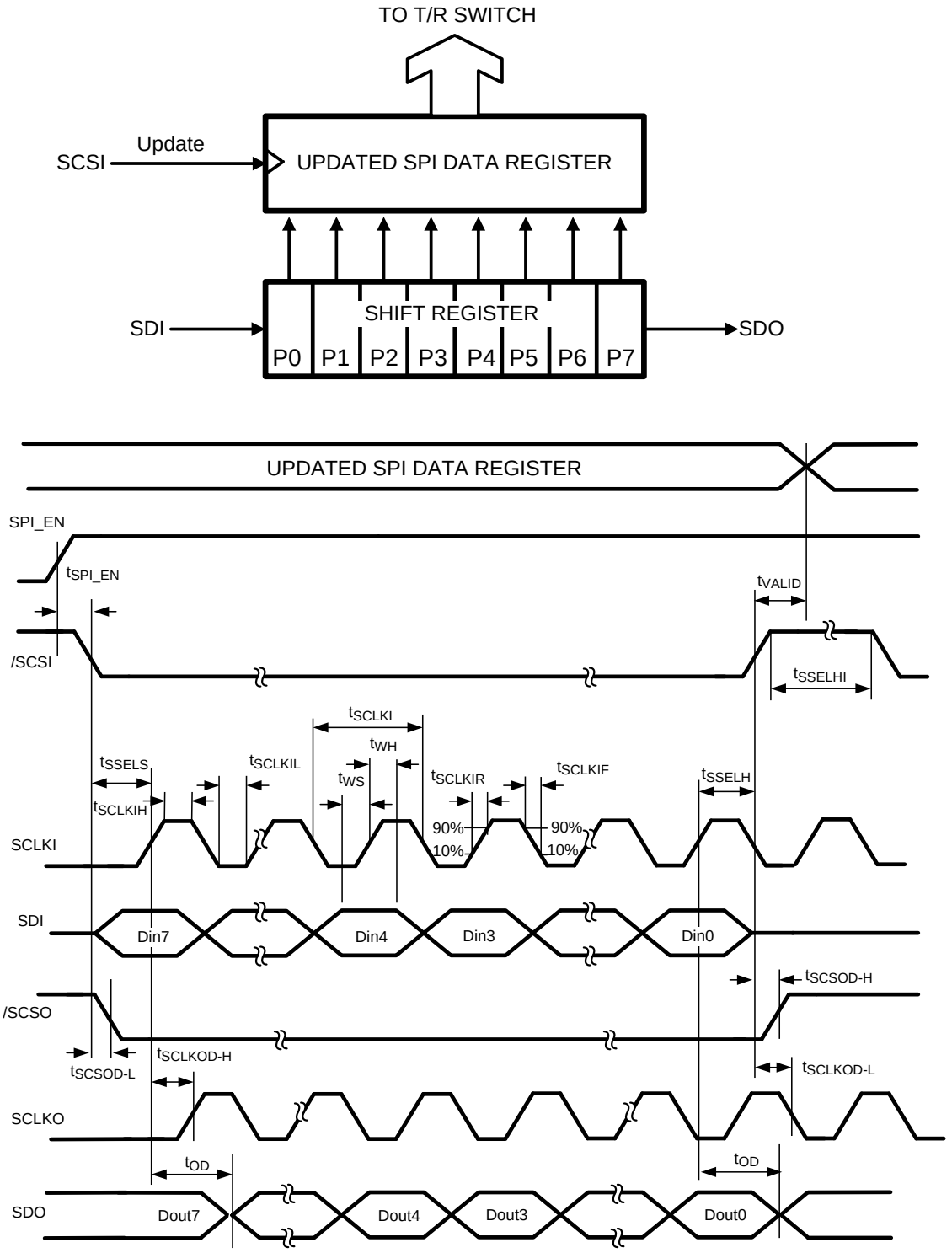

Figure 4. SPI™ Timing Diagram

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Typical Performance Characteristics

VLL = +2.5V, VDD = −VSS = 5V, VSUB = −60V, R_{REF} = 50 kΩ, R_T = 50Ω, f_{IN} = 5 MHz, T_A = 25°C.

Input Referred Noise vs Rref

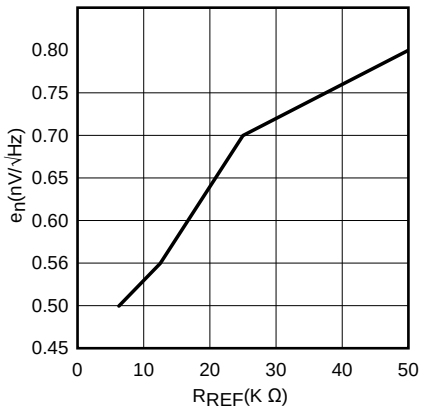

Figure 5.

2nd Harmonic Distortion vs Rref

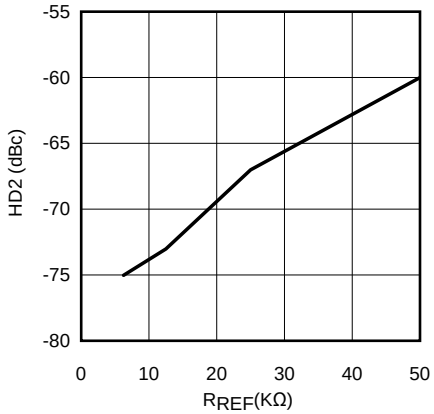

Figure 6.

Crosstalk vs frequency

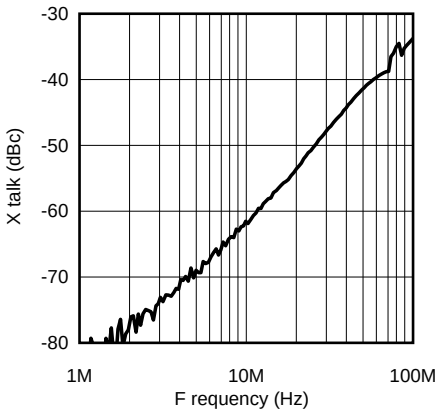

Figure 7.

Isolation vs Frequency

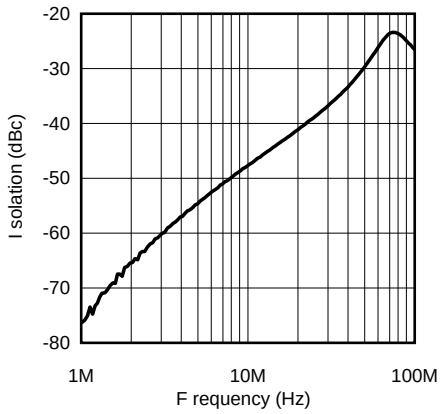

Figure 8.

Turn On Respone

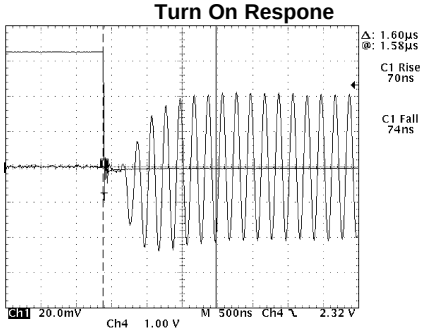

Figure 9.

Turn Off Response

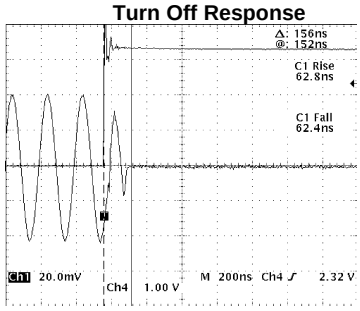

Figure 10.

FUNCTIONAL DESCRIPTION

The LM96530 RX switch provides an 8-channel receive side interface solution for medical ultrasound applications suitable for integration into multi-channel (128 / 256 channel) systems. Its diode-bridge-based architecture allows high-speed low-distortion channel designs targeting low-power, portable systems. A complete system can be designed using Texas Instruments' companion LM965XX chipset.

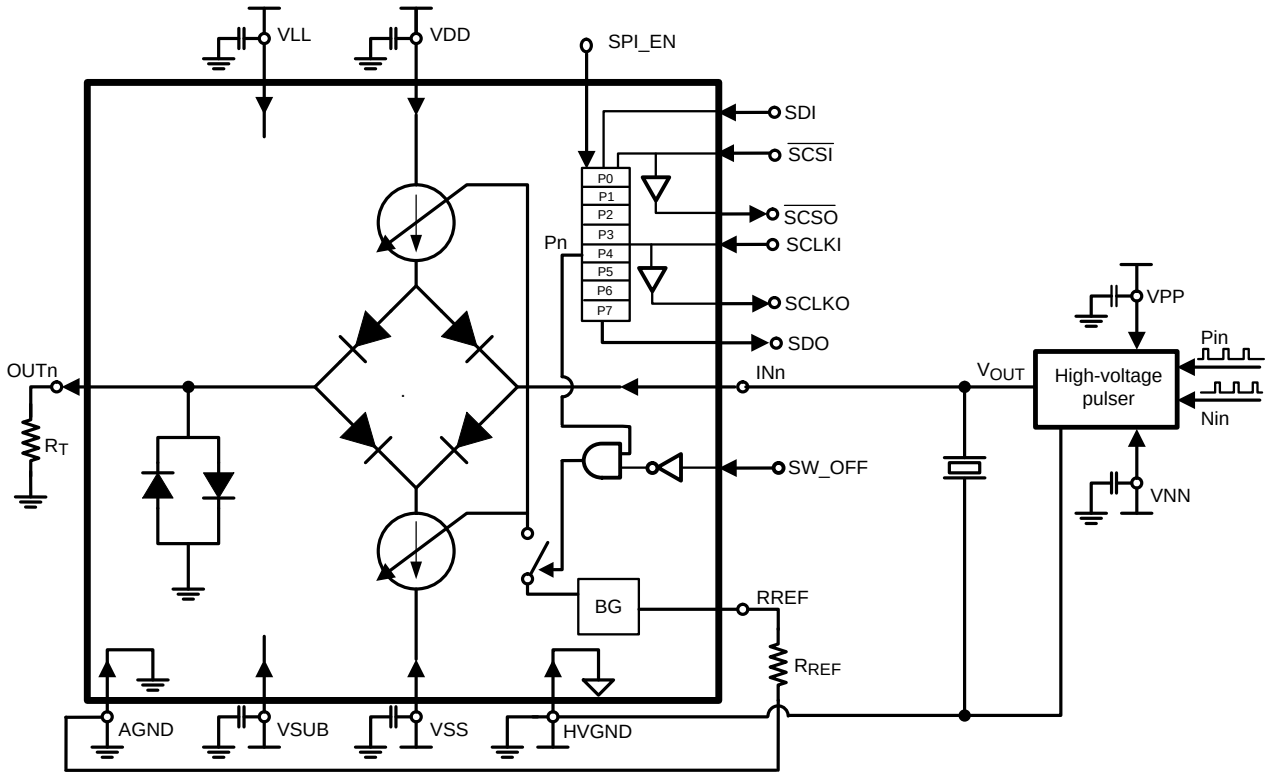

Figure 11. Block Diagram of T/R Channel

A functional block diagram of the IC is shown in Figure 11. Each RX switch channel on the IC has a high-voltage input that can be directly connected to a transducer driven by a high-voltage pulser, such as the LM96550. The input feeds into a diode bridge with its output being diode-clamped to ± 0.7V. The diode bridge bias current is set to 1 mA with Rref = 50KΩ. Therefore, the output can be directly connected to a low noise amplifier (LNA) stage which must be protected from the high-voltage signals on the transducer.

The bias current of the bridge is determined by two equally-sized current sources with their current value ranging between 0 and 8mA depending on the external resistor Rref at the input of the bandgap reference block. While the bias current is the same value for all channels on the IC, each channel can be switched on and off individually with an 8–bit shift register that is programmed via a SPI™ compatible bus.

The on-chip analog circuitry requires dual 5V supplies VDD and VSS, a single logic supply VLL, and a high voltage negative bias, VSUB.

SERIAL INTERFACE OPERATION

The digital interface is comprised of an 8-bit shift register and a latch. Each bit controls one T/R switch channel, where the MSB bit, i.e., the first bit written (D7) controls channel 7, and the LSB bit (D0) controls channel 0. The three input pins, SDI, SCSI and SCKI, are all Schmitt Trigger inputs with 0.5V typical hysteresis. The output pins SDO, SCSO, and SCLKO are SPI™ compatible. The serial data input SDI is synchronously read into the shift register on the rising edge of the clock SCKI. When SCSI changes from low to high, the data in the shift register is transferred to the latch circuit, and output on the parallel data signals P0 through P7 which drive the switched bias current sources for channels n=0,…, 7, respectively. When SCSI changes from high to low, the latch output Pn, and thus the biasing condition, does not change.

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DAISY CHAINING MULTIPLE LM96530 ICs

For connecting multiple T/R switch ICs, the LM965XX SPI™-compatible bus can be daisy-chained up to 16 ICs at 10MHz SCLKI for easy PCB routing. The inputs SDI, SCSI and SCLKI are daisy-chained together with SDO, SCSO and SCLKO. Therefore, the next IC's SDI is connected to the previous IC's SDO. Similarly, the next IC's SCSI is connected to the previous IC's SCSO, and the next IC's SCLKI is connected to the previous IC's SCLKO, as shown in Figure 12. Daisy-chaining multiple LM96530 devices amounts to one large shift register with the number of bits being equal to 8 times the number of LM96530 ICs. For example, if 3 LM96530 ICs are daisy-chained, one can picture a 24–bit shift register. Thus, the MSB or first bit written on the SDI line (D23) will control channel 7 of the last LM96530, i.e., the IC that is daisy-chained the farthest away from the SPI master. The LSB or last bit written on the SDI line (D0) will control channel 0 of the first LM96530, i.e., the IC that is closest to the SPI master. It is important to note that If only one particular channel of an IC in the daisy-chain requires updating, all of the ICs, i.e., the entire shift register, must be written to.

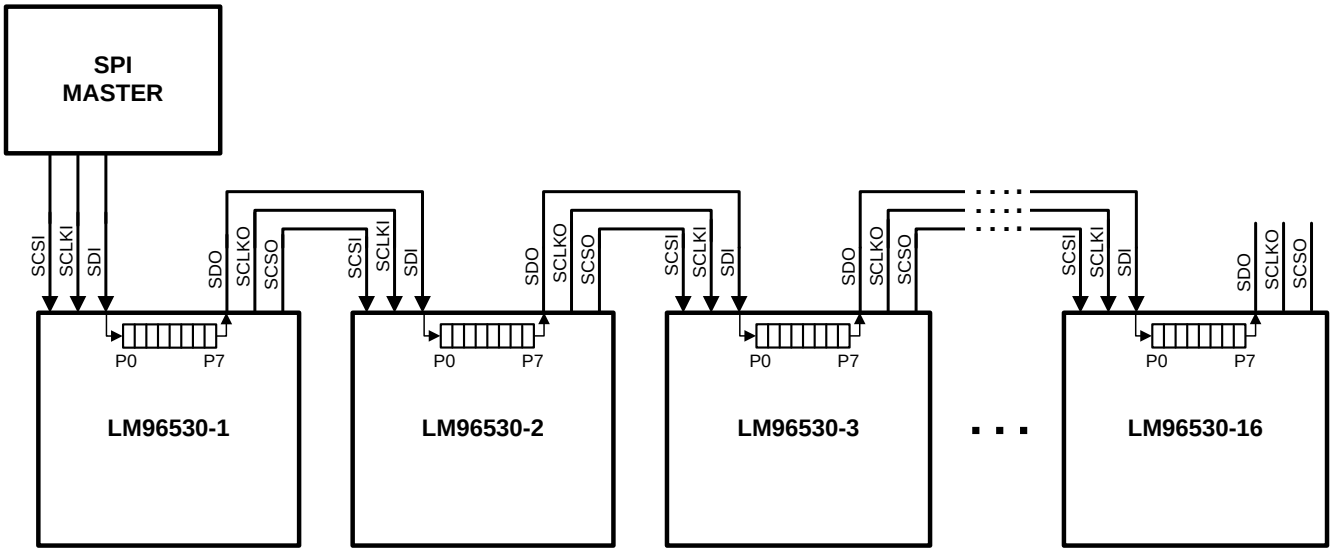

Figure 12. 16 LM96530 Devices Daisy Chained at SCLKI = 16MHz

BASIC OPERATION WITHOUT SERIAL INTERFACE COMMUNICATION

To disable the SPI™ compatible interface, connect the pin SPI_EN to AGND. To reverse bias all 8 channels of the T/R switch, connect the pin, SW_OFF to VLL. To forward bias all 8 channels of the T/R switch, connect the pin, SW_OFF to AGND.

POWER-UP AND POWER-DOWN SEQUENCES

VSUB needs to always be the most negative supply – equal to or more negative than VSS or the most negative transmit pulse at all times. **The power sequence should be to applied to VSUB first, followed by the remaining supplies in any order.**

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REVISION HISTORY

Changes from Revision E (May 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM96530SQ/NOPB	OBSOLETE	WQFN	NKA	60		TBD	Call TI	Call TI	0 to 70	LM96530SQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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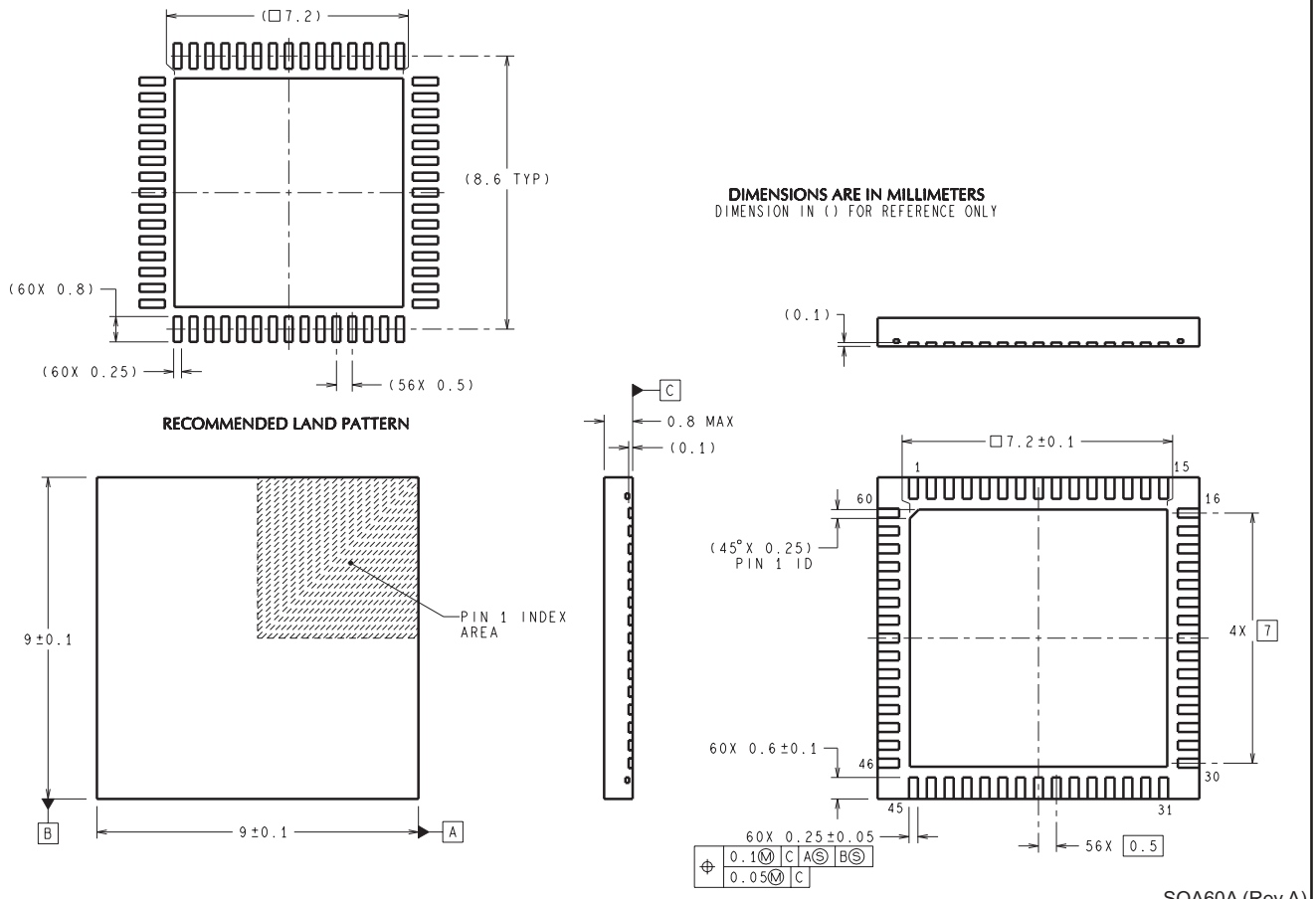

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