19-0627; Rev 0; 9/06

EVALUATION KIT AVAILABLE

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

General Description

The MAX9726 stereo, DirectDrive™, headphone amplifier with BassMax and volume control is ideal for portable audio applications where space is at a premium and performance is essential. The MAX9726 operates from a single 2.7V to 5.5V power supply and includes features that reduce external component count, system cost, board space, and offer improved audio reproduction. High 85dB PSRR makes the MAX9726 ideal for direct connection to a battery-powered supply and eliminates the need for a dedicated LDO. The MAX9726 features Maxim's industry-leading click-and-pop suppression circuitry, which reduces/eliminates audible transients during power-up and power-down.

The headphone amplifier uses Maxim's patented† DirectDrive architecture that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors. The headphone amplifiers deliver 105mW into a 32Ω load and feature low 0.02% THD+N.

The BassMax feature boosts the bass response of the amplifier, improving audio reproduction when using inexpensive headphones. The integrated volume control features 64 discrete volume levels, eliminating the need for an external potentiometer. External resistors set the MAX9726's overall gain allowing for custom gain settings.

BassMax and the volume control are enabled through the I²C/SMBus™-compatible interface. Shutdown can be controlled through the hardware or software interface.

The MAX9726 consumes only 5.5mA of supply current, provides short-circuit and thermal-overload protection, and is specified over the -40°C to +85°C extended temperature range. The MAX9726 is available in a tiny (2mm x 2.5mm x 0.62mm) 20-bump chip-scale package (UCSP™) and a 20-pin TQFN package (4mm x 4mm x 0.75mm).

Applications

Cell Phones

MP3/PMP Players

Flat-Panel TVs

Automotive Rear-Seat Entertainment (RSE)

Portable CD/DVD/MD Players

†*U.S. Patent # 7,061,327*

SMBus is a trademark of Intel Corp.

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- **105mW DirectDrive Headphone Amplifier Eliminates Bulky DC-Blocking Capacitors**
- **2.7V to 5.5V Single-Supply Operation**
- **Integrated 64-Level Volume Control**
- **High 85dB PSRR at 1kHz**
- **Software-Enabled Bass Boost (BassMax)**
- **Industry-Leading Click-and-Pop Suppression**
- **±7.5kV HBM ESD-Protected Headphone Outputs**
- **Short-Circuit and Thermal-Overload Protection**
- **Low-Power Shutdown Mode (8µA)**
- **Low 0.02% THD+N**
- **I²C/SMBus-Compatible Interface**
- **Available in Space-Saving, Thermally Efficient Packages**
  - **20-Bump UCSP (2mm x 2.5mm x 0.62mm)**
  - **20-Pin TQFN (4mm x 4mm x 0.75mm)**

Ordering Information

PART	PIN-PACKAGE	SLAVE ADDRESS	PKG CODE
MAX9726AEBP+T*	20 UCSP-20	1001100	B20-1
MAX9726AETP+	20 TQFN-EP**	1001100	T2044-3
MAX9726BEBP+T*	20 UCSP-20	1001101	B20-1
MAX9726BETP+	20 TQFN-EP**	1001101	T2044-3

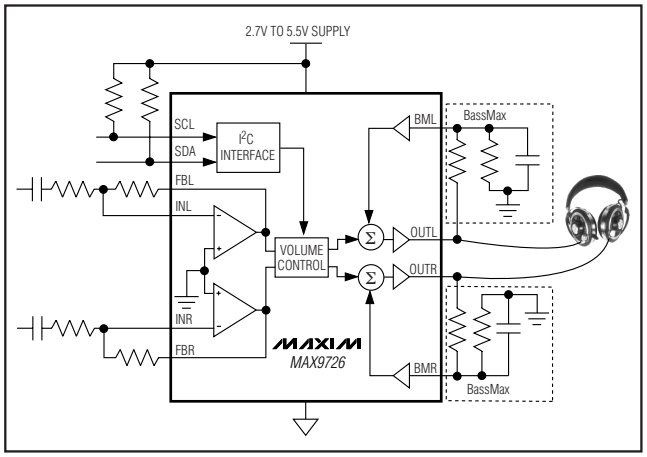
Note: *All devices specified over the -40°C to +85°C operating range.*

+Denotes lead-free package.

**Future product—contact factory for availability.*

***EP = Exposed pad.*

Simplified Block Diagram



Pin Configurations appear at end of data sheet.

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

ABSOLUTE MAXIMUM RATINGS

V_{DD} to PGND .....-0.3V to +6V
PV_{SS} to SV_{SS} .....-0.3V to +0.3V
SGND to PGND .....-0.3V to +0.3V
C1P to PGND.....-0.3V to (V_{DD} + 0.3V)
C1N to PGND.....(PV_{SS} - 0.3V) to +0.3V
PV_{SS}, SV_{SS} to PGND .....+0.3V to -6V
IN_ to SGND.....(SV_{SS} - 0.3V) to (V_{DD} + 0.3V)
FB_ to SGND.....(SV_{SS} - 0.3V) to (V_{DD} + 0.3V)
SDA, SCL to PGND .....-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$ to PGND .....-0.3V to (V_{DD} + 0.3V)
OUT_ to SGND .....-3V to +3V
BM_ to SGND .....-3V to +3V
Duration of OUT_ Short Circuit to PGND.....Continuous

Continuous Current Into/Out of:
V_{DD}, C1P, PGND, C1N, PV_{SS}, SV_{SS}, or OUT_ .....±850mA
Any Other Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C, multilayer board)
20-Bump UCSP (derate 10mW/°C above +70°C) 800mW
20-Pin TQFN (derate 25.6mW/°C above +70°C) 2051mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
OUTL and OUTR ESD Protection (Human Body Model)....±7.5kV
Bump Temperature (soldering) Reflow.....+230°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (5V Supply)

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Quiescent Supply Current	I_{DD}	No load		5.5	10	mA
Shutdown Supply Current	I_{DD_SHDN}	$\overline{SHDN}$ = 0V		8	15	µA
Turn-On Time	t_{ON}			440		µs
Turn-Off Time	t_{OFF}			1		µs
Thermal-Shutdown Threshold	T_{THRES}			+150		°C
Thermal-Shutdown Hysteresis	T_{HYST}			12		°C
HEADPHONE AMPLIFIER						
Output Offset Voltage	V_{OSHP}	Measured between OUT_ and SGND, gain = 0dB, R_{IN} = R_F = 10kΩ, T_A = +25°C (Note 2)		±0.6	10	mV
Input Offset Voltage of Input Amplifier	V_{OS}	Referenced to SGND, measured between FBR, FBL, and SGND		3		mV
Input Bias Current	I_B			±20	±100	nA
BMR, BML Input Bias Current	I_{BIAS_BB}			±20	±100	nA
Power-Supply Rejection Ratio (Note 2)	PSRR	DC, V_{DD} = 2.7V to 5.5V	80	97		dB
		f = 1kHz, 100mV_{P-P} ripple		85		
		f = 20kHz, 100mV_{P-P} ripple		74		
Output Power	P_{OUT}	THD+N = 1%, f_{IN} = 1kHz, R_L = 16Ω		124		mW
		THD+N = 1%, f_{IN} = 1kHz, R_L = 32Ω		104		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω, P_{OUT} = 15mW, f_{IN} = 1kHz		0.04		%
		R_L = 32Ω, P_{OUT} = 30mW, f_{IN} = 1kHz		0.02		

ELECTRICAL CHARACTERISTICS (5V Supply) (continued)

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	R_L = 32Ω, V_{OUT} = 1.77V_{RMS}	BW = 22Hz to 22kHz		102		dB
			A-weighted		105		
Slew Rate	SR				1		V/µs
Capacitive Drive		No sustained oscillations			200		pF
Output Resistance in Shutdown	R_{OUT_SHDN}	$V_{\overline{SHDN}}$ = 0V, measured from OUT_ to SGND			50		kΩ
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second (Notes 2, 4)	Into shutdown		59		dBV
			Out of shutdown		61		
Charge-Pump Switching Frequency	f_{CP}			515	610	705	kHz
Crosstalk		L to R, or R to L, f = 10kHz, V_{OUT} = 1V_{P-P}, R_L = 32Ω, both channels loaded			85		dB
VOLUME CONTROL							
Attenuator Step Accuracy		0 to 64dB			±0.1		dB
		68dB to 96dB			±0.5		
		100dB to 120dB			±2		
DIGITAL INPUTS ($\overline{SHDN}$, SDA, SCL)							
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Low Voltage	V_{IL}					0.3 x V_{DD}	V
Input Leakage Current						±1	µA
DIGITAL OUTPUTS (SDA)							
Output Low Voltage	V_{OL}	I_{OL} = 3mA				0.06	V
Output High Current	I_{OH}	V_{SDA} = V_{DD}				1	µA

ELECTRICAL CHARACTERISTICS (3.3V Supply)

(V_{DD} = $\overline{SHDN}$ = 3.3V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power	P_{OUT}	THD+N = 1%, f_{IN} = 1kHz	R_L = 16Ω		80		mW
			R_L = 32Ω		70		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω, P_{OUT} = 15mW, f_{IN} = 1kHz			0.05		%
		R_L = 32Ω, P_{OUT} = 30mW, f_{IN} = 1kHz			0.03		

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

ELECTRICAL CHARACTERISTICS (3.3V Supply) (continued)

(V_{DD} = $\overline{SHDN}$ = 3.3V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 2)	PSRR	f = 1kHz, 100mV$_{P-P}$ ripple			85		dB
		f = 20kHz, 100mV$_{P-P}$ ripple			73		
Signal-to-Noise Ratio	SNR	R_L = 32Ω, V_{OUT} = 1.5V_{RMS}	BW = 22Hz to 22kHz		101		dB
			A-weighted		104		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second (Notes 2, 4)	Into shutdown		62		dBV
			Out of shutdown		67		

TIMING CHARACTERISTICS

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time Repeated for a START Condition	$t_{HD:STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_r				300	ns
Fall Time of Both SDA and SCL Signals	t_f				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}			50		ns
Capacitive Load for Each Bus Line	C_{L_BUS}				400	pF

Note 1: All specifications are 100% tested at T_A = +25°C. Temperature limits are guaranteed by design.

Note 2: Inputs AC-coupled to SGND.

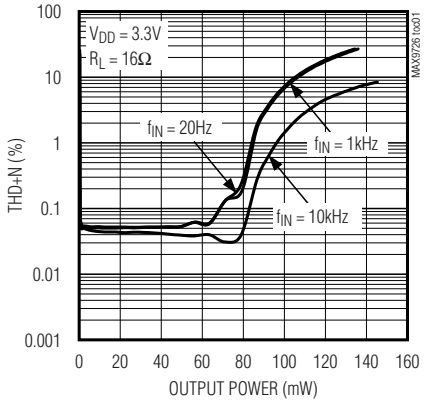
Note 3: Guaranteed by design.

Note 4: Headphone testing performed with a 32Ω resistive load connected to PGND. Mode transitions are controlled by $\overline{SHDN}$. K_{CP} level is calculated as 20log[(peak voltage during mode transition, no input signal)/1V_{RMS}]. Units are expressed in dBV.

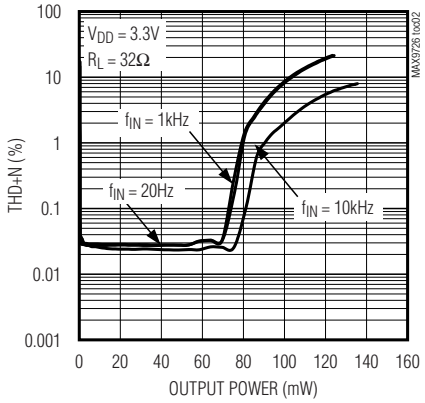
Typical Operating Characteristics

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. Outputs in phase, both channels loaded. T_A = +25°C, unless otherwise noted.) (See the *Functional Diagram/Typical Operating Circuit*)

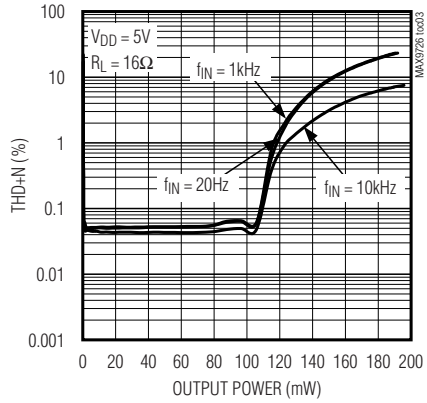
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



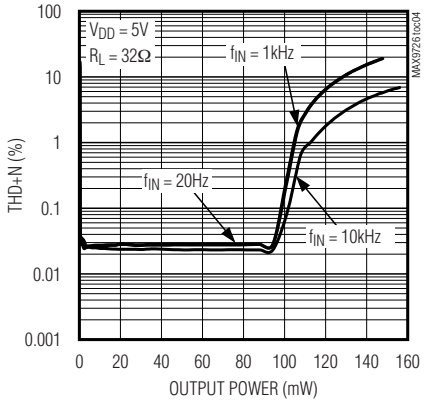
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



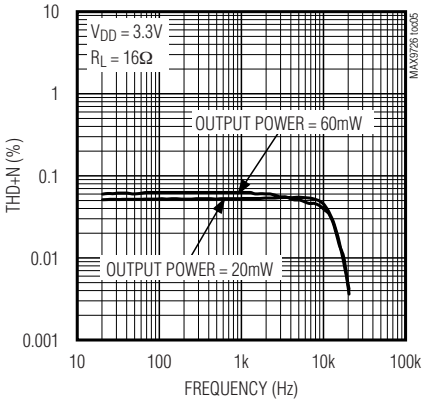
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



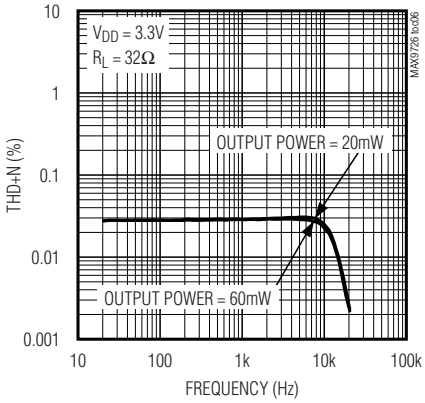
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



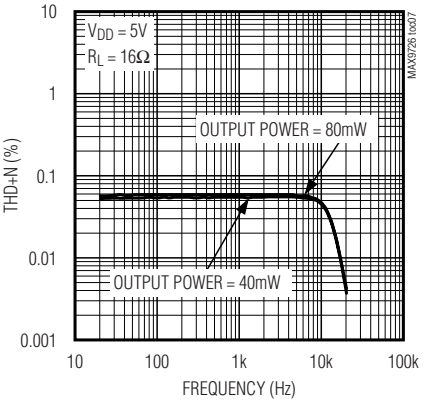
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

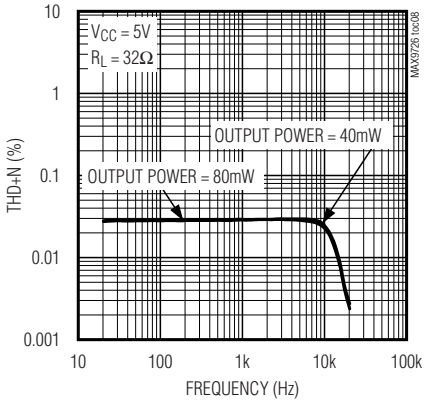


DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

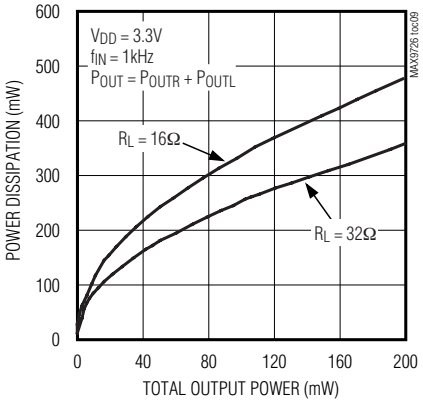
Typical Operating Characteristics (continued)

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. Outputs in phase, both channels loaded. T_A = +25°C, unless otherwise noted.) (See the *Functional Diagram/Typical Operating Circuit*)

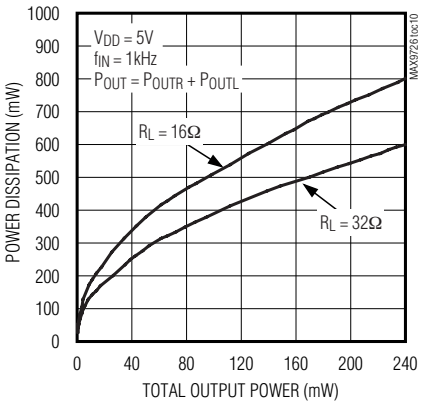
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



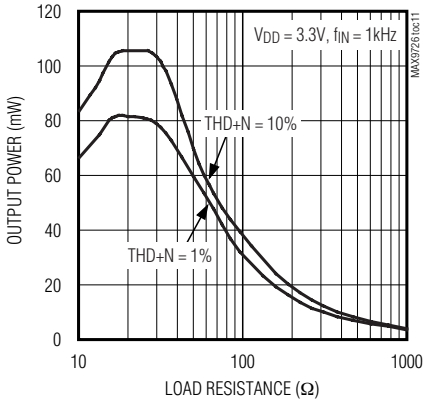
POWER DISSIPATION vs. OUTPUT POWER



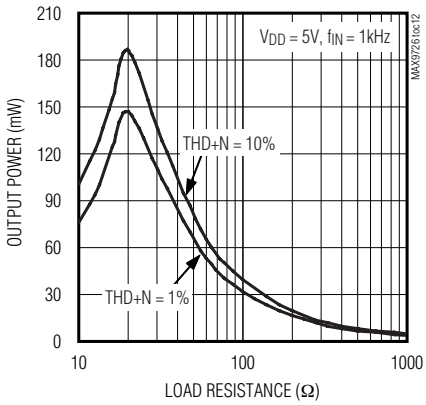
POWER DISSIPATION vs. OUTPUT POWER



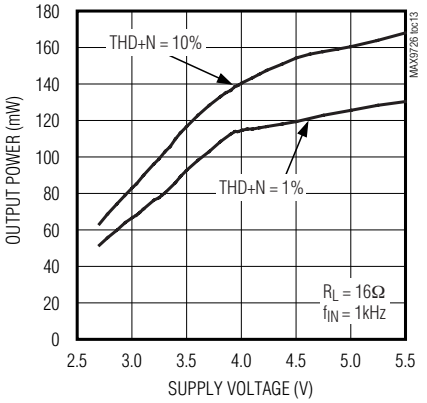
OUTPUT POWER vs. LOAD RESISTANCE



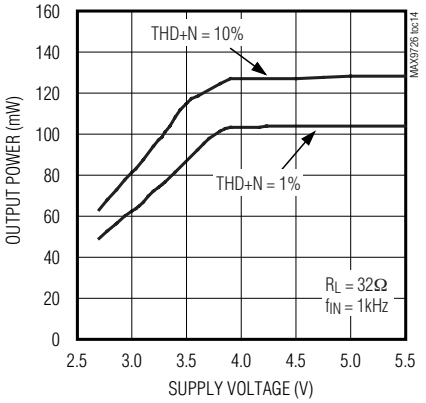
OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. SUPPLY VOLTAGE



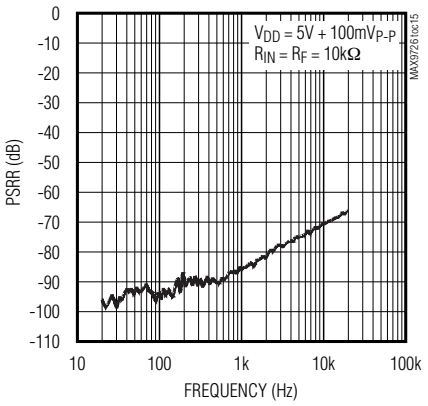
OUTPUT POWER vs. SUPPLY VOLTAGE



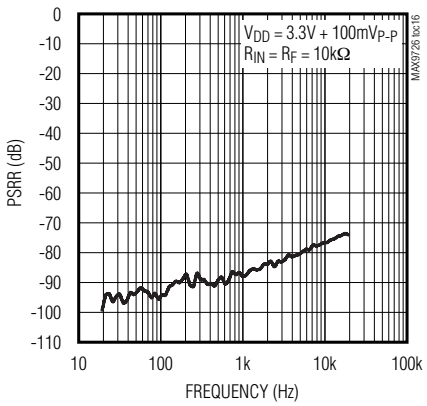
Typical Operating Characteristics (continued)

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. Outputs in phase, both channels loaded. T_A = +25°C, unless otherwise noted.) (See the *Functional Diagram/Typical Operating Circuit*)

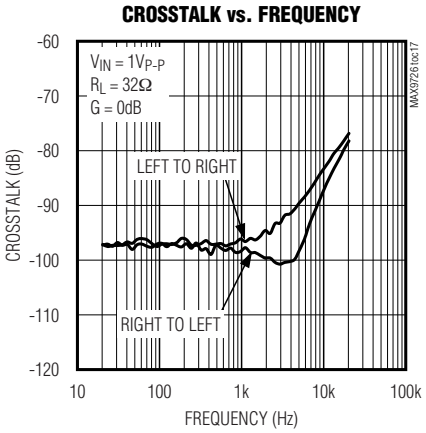
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



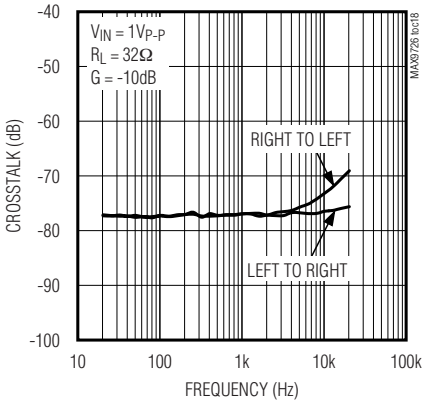
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



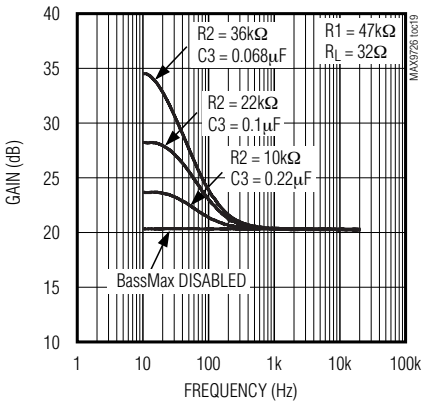
CROSSTALK vs. FREQUENCY



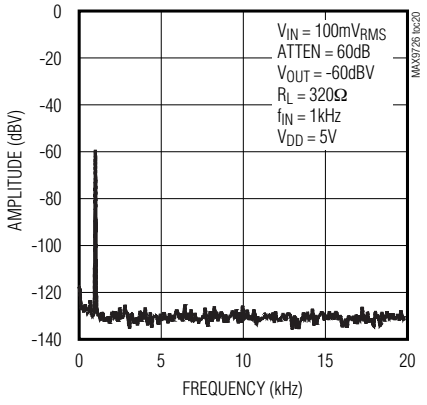
CROSSTALK vs. FREQUENCY



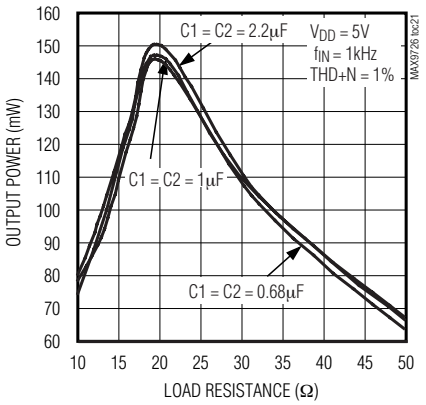
BassMax FREQUENCY RESPONSE



OUTPUT FFT



OUTPUT POWER vs. CHARGE-PUMP CAPACITANCE AND LOAD RESISTANCE

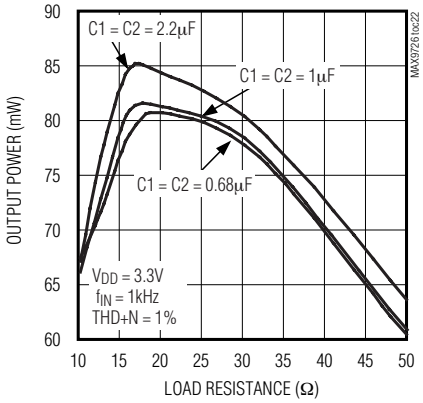


DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

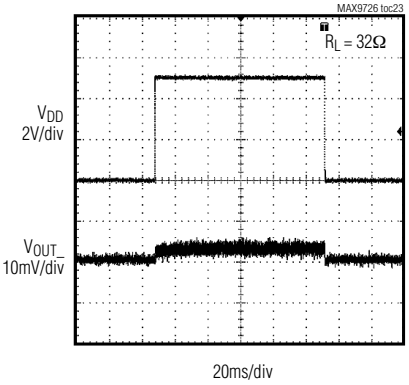
Typical Operating Characteristics (continued)

(V_{DD} = $\overline{SHDN}$ = 5V, PGND = SGND = 0V, C1 = C2 = 1µF, C_{PREG} = C_{NREG} = 1µF, BM_ = 0V, R_{IN} = 10kΩ, R_F = 10kΩ, maximum volume (overall gain = 0dB), BassMax disabled. Load connected between OUT_ and PGND where specified. Outputs in phase, both channels loaded. T_A = +25°C, unless otherwise noted.) (See the *Functional Diagram/Typical Operating Circuit*)

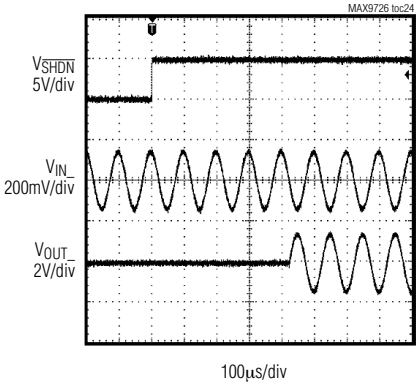
OUTPUT POWER vs. CHARGE-PUMP CAPACITANCE AND LOAD RESISTANCE



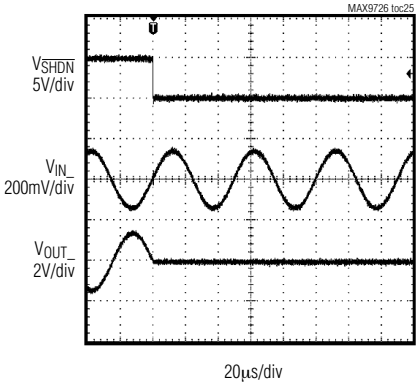
POWER-UP/POWER-DOWN



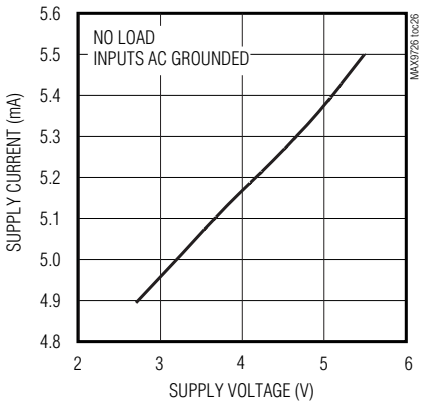
EXITING SHUTDOWN



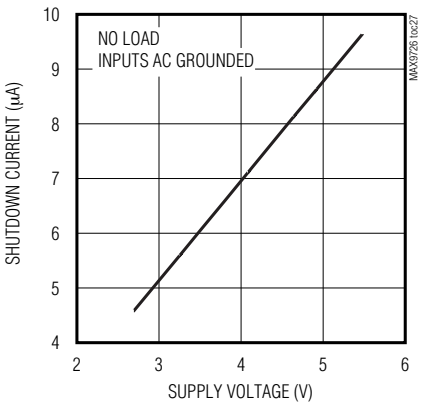
ENTERING SHUTDOWN



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN	BUMP	NAME	FUNCTION
TQFN	UCSP		
1	A1	V_{DD}	Power-Supply Input. Bypass V_{DD} to PGND with a 1µF capacitor.
2	A2	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF capacitor between C1P and C1N.
3	A3	PGND	Power Ground. Connect to SGND.
4	A4	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF capacitor between C1P and C1N.
5	A5	PV_{SS}	Charge-Pump Output. Connect to SV_{SS} and bypass with a 1µF capacitor to PGND.
6	B3	SDA	Serial Data Input. Connect a pullup resistor greater than 500Ω from SDA to V_{DD}.
7	C3	SCL	Serial Clock Input. Connect a pullup resistor greater than 500Ω from SCL to V_{DD}.
8	C2	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ low to disable the MAX9726. Connect $\overline{SHDN}$ to V_{DD} while bit 7 is high for normal operation (see the *Command Register* section).
9	B4	FBL	Left-Channel Feedback Output. Connect a feedback resistor between FBL and INL. See the *Gain-Setting Components* section.
10	B5	INL	Left-Channel Input. Connect an input resistor to INL. See the *Gain-Setting Components* section.
11	C5	INR	Right-Channel Input. Connect an input resistor to INR. See the *Gain-Setting Components* section.
12	C4	FBR	Right-Channel Feedback Output. Connect a feedback resistor between FBR and INR. See the *Gain-Setting Components* section.
13	D5	SGND	Signal Ground. Connect to PGND.
14	D2	NREG	Negative Supply Regulator Voltage. Bypass NREG to PGND with a 1µF capacitor.
15	D4	BMR	Right BassMax Input. Connect an external passive network between OUTR and BMR to apply bass boost to the right-channel output. See the *Gain-Setting Components* section. Connect BMR to SGND if BassMax is not used.
16	D1	SV_{SS}	Headphone Amplifier Negative Power-Supply Input. Connect to PV_{SS} and bypass with a 1µF capacitor to PGND.
17	C1	OUTR	Right Headphone Output
18	B1	OUTL	Left Headphone Output
19	D3	BML	Left BassMax Input. Connect an external passive network between OUTL and BML to apply bass boost to the right-channel output. See the *Gain-Setting Components* section. Connect BML to SGND if BassMax is not used.
20	B2	PREG	Positive Supply Regulator Voltage. Bypass PREG to PGND with a 1µF capacitor.
EP	—	EP	Exposed Pad. **Connect EP to SV_{SS} or leave unconnected.**

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Detailed Description

The MAX9726 stereo headphone amplifier features Maxim's patented DirectDrive architecture, eliminating the large output-coupling capacitors required by conventional single-supply headphone amplifiers. The MAX9726 consists of two 105mW Class AB headphone amplifiers, two adjustable gain preamplifiers, hardware/software shutdown control, inverting charge pump, integrated 64-level volume control, BassMax feature, comprehensive click-and-pop suppression circuitry, and an I²C-/SMBus-compatible interface (see the *Functional Diagram/Typical Operating Circuit*). A negative power supply (PV_{SS}) is created internally by inverting the positive supply (V_{DD}). Powering the amplifiers from V_{DD} and PV_{SS} increases the dynamic range of the amplifiers to almost twice that of other single-supply amplifiers, increasing the total available output power. High PSRR topologies eliminate the need for an external voltage regulator.

An I²C-/SMBus-compatible interface allows serial communication between the MAX9726 and a microcontroller. The internal command register controls the shutdown status of the MAX9726, enables the BassMax circuitry, and sets the volume level (see the *Volume Control* section). The MAX9726's BassMax circuitry improves audio reproduction by boosting the bass response of the amplifier, compensating for any low-frequency attenuation introduced by the headphone. External components set the MAX9726's overall gain allowing for custom gain settings (see the *Gain-Setting Components* section). Amplifier volume is digitally programmable to any one of 64 levels.

DirectDrive

Traditional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage, typically half the supply, for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and headphone amplifier. In addition to the cost and size disadvantages, the DC-blocking capacitors required by conventional headphone amplifiers limit low-frequency response and can distort the audio signal.

Maxim's patented DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the MAX9726 headphone amplifier outputs to be biased about ground, almost doubling the dynamic range while operating from a single supply (see Figure 1). With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (up to 220µF) tantalum capacitors, the MAX9726 charge pump requires only two small 1µF ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graphs in the *Typical Operating Characteristics* for details of the possible capacitor sizes.

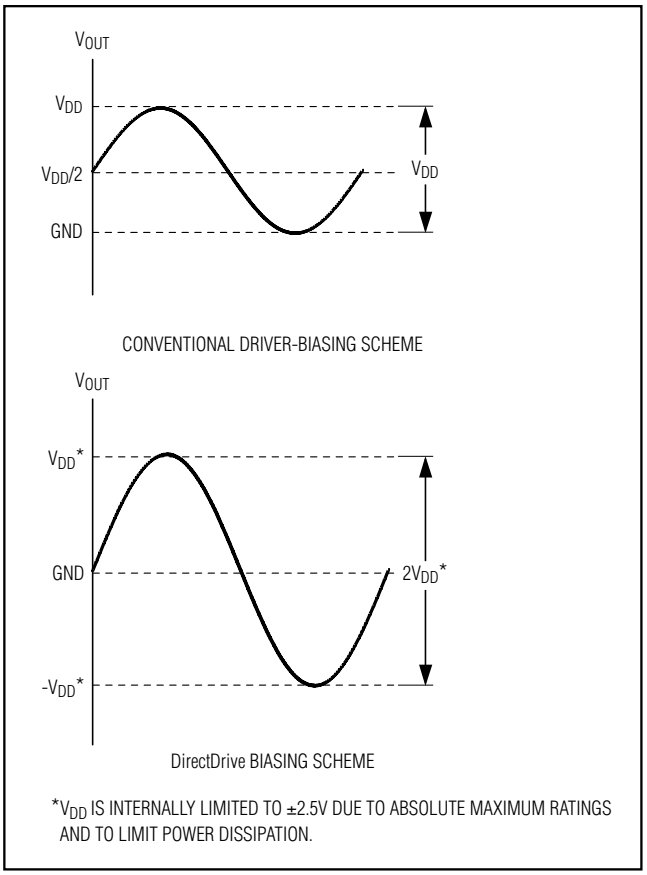


Figure 1. Traditional Amplifier Output vs. MAX9726 DirectDrive Output

Charge Pump

The MAX9726 features a low-noise charge pump. The 610kHz switching frequency is well beyond the audio range, and does not interfere with the audio signals. This enables the MAX9726 to achieve an SNR of 102dB. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Limiting the switching speed of the charge pump also minimizes di/dt noise caused by the parasitic bond wire and trace inductance.

Click-and-Pop Suppression

In conventional single-supply headphone amplifiers, the output coupling capacitor is a major contributor of audible clicks and pops. The amplifier charges the coupling capacitor to its output bias voltage at startup. During shutdown, the capacitor is discharged. This charging and discharging results in a DC shift across the capacitor, which appears as an audible transient at the headphone speaker. Since the MAX9726 headphone amplifier does not require output-coupling capacitors, no audible transients occur.

Additionally, the MAX9726 features extensive click-and-pop suppression that eliminates any audible transient sources internal to the device. The Power-Up/Power-Down graph in the *Typical Operating Characteristics* shows that there are minimal transients at the output upon startup or shutdown.

In most applications, the preamplifier driving the MAX9726 has a DC bias of typically half the supply. The input-coupling capacitor is charged to the preamplifier's bias voltage through the MAX9726's input resistor (R_{IN}) during startup. The resulting voltage shift across the capacitor creates an audible click-and-pop. Delay the rise of $\overline{SHDN}$ by at least four time constants ($4 \times R_{IN} \times C_{IN}$) relative to the start of the preamplifier to avoid clicks/pops caused by the input filter.

Shutdown

The MAX9726 features a 8µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. Shutdown is controlled by a hardware and software interface. Driving the $\overline{SHDN}$ input low disables the drive amplifiers, bias circuitry, charge pump, and sets the headphone amplifier output resistance to 50kΩ. Similarly, the MAX9726 enters shutdown when bit seven (B7) in the control register is set to 0 (see the *Command Register* section). $\overline{SHDN}$ and B7 must be high to enable the MAX9726. The I²C/SMBus interface is active and the contents of the command register are not affected when in shutdown. This allows the master to write to the MAX9726 while in shutdown.

BassMax (Bass Boost)

Typical headphones do not have a flat-frequency response. The small physical size of the diaphragm does not allow the headphone speaker to efficiently reproduce low frequencies. This physical limitation results in attenuated bass response. The MAX9726 includes a bass-boost feature that compensates for the headphone's poor bass response by increasing the amplifier gain at low frequencies.

The DirectDrive output of the MAX9726 has more headroom than typical single-supply headphone amplifiers. This additional headroom allows boosting the bass frequencies without the output signal clipping.

Program the BassMax gain and cutoff frequency with external components connected between OUT_ and BM_ (see the *Gain-Setting Components* section and the *Functional Diagram/Typical Operating Circuit*). Use the I²C-compatible interface to program the command register to enable/disable the BassMax circuit.

BM_ is connected to the noninverting input of the output amplifier when BassMax is enabled. BM_ is pulled to SGND when BassMax is disabled. The typical application of the BassMax circuit involves feeding a low-pass version of the output signal back to the amplifier. This is realized using positive feedback from OUT_ to BM_. Figure 2 shows the connections needed to implement BassMax.

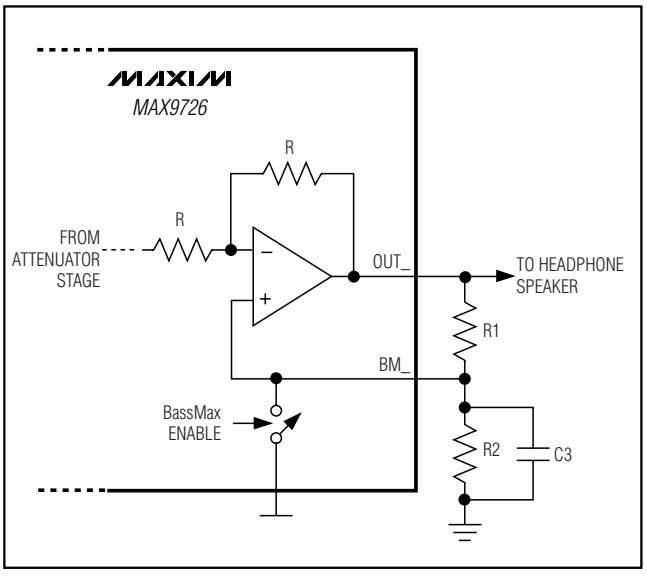


Figure 2. BassMax External Connections

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Volume Control

The MAX9726 includes a 64-level volume control that adjusts the gain of the output amplifiers according to the code contained in the command register. Volume is programmed through the command register bits [5:0]. Table 5 shows all possible attenuation settings of the MAX9726 with respect to the overall gain set by the external gain-setting resistors (R_{IN} and R_F). Mute attenuation is typically better than 120dB when driving a 32Ω load. To perform smooth-sounding volume changes, step through all intermediate volume settings at a rate of approximately 2ms per step when a volume change occurs.

Serial Interface

The MAX9726 features an I²C-/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9726 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX9726 is a receive-only slave device relying on the master to generate the SCL signal. The MAX9726 cannot write to the SDA bus except to acknowledge the receipt of data from the master. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus.

A master device communicates to the MAX9726 by transmitting the slave address with the read/$\overline{\text{write}}$ (R/$\overline{\text{W}}$) bit followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9726 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9726 SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9726 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

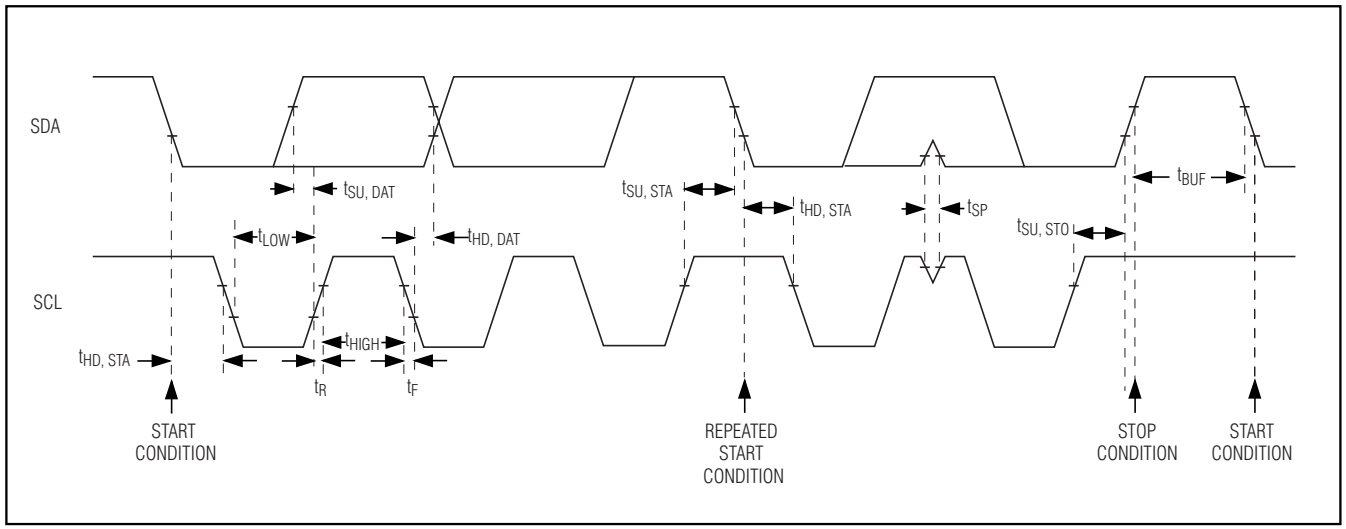


Figure 3. 2-Wire Serial-Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse since changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 5). A START condition from the master signals the beginning of a transmission to the MAX9726. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9726 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) of the serial data transmission. The first byte of information sent to the MAX9726 after the START condition must contain the slave address and R/$\overline{W}$ bit (see Table 1). The MAX9726 is a slave device only capable of being written to. The sent R/$\overline{W}$ bit must always be set to zero when configuring the MAX9726.

The MAX9726 acknowledges the receipt of its address even if R/$\overline{W}$ is set to 1. However, the MAX9726 does not drive SDA. Addressing the MAX9726 with R/$\overline{W}$ set to 1 causes the master to receive all ones regardless of the contents of the command register.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9726 uses to handshake receipt each byte of data (see Figure 6). The MAX9726 pulls down SDA during the master generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may reattempt communication.

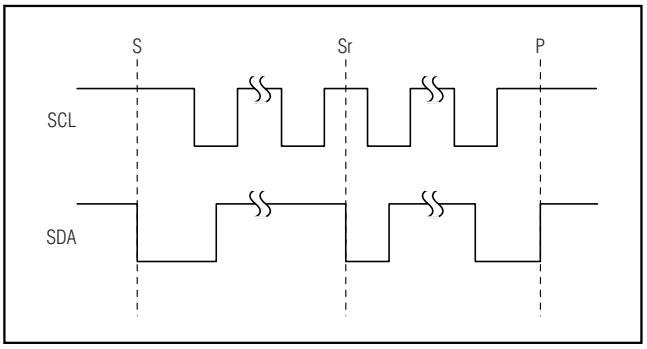


Figure 4. START, STOP, and REPEATED START Conditions

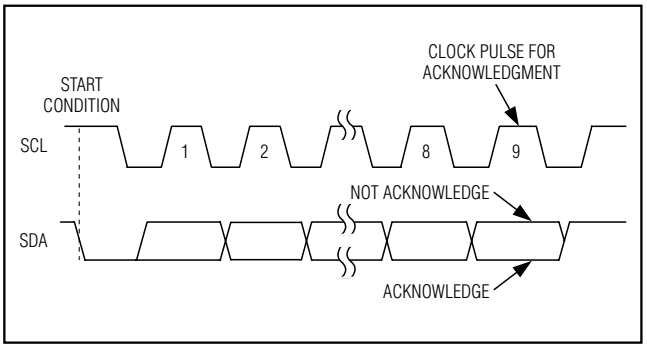


Figure 5. Acknowledge Bit

Table 1. MAX9726 Slave Address with Read/$\overline{\text{Write}}$ Bit

PART	A6 (MSB)	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
MAX9726A	1	0	0	1	1	0	0	0
MAX9726B	1	0	0	1	1	0	1	0

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

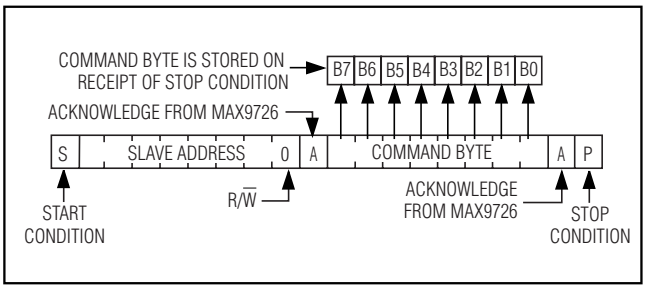


Figure 6. Write Data Format Example

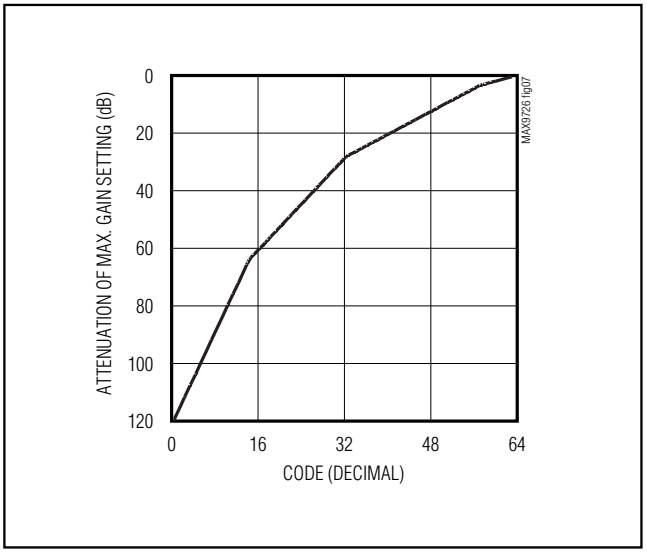


Figure 7. Volume-Control Transfer Function

Write Data Format

A write to the MAX9726 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0 (see Table 1), one byte of data to configure the command register, and a STOP condition. Figure 6 illustrates the proper format for one frame.

The MAX9726 only accepts write data, but it acknowledges the receipt of its address byte with the R/$\overline{W}$ bit set to 1. The MAX9726 does not write to the SDA bus in the event that the R/$\overline{W}$ bit is set to 1. Subsequently, the master reads all 1's from the MAX9726. Always set the R/$\overline{W}$ bit to zero to avoid this situation.

Command Register

The MAX9726 has one command register that is used to enable/disable shutdown, enable/disable BassMax, and set the volume. Table 2 describes the function of the bits contained in the command register.

Set B7 to 0 to shutdown the MAX9726. The MAX9726 wakes up from shutdown when B7 is set to 1 provided $\overline{SHDN}$ is high. $\overline{SHDN}$ must be high and B7 must be set to 1 for the MAX9726 to operate normally (see Table 3).

Set B6 to 1 to enable BassMax (see Table 4). The output signal's low-frequency response is boosted according to the external components connected between OUT_ and BM_. See the *Gain-Setting Components* section for details on choosing the external components.

Adjust the MAX9726's volume with control bits [5:0]. The volume is adjustable to one of 64 steps ranging from full mute to the maximum gain set by the external components. Table 5 lists all the possible volume settings for the MAX9726. Figure 7 shows the volume-control transfer function for the MAX9726.

Table 2. Command Register

B7	B6	B5	B4	B3	B2	B1	B0
Shutdown	BassMax Enable	Volume (See Table 5)					

Table 3. Shutdown Control, $\overline{SHDN}$ = V_{DD}

MODE	B7
Disabled	0
Enabled	1

Table 4. BassMax Control

MODE	B6
BassMax Disabled	0
BassMax Enabled	1

Table 5. MAX9726 Volume-Control Settings

B5	B4	B3	B2	B1	B0 (LSB)	ATTENUATION OF MAXIMUM GAIN SETTING (dB)
0	0	0	0	0	0	120
0	0	0	0	0	1	116
0	0	0	0	1	0	112
0	0	0	0	1	1	108
0	0	0	1	0	0	104
0	0	0	1	0	1	100
0	0	0	1	1	0	96
0	0	0	1	1	1	92
0	0	1	0	0	0	88
0	0	1	0	0	1	84
0	0	1	0	1	0	80
0	0	1	0	1	1	76
0	0	1	1	0	0	72
0	0	1	1	0	1	68
0	0	1	1	1	0	64
0	0	1	1	1	1	62
0	1	0	0	0	0	60
0	1	0	0	0	1	58
0	1	0	0	1	0	56
0	1	0	0	1	1	54
0	1	0	1	0	0	52
0	1	0	1	0	1	50
0	1	0	1	1	0	48
0	1	0	1	1	1	46
0	1	1	0	0	0	44
0	1	1	0	0	1	42
0	1	1	0	1	0	40
0	1	1	0	1	1	38
0	1	1	1	0	0	36
0	1	1	1	0	1	34
0	1	1	1	1	0	32
0	1	1	1	1	1	30
1	0	0	0	0	0	28

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Table 5. MAX9726 Volume-Control Settings (continued)

B5	B4	B3	B2	B1	B0 (LSB)	ATTENUATION OF MAXIMUM GAIN SETTING (dB)
1	0	0	0	0	1	27
1	0	0	0	1	0	26
1	0	0	0	1	1	25
1	0	0	1	0	0	24
1	0	0	1	0	1	23
1	0	0	1	1	0	22
1	0	0	1	1	1	21
1	0	1	0	0	0	20
1	0	1	0	0	1	19
1	0	1	0	1	0	18
1	0	1	0	1	1	17
1	0	1	1	0	0	16
1	0	1	1	0	1	15
1	0	1	1	1	0	14
1	0	1	1	1	1	13
1	1	0	0	0	0	12
1	1	0	0	0	1	11
1	1	0	0	1	0	10
1	1	0	0	1	1	9
1	1	0	1	0	0	8
1	1	0	1	0	1	7
1	1	0	1	1	0	6
1	1	0	1	1	1	5
1	1	1	0	0	0	4
1	1	1	0	0	1	3
1	1	1	0	1	0	2.5
1	1	1	0	1	1	2
1	1	1	1	0	0	1.5
1	1	1	1	0	1	1
1	1	1	1	1	0	0.5
1	1	1	1	1	1	0

Table 6. Initial Power-Up Command Register Status

MODE	B7	B6	B5	B4	B3	B2	B1	B0
Power-On Reset	1	1	1	1	1	1	1	1

Power-On Reset

The contents of the MAX9726's command register at power-on are as shown in Table 6.

Applications Information

Power Dissipation and Heatsinking

Linear power amplifiers can dissipate a significant amount of power under normal operating conditions. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} for the TQFN package is +39°C/W.

If the power dissipation exceeds the rated package dissipation, reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking. Large output, supply, and ground traces decrease θ_{JA}, allowing more heat to be transferred from the package to surrounding air.

Output Dynamic Range

Dynamic range is the difference between the noise floor of the system and the output level at 1% THD+N. It is essential that a system's dynamic range be known before setting the maximum output gain. Output clipping occurs if the output signal is greater than the dynamic range of the system. The DirectDrive architecture of the MAX9726 has increased dynamic range (for a given V_{DD}) compared to other single-supply amplifiers. Due to the absolute maximum ratings of the MAX9726 and to limit power dissipation, the MAX9726 includes internal circuitry that limits the output voltage to approximately ±2.5V.

Use the THD+N vs. Output Power graphs in the *Typical Operating Characteristics* section to identify the system's dynamic range. Find the output power that causes 1% THD+N for a given load. This point indicates the output power that causes the output to begin to clip. Use the following equation to determine the peak-to-peak output voltage that causes 1% THD+N for a given load.

$$V_{OUT(P-P)} = 2\sqrt{2(P_{OUT\_1\%} \times R_L}$$

where $P_{OUT\_1\%}$ is the output power that causes 1% THD+N, R_L is the load resistance, and $V_{OUT(P-P)}$ is the peak-to-peak output voltage. Determine the voltage gain (A_V) necessary to attain this output voltage based on the maximum peak-to-peak input voltage ($V_{IN(P-P)}$):

$$A_V = \frac{V_{OUT(P-P)}}{V_{IN(P-P)}}$$

The maximum voltage gain setting is determined by external components (see the *Gain-Setting Components* section).

UVLO

The MAX9726 features an undervoltage lockout (UVLO) function that prevents the device from operating if the supply voltage is less than 2.7V. This feature ensures proper operation during brownout conditions and prevents deep battery discharge. Once the supply voltage exceeds the UVLO threshold, the MAX9726 charge pump is turned on and the amplifiers are powered, provided that $\overline{SHDN}$ is high and B7 in the command register is set to 1.

Component Selection

Charge-Pump Capacitor Selection

Use ceramic capacitors with a low ESR for optimum performance. For optimal performance over the extended temperature range, select capacitors with an X7R dielectric.

Charge-Pump Flying Capacitor (C1)

The charge-pump flying capacitor connected between C1N and C1P affects the charge pump's load regulation and output impedance. Choosing a flying capacitor that is too small degrades the MAX9726's ability to provide sufficient current drive and leads to a loss of output voltage. Increasing the value of the flying capacitor improves load regulation and reduces the charge-pump output impedance. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graphs in the *Typical Operating Characteristics*.

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Charge-Pump Hold Capacitor (C2)

The hold capacitor's value and ESR directly affect the ripple at PV_{SS}. Ripple is reduced by increasing the value of the hold capacitor. Choosing a capacitor with lower ESR reduces ripple and output impedance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graphs in the *Typical Operating Characteristics*. C2 should be greater than or equal to the value of C1.

Input-Coupling Capacitor

The AC-coupling capacitor (C_{IN}) and input resistor (R_{IN}) form a highpass filter that removes any DC bias from an input signal. See the *Functional Diagram/Typical Operating Circuit*. C_{IN} prevents any DC components from the input signal source from appearing in the amplifier outputs. The -3dB point of the highpass filter, assuming zero-source impedance due to the input signal source, is given by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}} (Hz)$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors with low-voltage coefficient dielectrics. Aluminum electrolytic, tantalum, or film dielectric capacitors are good choices for AC-coupling capacitors. Capacitors with high-voltage coefficients, such as ceramics (non-C0G dielectrics), can result in increased distortion at low frequencies.

Gain-Setting Components

With BassMax disabled, the maximum gain of the MAX9726 is set by the values of the external resistors R_{IN} and R_F (see the *Functional Diagram/Typical Operating Circuit*). When BassMax is disabled, the maximum gain of the MAX9726 is:

$$A_V = 20 \times \log\left(\frac{R_F}{R_{IN}}\right) (dB)$$

where A_V is the maximum voltage gain in dB. The overall voltage gain of the MAX9726 with BassMax disabled is equal to:

$$A_{TOTAL} = A_V - ATTEN_{dB\_VOL} (dB)$$

where $ATTEN_{dB\_VOL}$ is the attenuation due to the volume setting in dB and A_{TOTAL} is the overall voltage gain of the MAX9726 in dB.

When BassMax is enabled, the bass-boost low-frequency response is set by the ratio of R1 to R2, by the following equation (see Figure 2):

$$A_{BOOST} = 20 \times \log\left(\frac{R1 + R2}{R1 - R2}\right) (dB)$$

where A_{BOOST} is the voltage gain boost at low frequencies in dB. A_{BOOST} is added to the gain realized by the volume setting and the gain set by resistors R_{IN} and R_F (A_V). The overall voltage gain of the MAX9726 at low frequencies with BassMax enabled is equal to:

$$A_{TOTAL\_BB} = A_V + A_{BOOST} - ATTEN_{dB\_VOL} (dB)$$

where A_{TOTAL_BB} is the overall gain of the MAX9726 at low frequencies in dB.

To maintain circuit stability, the ratio $\frac{R2}{R1 + R2}$ must not exceed one-half. A ratio equal to or less than one-third is recommended. The switch that shorts BM_ to SGND, when BassMax is disabled, can have an on-resistance as high as 300Ω. Choose a value for R1 that is greater than 40kΩ to ensure that positive feedback is negligible when BassMax is disabled. Table 7 contains a list of R2 values, with R1 = 47kΩ, and the corresponding low-frequency gain boost.

Table 7. BassMax Gain Examples (R1 = 47kΩ)

R2 (kΩ)	LOW-FREQUENCY GAIN BOOST (dB)
39	20.6
33	15.1
27	11.3
22	8.8
15	5.7
10	3.7

The low-frequency boost attained by the BassMax circuit is added to the gain realized by the maximum gain and volume settings. Select the BassMax gain so that the output signal remains within the dynamic range of the MAX9726. Output signal clipping occurs at low frequencies if the BassMax gain boost is excessively large. See the *Output Dynamic Range* section.

Capacitor C3 forms a pole and a zero according to the following equations:

$$f_{POLE} = \frac{R1 - R2}{2\pi \times C3 \times R1 \times R2}(Hz)$$

$$f_{ZERO} = \frac{R1 + R2}{2\pi \times C3 \times R1 \times R2}(Hz)$$

f_{POLE} is the frequency at which the gain boost begins to roll off. f_{ZERO} is the frequency at which the bass-boost gain no longer effects the transfer function. At frequencies greater than or equal to f_{ZERO}, the gain set by resistors R_{IN} and R_F and the volume control attenuation dominate. Table 8 contains a list of capacitor values and the corresponding poles and zeros for a given DC gain. See Figure 8 for an example of a gain profile using BassMax.

Table 8. BassMax Pole and Zero Examples for a Gain Boost of 8.8dB (R1 = 47kΩ, R2 = 22kΩ)

C3 (nF)	f_{POLE} (Hz)	f_{ZERO} (Hz)
100	38	106
82	47	130
68	56	156
56	68	190
47	81	230
22	174	490
10	384	1060

Single-Pole Active Lowpass Filter (LPF)

To configure the MAX9726 as an active single-pole lowpass filter (Figure 9), connect a single feedback capacitor (C_F) in parallel with the feedback resistor (R_F). The -3dB point (below passband) of the active lowpass filter is equal to:

$$f_{-3dB} = \frac{1}{2\pi R_F C_F}(Hz)$$

The passband gain of the active filter is determined by the external component values described in the *Gain-Setting Components* section.

To minimize distortion, use capacitors with low-voltage coefficient dielectrics when selecting C_F. Film or C0G dielectric capacitors are good choices for feedback capacitors. Capacitors with high-voltage coefficients, such as ceramics (non-C0G dielectrics), can result in increased distortion.

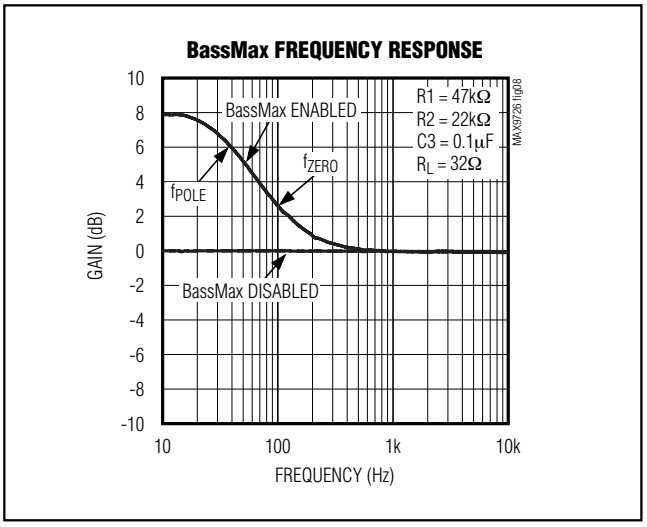


Figure 8. BassMax Gain Profile Example

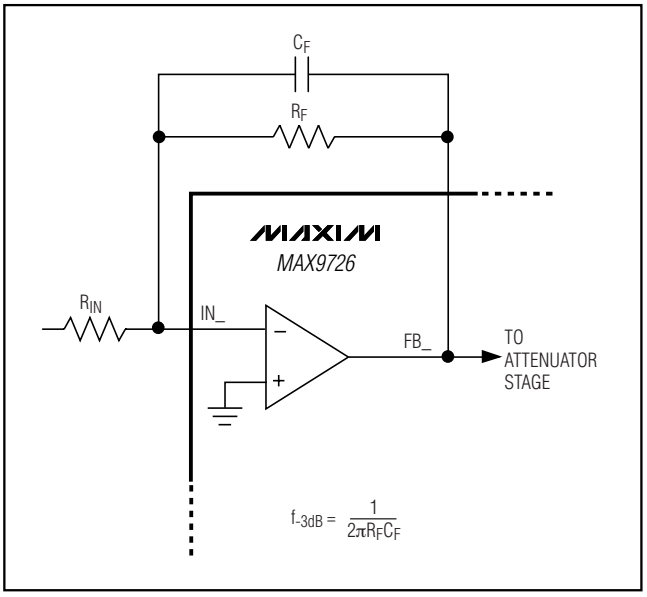


Figure 9. Single-Pole Active Lowpass Filter

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Summing Amplifier (Audio Mixer)

Figure 10 shows the MAX9726 configured as a summing amplifier, which allows multiple audio sources to be linearly mixed together. Using this configuration, the output of the MAX9726 is equal to the weighted sum of the input signals:

$$V_{OUT\_} = -\left(V_{IN1}\frac{R_F}{R_{IN1}} + V_{IN2}\frac{R_F}{R_{IN2}} + V_{IN3}\frac{R_F}{R_{IN3}}\right)$$

As shown in the above equation, the weighting or amount of gain applied to each input signal source is determined by the ratio of R_F and the respective input resistor (R_{IN1}, R_{IN2}, R_{IN3}) connected to each signal source. When BassMax is enabled, the low-frequency gain (A_{BOOST}) set by R1, R2, and C3 (see the *Gain-Setting Components* section) adds to the gain determined by R_F and $R_{IN\_}$. Select R_F and $R_{IN\_}$ such that the dynamic range of the MAX9726 is not exceeded when BassMax is enabled and/or when the input signals are at their maximum values and in phase with each other.

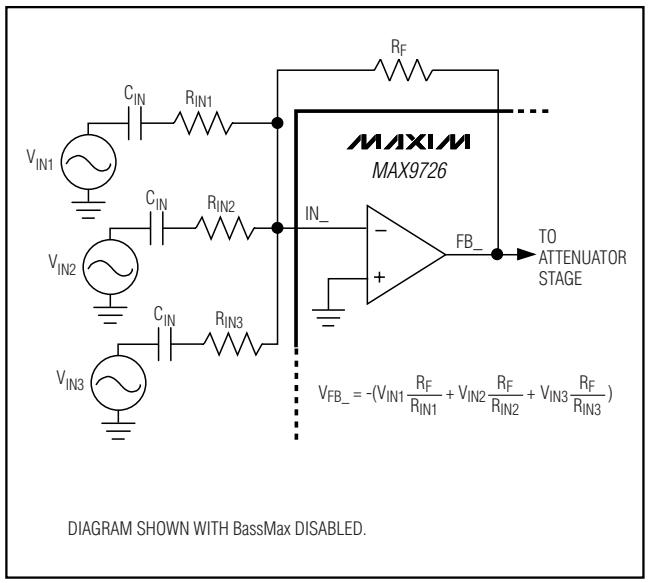


Figure 10. Summing Amplifier

Layout and Grounding

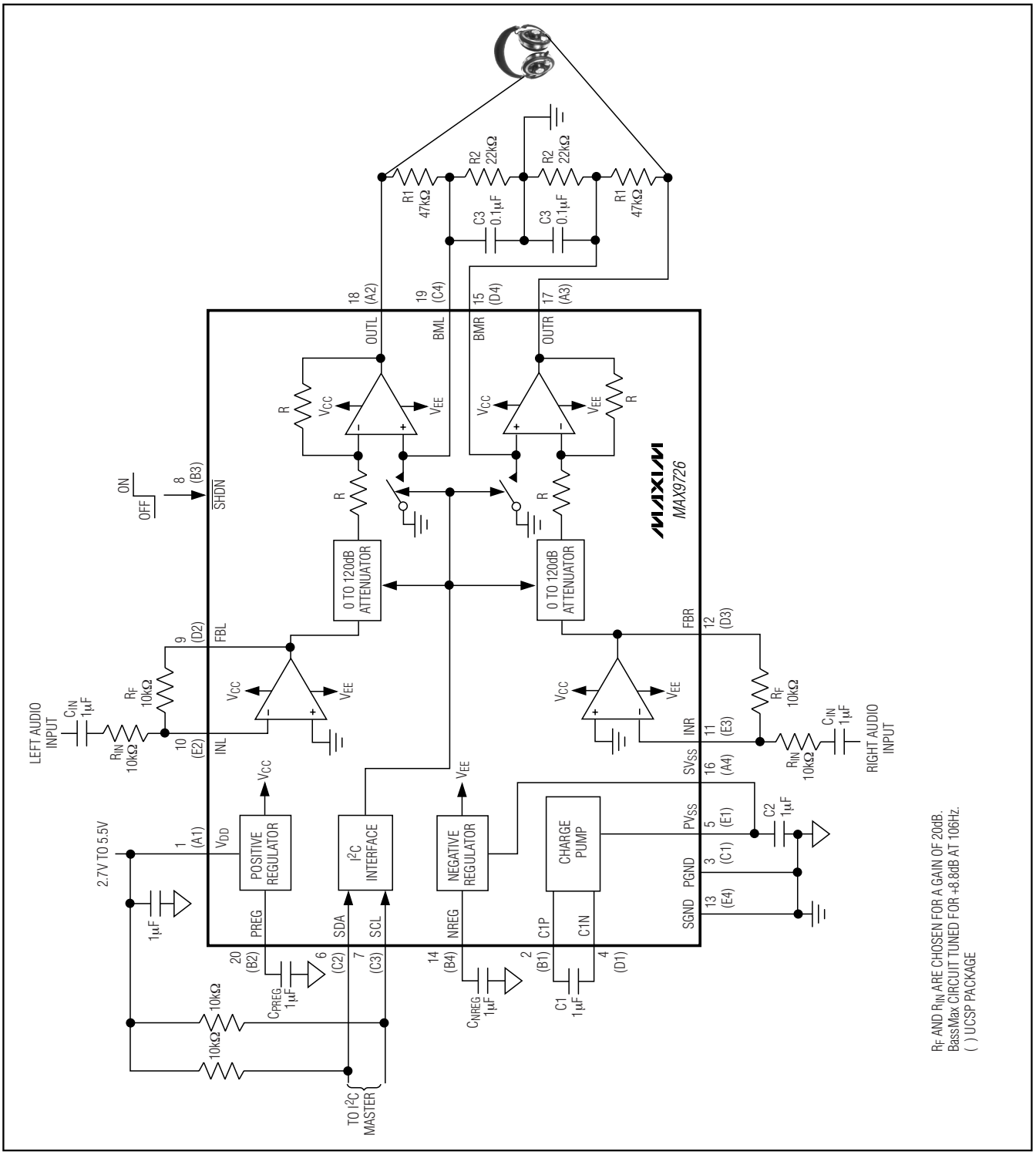
Proper layout and grounding are essential for optimum performance. Connect PGND and SGND together at a single point (star ground point) on the PC board. Connect PV_{SS} to SV_{SS} at the device and bypass this connection with a 1µF capacitor to PGND. Bypass V_{DD}, PREG, and NREG to PGND with a 1µF capacitor. Place the power-supply bypass capacitor and the charge-pump hold capacitor as close as possible to the MAX9726. Route PGND, and all traces that carry switching transients, away from SGND and the audio signal path. Route digital signal traces away from the audio signal path. Make traces perpendicular to each other when routing digital signals over or under audio signals.

The TQFN package features an exposed pad that improves thermal efficiency. **Ensure that the exposed pad is electrically isolated from PGND, SGND, and V_{DD}. Connect the exposed pad to PV_{SS} when the board layout dictates that the exposed pad cannot be left unconnected.**

UCSP Applications Information

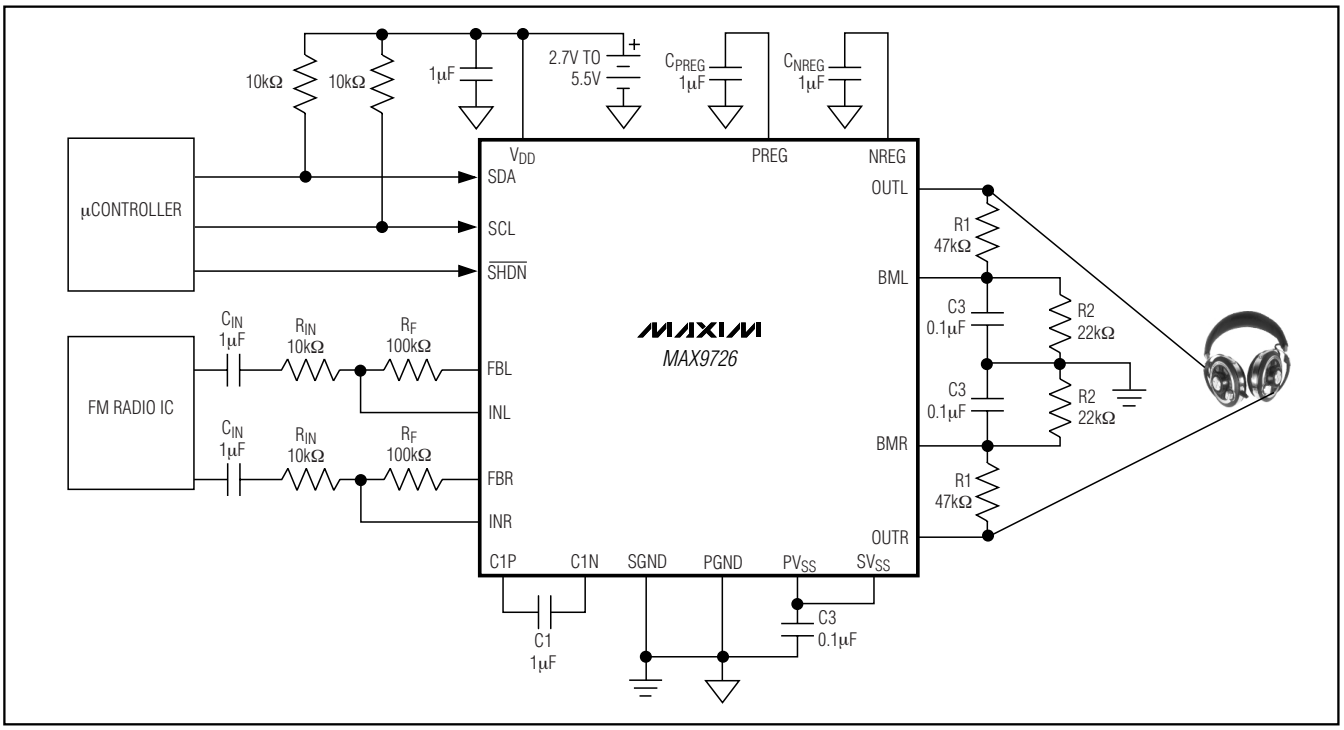
For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to Maxim's website at www.maxim-ic.com/ucsp and look up the Application Note: *UCSP—A Wafer-Level Chip-Scale Package*.

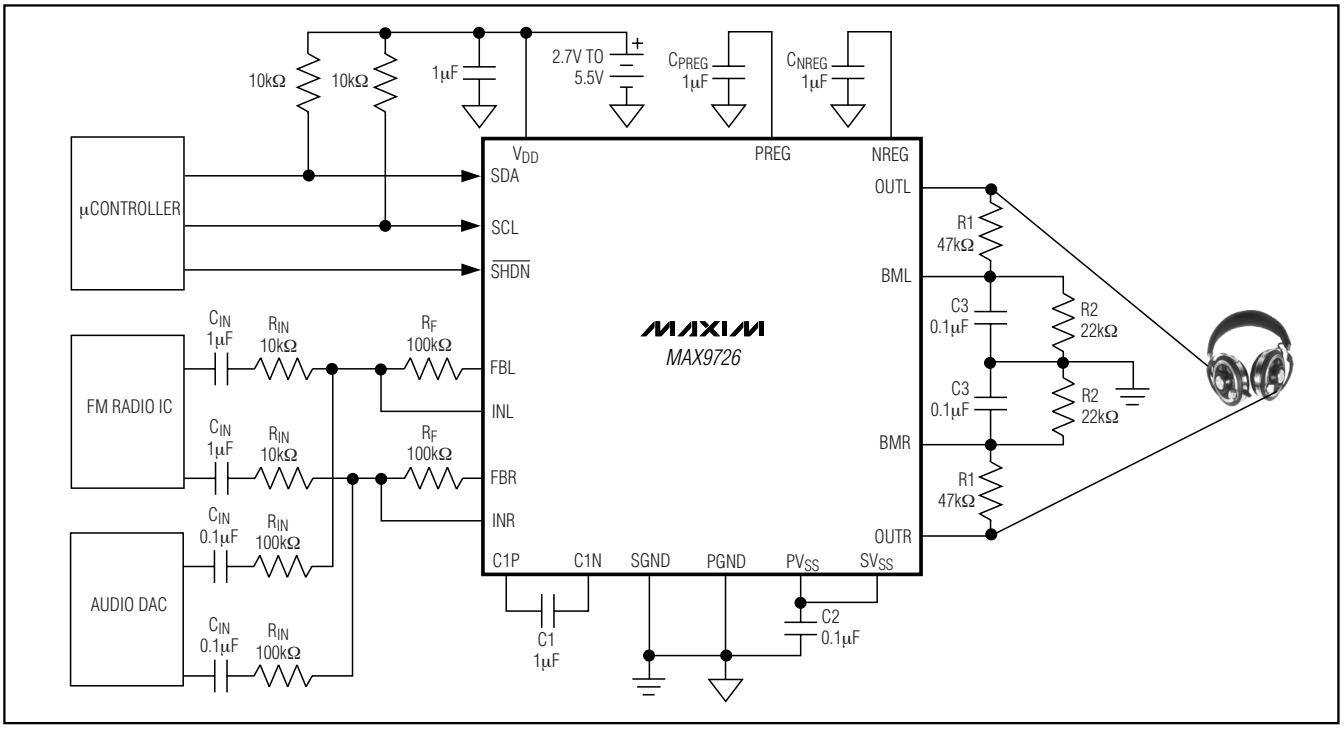
Functional Diagram/Typical Operating Circuit



DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

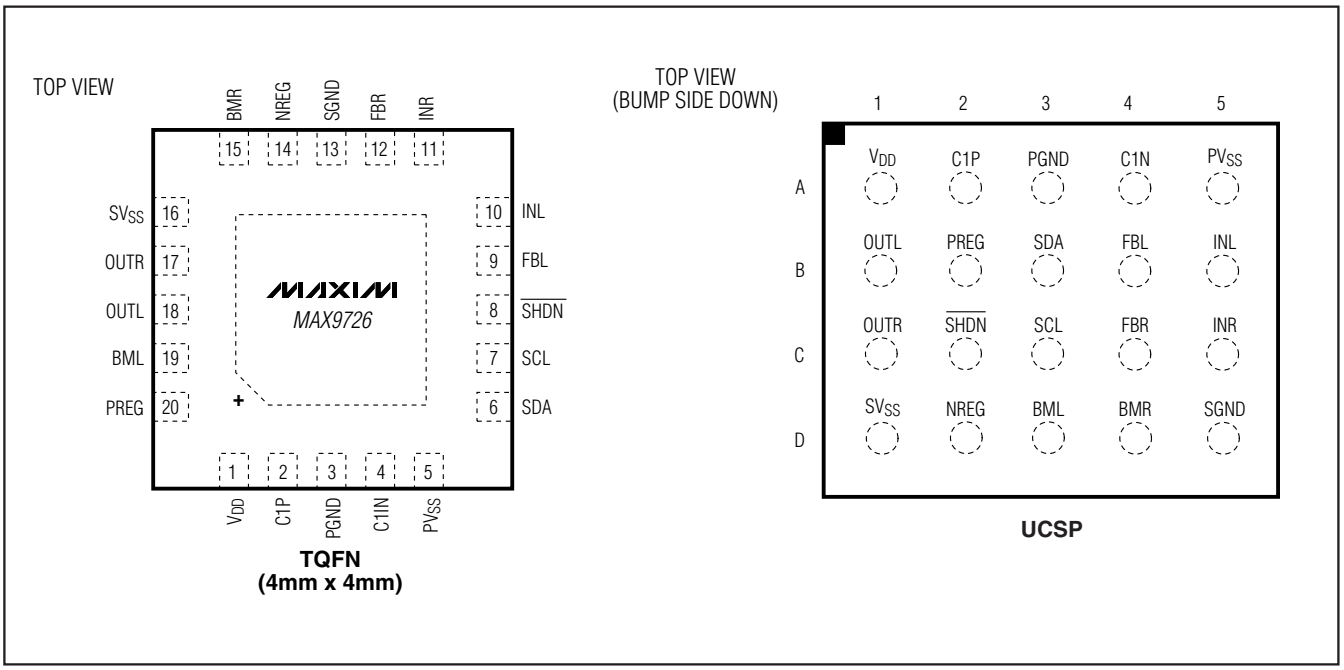
System Diagrams





DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Pin Configurations



Chip Information

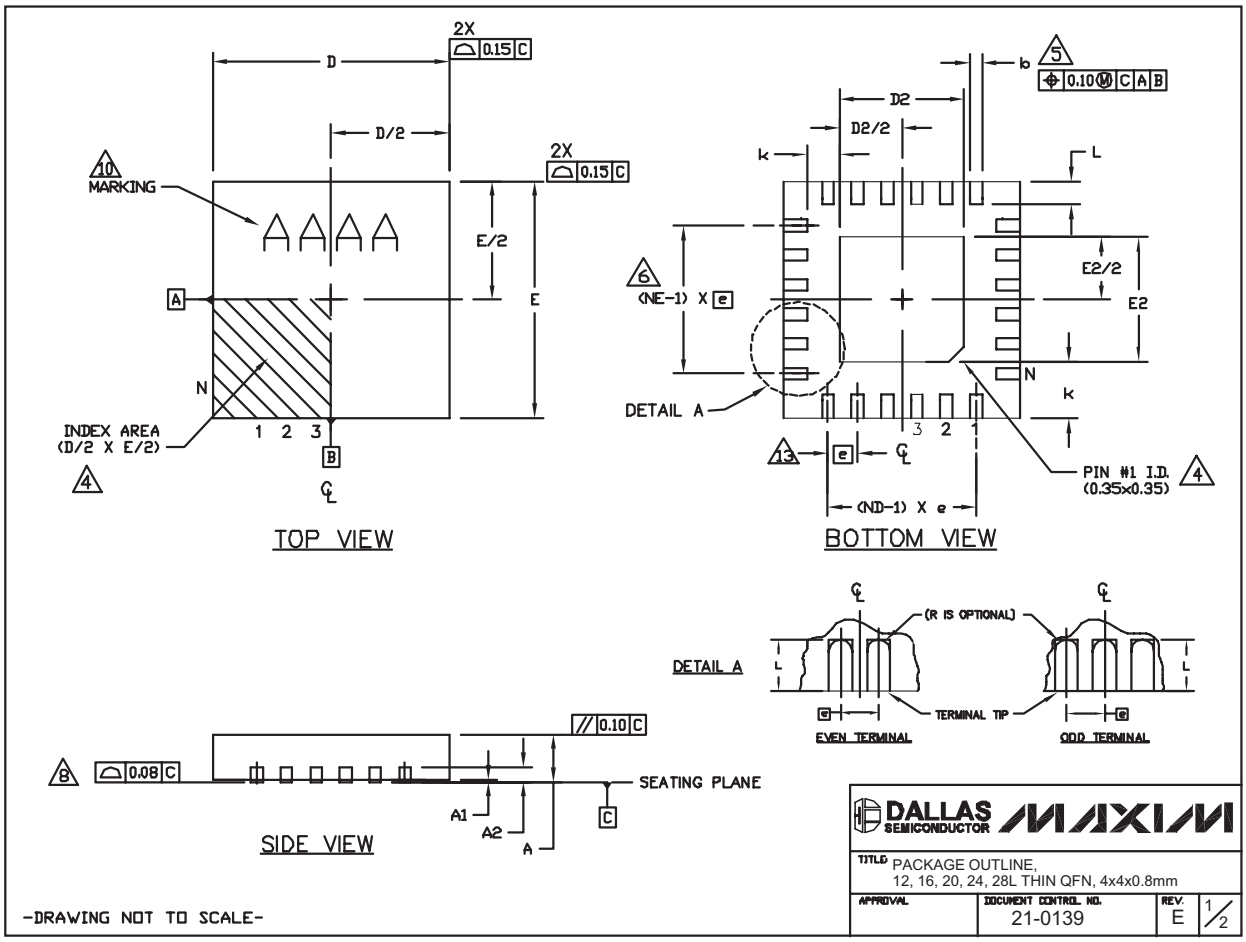
PROCESS: BiCMOS

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

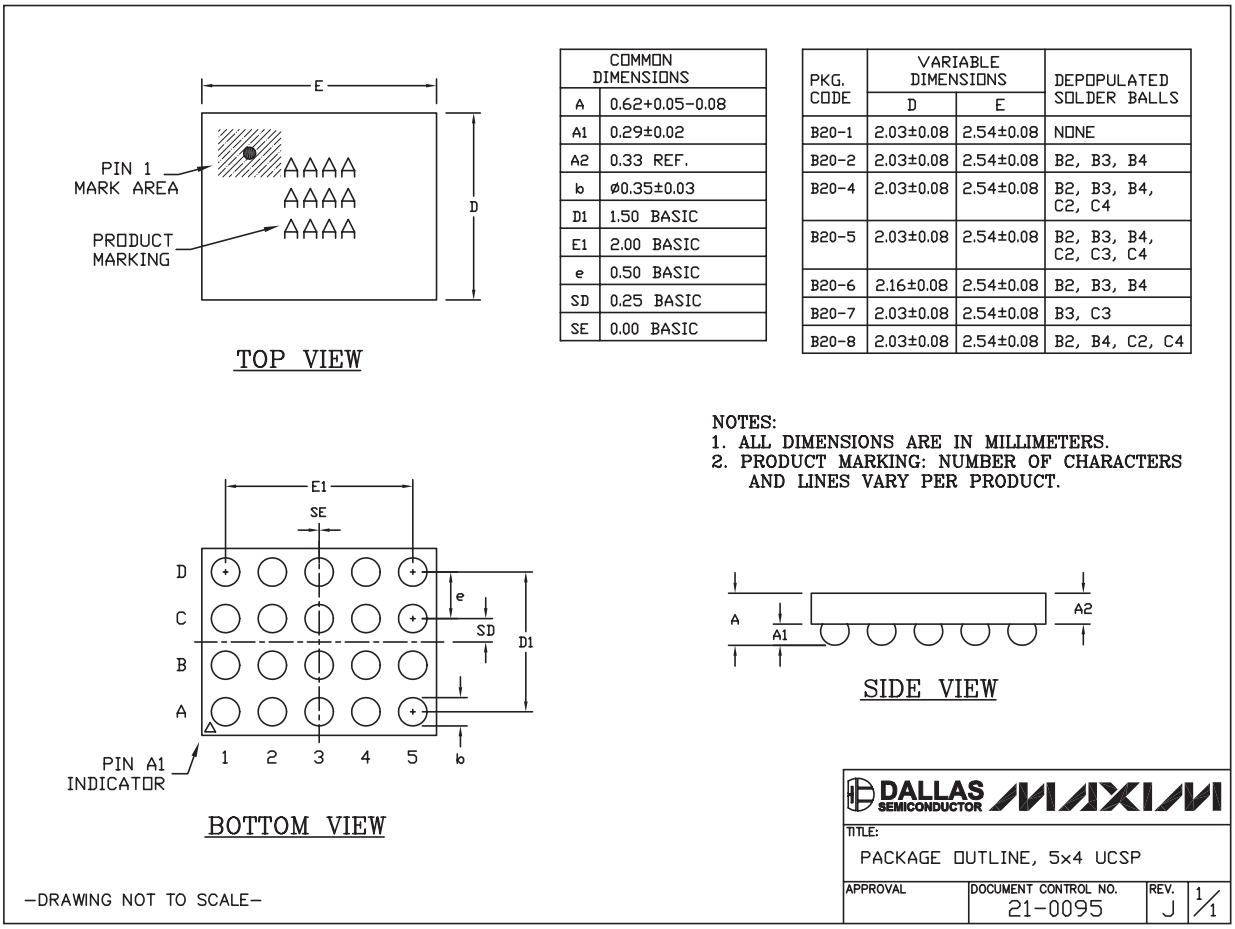
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2

DirectDrive, Headphone Amplifier with BassMax, I²C, Volume and Gain Control

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B20-1	2.03±0.08	2.54±0.08	NONE
B20-2	2.03±0.08	2.54±0.08	B2, B3, B4
B20-4	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C4
B20-5	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C3, C4
B20-6	2.16±0.08	2.54±0.08	B2, B3, B4
B20-7	2.03±0.08	2.54±0.08	B3, C3
B20-8	2.03±0.08	2.54±0.08	B2, B4, C2, C4

MAX9726

Part Number Table

Notes:

1. See the MAX9726 QuickView Data Sheet for further information on this product family or download the MAX9726 full data sheet (PDF, 472kB).
2. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
3. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See full data sheet or Part Naming Conventions.
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX9726AETP+T				-40C to +85C	RoHS/Lead-Free: Yes
MAX9726BETP+T				-40C to +85C	RoHS/Lead-Free: Yes
MAX9726AETP+			THIN QFN;20 pin;4X4X0.8mm Dwg: 21-0139E (PDF) Use pkgcode/variation: T2044+3*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX9726BETP+			THIN QFN;20 pin;4X4X0.8mm Dwg: 21-0139E (PDF) Use pkgcode/variation: T2044+3*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis

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