

MC100EP16VT

3.3 V / 5 V ECL Differential Receiver/Driver with Variable Output Swing and Internal Input Termination

Description

The MC100EP16VT is a differential receiver functionally equivalent to the 100EP16 with input pins controlling the amplitude of the outputs (pin 1) and providing an internal termination network (pin 4).

The V_{CTRL} input pin controls the output amplitude of the EP16VT and is referenced to V_{CC} . (See Figure 4.) The operational range of the V_{CTRL} input is from $\leq V_{BB}$ (a supply at $V_{CC}-1.42$ V, maximum output amplitude) to V_{CC} (minimum output amplitude). V_{BB} is an externally supplied voltage equal to $V_{CC}-1.42$ V (See Figures 2 and Figure 3). A variable resistor between V_{CC} and V_{BB} , with the wiper driving V_{CTRL} , can control the output amplitude. Typical application circuits and a V_{CTRL} Voltage vs. Output Amplitude graph are described in this data sheet. When left open, the V_{CTRL} pin will be internally pulled down to V_{EE} and operate as a standard EP16, with 100% output amplitude.

The V_{TT} input pin offers an internal termination network for a 50 Ω line impedance environment, shown in Figure 1. For further reference, see Application Note [AND8020](#), Termination of ECL Logic Devices. Input considerations are required for D and \bar{D} under no signal conditions to prevent instability.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

Features

- 220 ps Propagation Delay
- Maximum Frequency > 4 GHz Typical (See Graph)
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:
 - ♦ $V_{CC} = 3.0$ V to 5.5 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
 - ♦ $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -5.5 V
- Open Input Default State
- 50 Ω Internal Termination Resistor
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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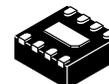
www.onsemi.com



SOIC-8 NB
D SUFFIX
CASE
751-07

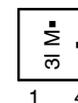
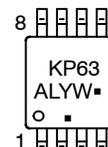
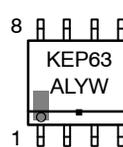


TSSOP-8
DT SUFFIX
CASE
948R-02



DFN-8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP16VTDG	SOIC-8 NB (Pb-Free)	98 Units/Tube
MC100EP16VTDR2G	SOIC-8 NB (Pb-Free)	2500/Tape & Reel
MC100EP16VTDTG	TSSOP-8 (Pb-Free)	100 Units/Tube
MC100EP16VTDR2G	TSSOP-8 (Pb-Free)	2500/Tape & Reel
MC100EP16VTMNR4G	DFN-8 (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MC100EP16VT

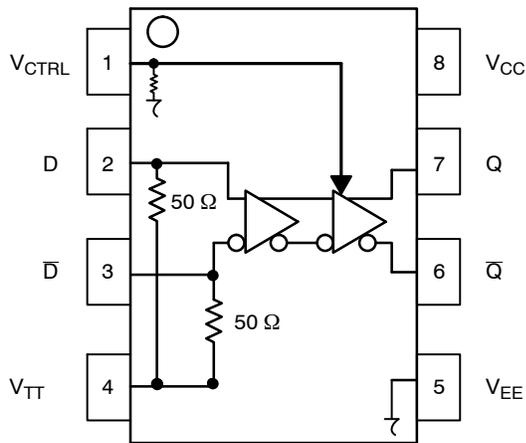


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D, \bar{D}	ECL Data Inputs
Q, \bar{Q}	ECL Data Outputs
V_{CTRL}^*	Output Swing Control
V_{TT}	Termination Supply
V_{CC}	Positive Supply
V_{EE}	Negative Supply
EP	(DFN-8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

* Pin will default LOW when left open.

Table 2. ATTRIBUTES

Characteristics	Value	Value
Internal Input Pulldown Resistor	75 k Ω	
Internal Input Pullup Resistor	N/A	
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg	
SOIC-8 NB TSSOP-8 DFN-8	Level 1 Level 3 Level 1	
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count	140 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note [AND8003/D](#).

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V
I _{out}	Output Current	Continuous Surge		50 100	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB	190 130	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8	185 140	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN-8	129 84	°C/W
T _{sol}	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN-8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V _{OH}	Output HIGH Voltage (Max Swing) (Note 2) V _{CC} ≥ V _{CTRL} ≥ V _{EE}	2155		2405	2155		2405	2155		2405	mV
V _{OL}	Output LOW Voltage (Max Swing) (Note 2) V _{CTRL} ≤ V _{BB}	1355	1490	1605	1355	1520	1605	1355	1520	1605	mV
	V _{CC} ≥ V _{CTRL} > V _{BB}		See Fig.2			See Fig.2			See Fig.2		
	V _{CTRL} = V _{CC} (Min Swing)	2105	2230	2355	2095	2220	2345	2065	2190	2315	
V _{IH}	D, \bar{D} Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V _{IL}	D, \bar{D} Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V _{CTRL}	Input Voltage (V _{CTRL})	V _{EE}		V _{CC}	V _{EE}		V _{CC}	V _{EE}		V _{CC}	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		2.9	2.0		2.9	2.0		2.9	V
I _{IH}	Input HIGH Current (V _{TT} Open)			150			150			150	μA
I _{IL}	Input LOW Current (V _{TT} Open)	-150			-150			-150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.
2. All loading with 50 Ω to V_{CC} - 2.0 V. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
3. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 5. DC CHARACTERISTICS, PECL ($V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Note 2) $V_{CC} > V_{CTRL} > V_{EE}$	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 2) $V_{CTRL} \leq V_{BB}$	3055	3190	3305	3055	3220	3305	3055	3220	3305	mV
	$V_{CC} \geq V_{CTRL} > V_{BB}$		See Fig.2			See Fig.2		See Fig.2			
	$V_{CTRL} = V_{CC}$ (Min Swing)	3805	3930	4055	3795	3920	4045	3765	3890	4015	
V_{IH}	D, \bar{D} Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	D, \bar{D} Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		4.6	2.0		4.6	2.0		4.6	V
I_{IH}	Input HIGH Current (V_{TT} Open)			150			150			150	μA
I_{IL}	Input LOW Current (V_{TT} Open)	-150			-150			-150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$. V_{OH} does not change with V_{CTRL} . V_{OL} changes with V_{CTRL} . V_{CTRL} is referenced to V_{CC} .
3. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 6. DC CHARACTERISTICS, NECL ($V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Note 2) $V_{CC} > V_{CTRL} > V_{EE}$	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 2) $V_{CTRL} \leq V_{BB}$	-1945	-1810	-1695	-1945	-1780	-1695	-1945	-1780	-1695	mV
	$V_{CC} \geq V_{CTRL} > V_{BB}$		See Fig.2			See Fig.2			See Fig.2		
	$V_{CTRL} = V_{CC}$ (Min Swing)	-1195	-1070	-945	-1205	-1080	-955	-1235	-1110	-985	
V_{IH}	D, \bar{D} Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	D, \bar{D} Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	$V_{EE}+2.0$		-0.4	$V_{EE}+2.0$		-0.4	$V_{EE}+2.0$		-0.4	V
I_{IH}	Input HIGH Current (V_{TT} Open)			150			150			150	μA
I_{IL}	Input LOW Current (V_{TT} Open)	-150			-150			-150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} .
2. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$. V_{OH} does not change with V_{CTRL} . V_{OL} changes with V_{CTRL} . V_{CTRL} is referenced to V_{CC} .
3. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V or $V_{CC} = 3.0\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (See Figure 8. F_{max}/JITTER)		> 4			> 4			> 4		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential Max Swing Min Swing	250 200	300 250	350 300	250 200	300 250	350 300	250 200	300 250	350 300	ps
t_{SKEW}	Duty Cycle Skew (Note 2)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 8. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential Configuration) (Note 3)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times Max Swing Q (20% - 80%) Min Swing	70 30	120 80	170 130	80 20	130 70	180 120	100 20	150 70	200 120	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. $V_{PP}(\text{min})$ is minimum input swing for which AC parameters are guaranteed.

MC100EP16VT

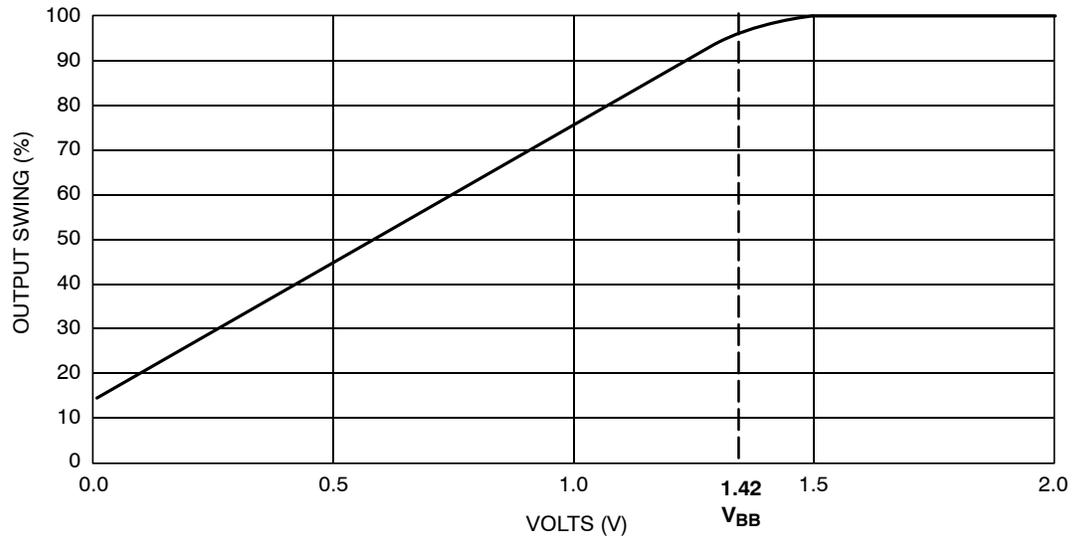


Figure 2. $V_{CC} - V_{CTRL}$ (pin #1)

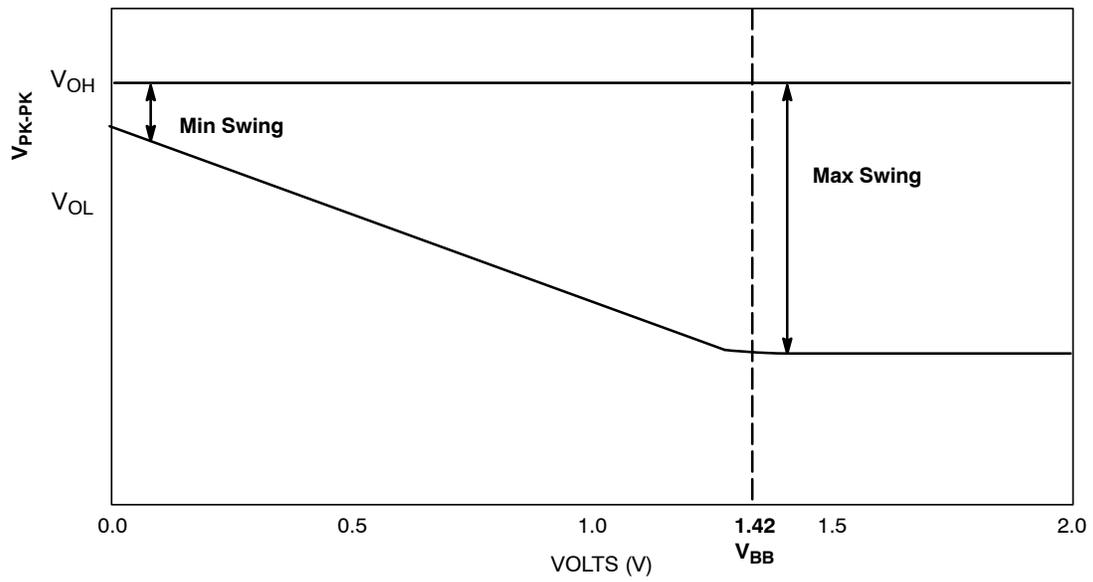


Figure 3. $V_{CC} - V_{CTRL}$

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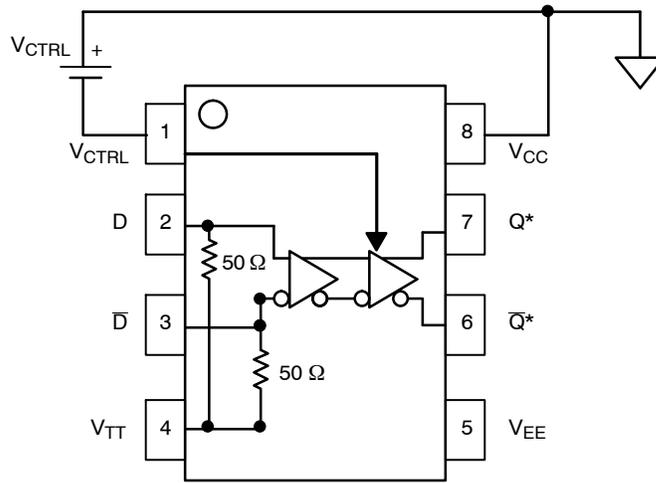


Figure 4. Voltage Source Implementation, V_{CTRL} Pin 1

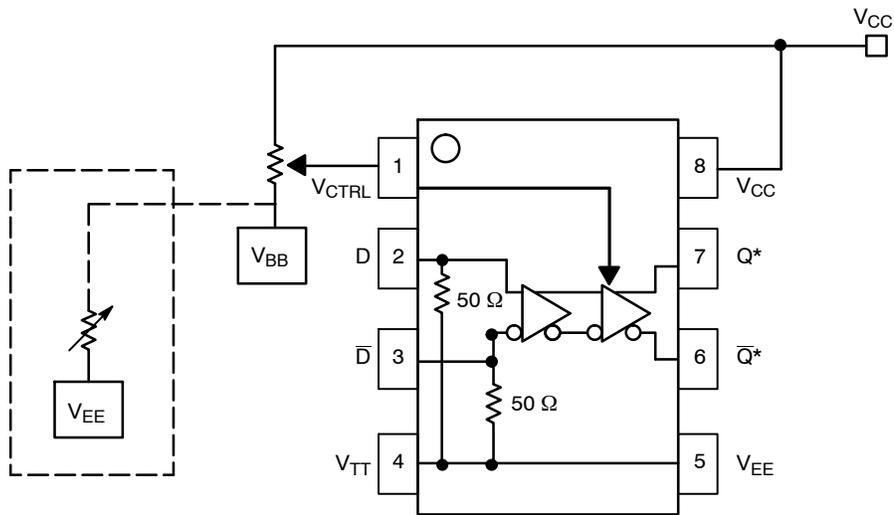


Figure 5. Alternative Implementations, V_{CTRL} Pin 1

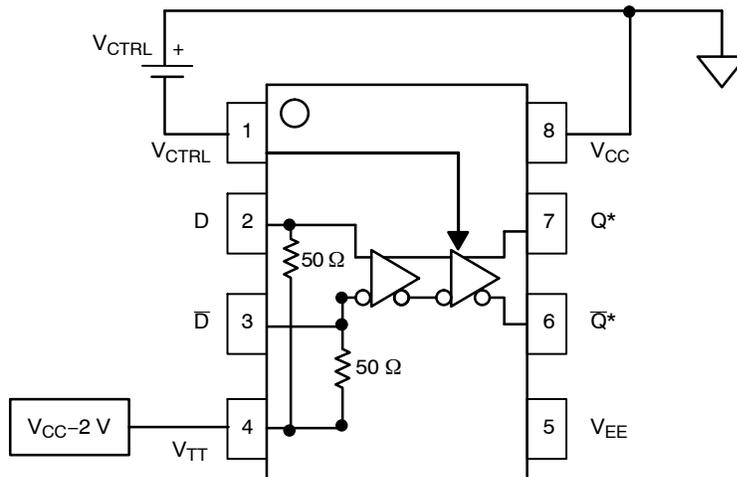


Figure 6. Standard Termination Method, V_{TT} Pin 4

MC100EP16VT

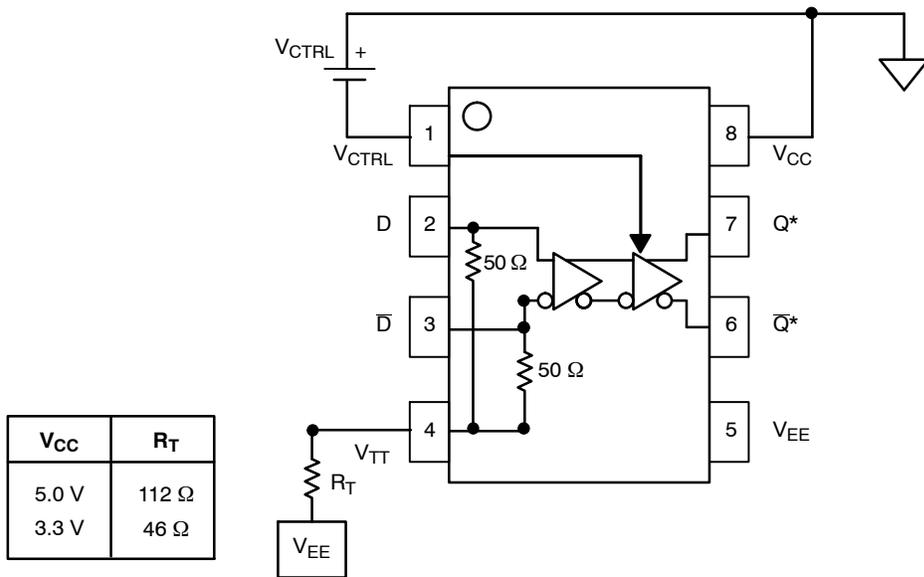


Figure 7. Alternate “Y” Termination Method, V_{TT} Pin 4

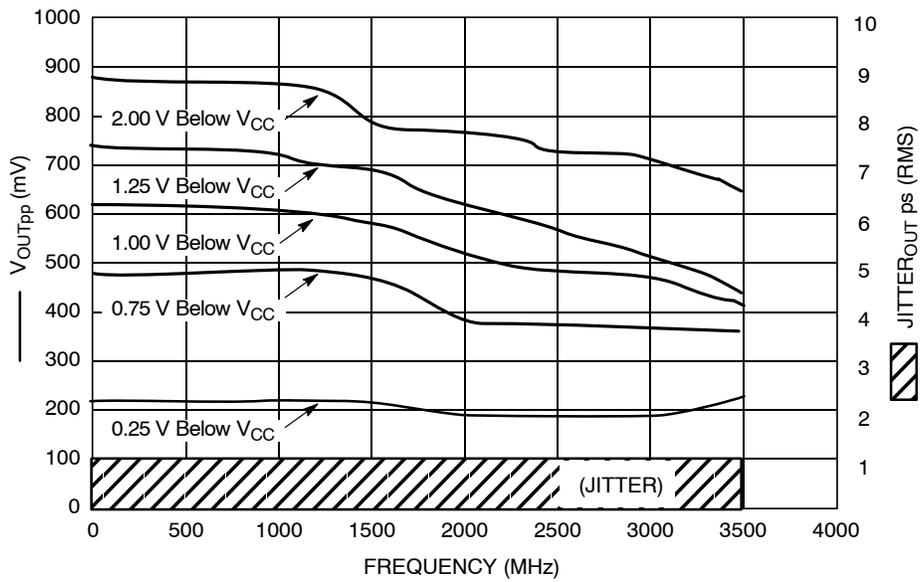


Figure 8. F_{max}/Jitter

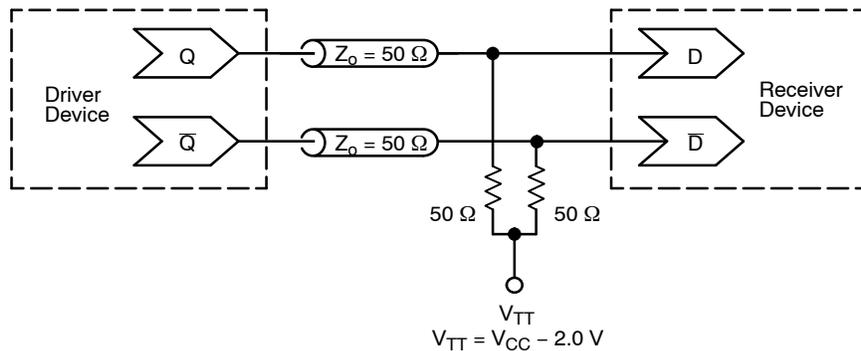


Figure 9. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

MC100EP16VT

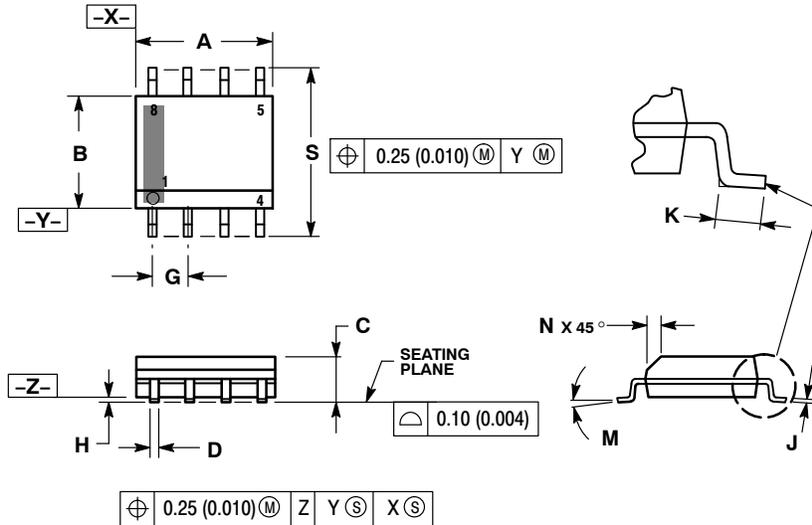
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC100EP16VT

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

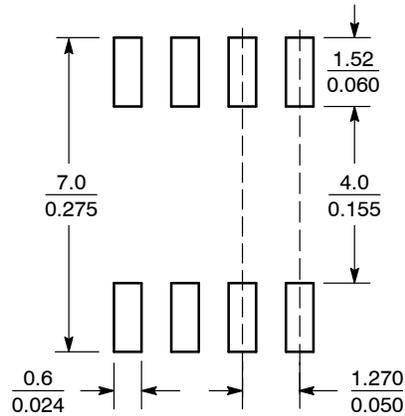


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



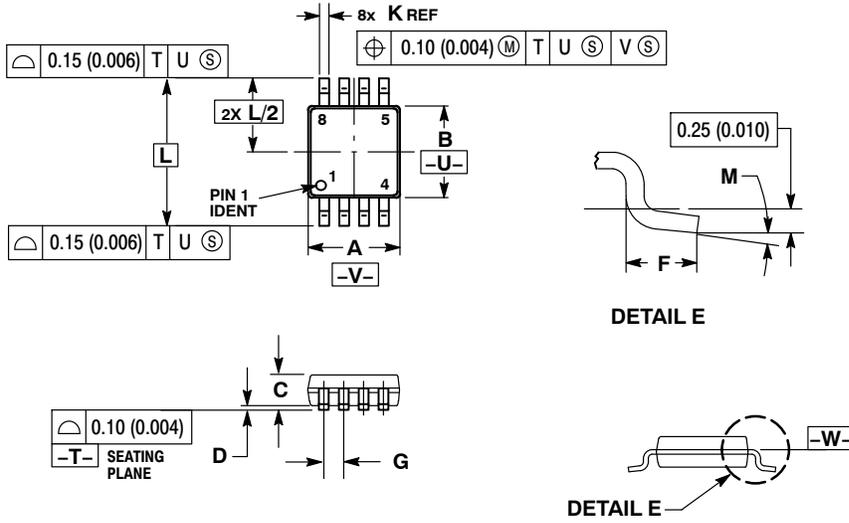
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

MC100EP16VT

PACKAGE DIMENSIONS

TSSOP-8
CASE 948R-02
ISSUE A



NOTES:

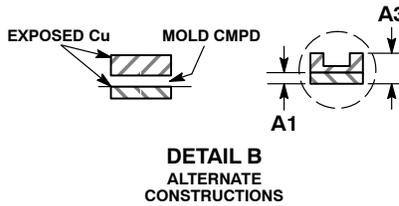
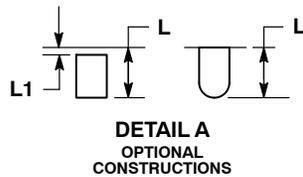
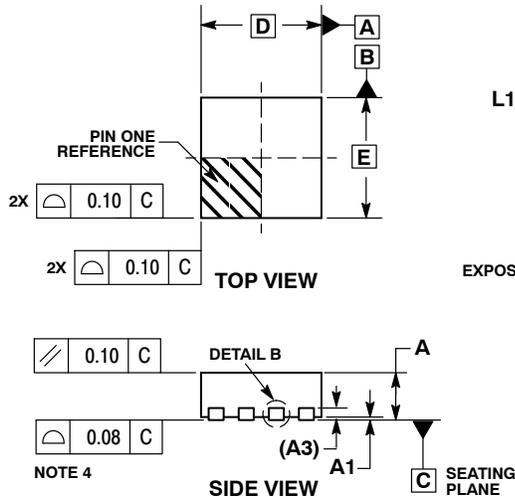
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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PACKAGE DIMENSIONS

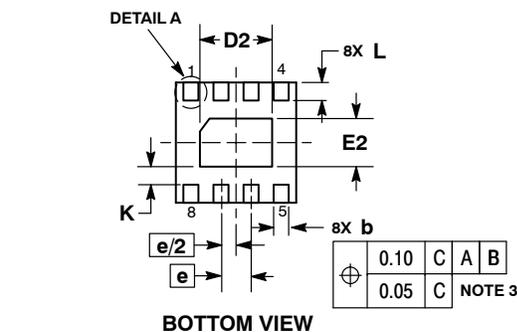
DFN-8 2x2, 0.5P
CASE 506AA
ISSUE F



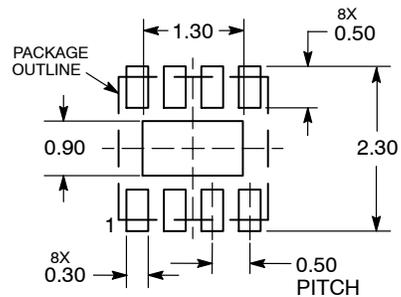
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1	---	0.10



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDRRM/D](#).

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