

MC10H176

Hex D Master-Slave Flip-Flop

Description

The MC10H176 contains six master slave type D flip-flops with a common clock. This MECL 10H™ part is a functional/pinout duplication of the standard MECL 10K™ family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

Features

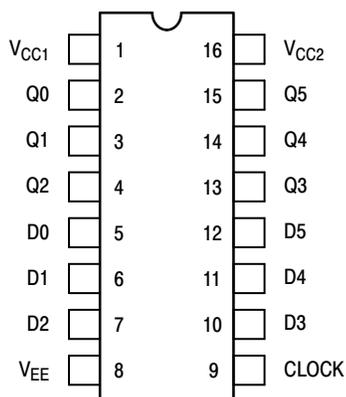
- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

CLOCKED TRUTH TABLE

C	Q	Q _{n+1}
L	X	Q _n
H *	L	L
H *	H	H

* A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT

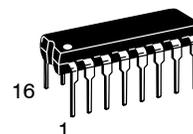


Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



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**PDIP-16
P SUFFIX
CASE 648-02**

MARKING DIAGRAMS*



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping
MC10H176PG	PDIP-16 (Pb-Free)	25 Units/Tube

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Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply ($V_{CC} = 0$)	-8.0 to 0	Vdc
V_I	Input Voltage ($V_{CC} = 0$)	0 to V_{EE}	Vdc
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range Plastic Ceramic	-55 to +150 -55 to +165	°C

Table 2. ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2\text{ V} \pm 5\%$) (Note 1)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
I_E	Power Supply Current	-	123	-	112	-	123	mA
I_{inH}	Input Current High Pins 5,6,7,10,11,12 Pin 9	-	425	-	265	-	265	μA
		-	670	-	420	-	420	
I_{inL}	Input Current Low	0.5	-	0.5	-	0.3	-	μA
V_{OH}	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

1. Each MECL 10H™ series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Table 3. AC PARAMETERS

t_{pd}	Propagation Delay	0.9	2.1	0.9	2.2	1.0	2.4	ns
t_{set}	Set-up Time	1.5	-	1.5	-	1.5	-	ns
t_{hold}	Hold Time	0.9	-	0.9	-	1.0	-	ns
t_r	Rise Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
t_f	Fall Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
f_{tog}	Toggle Frequency	250	-	250	-	250	-	MHz

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

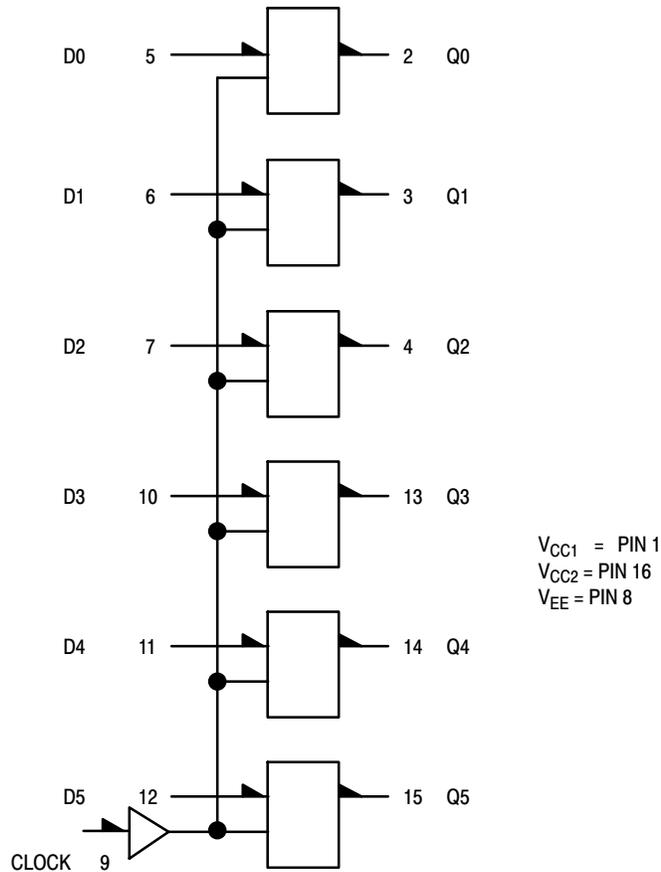
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APPLICATION INFORMATION

The MC10H176 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change

only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

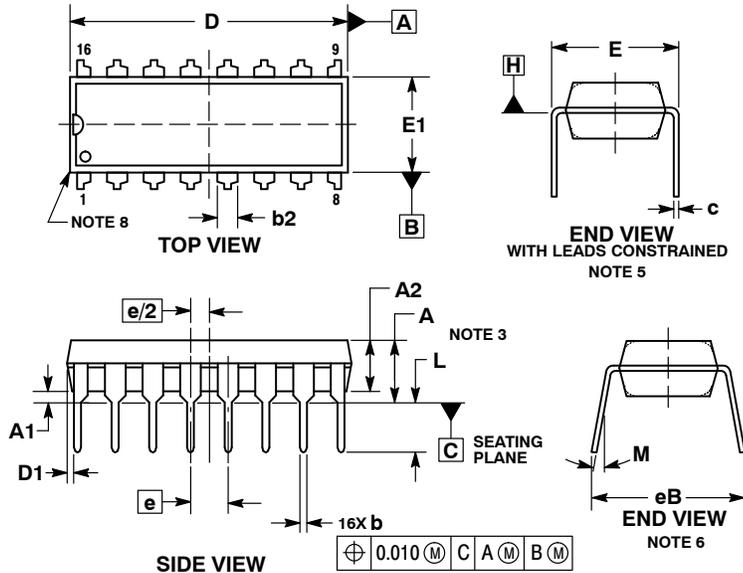
LOGIC DIAGRAM



MC10H176

PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 ISSUE V



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

STYLE 1:

- PIN 1. CATHODE
- ANODE

STYLE 2:

- PIN 1. COMMON DRAIN
- GATE
- SOURCE
- GATE
- SOURCE
- GATE
- SOURCE
- GATE
- SOURCE

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