# 2-Input Exclusive OR Gate / CMOS Logic Level Shifter

# with LSTTL-Compatible Inputs

The MC74VHC1GT86 is an advanced high speed CMOS 2-input Exclusive OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT86 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT86 to be used to interface 5.0 V circuits to 3.0 V circuits. The output structures also provide protection when  $V_{\rm CC}$  = 0 V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

#### **Features**

- High Speed:  $t_{PD} = 4.8 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 1 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- TTL-Compatible Inputs:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- CMOS–Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 83; Equivalent Gates = 16
- Pb-Free Packages are Available

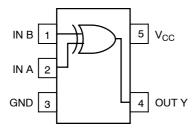


Figure 1. Pinout (Top View)

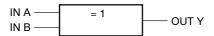


Figure 2. Logic Symbol



# ON Semiconductor®

http://onsemi.com



SC-88A/SOT-353/SC-70 DF SUFFIX CASE 419A



**MARKING** 



TSOP-5/SOT-23/SC-59 DT SUFFIX CASE 483



M = Date Code\*

A = Assembly Location

= Year

W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)
\*Date Code orientation and/or position in

\*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT					
1	IN B				
2	IN A				
3	GND				
4	OUT Y				
5	V <sub>CC</sub>				

#### **FUNCTION TABLE**

Inp	uts	Output
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

#### **MAXIMUM RATINGS**

Symbol	Characteri	stics	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		−0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage		−0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage	$V_{CC} = 0$ High or Low State	−0.5 to 7.0 −0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current		-20	mA
lok	Output Diode Current	V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub>	+20	mA
l <sub>OUT</sub>	DC Output Current, per Pin		+25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND		+50	mA
$P_{D}$	Power dissipation in still air	SC-88A, TSOP-5	200	mW
$\theta_{\sf JA}$	Thermal resistance	SC-88A, TSOP-5	333	°C/W
TL	Lead temperature, 1 mm from case for 10	S	260	°C
TJ	Junction temperature under bias		+150	°C
T <sub>stg</sub>	Storage temperature		-65 to +150	°C
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I <sub>Latchup</sub>	Latchup Performance Above V <sub>C</sub>	<sub>CC</sub> and Below GND at 125°C (Note 5)	±500	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. Derating SC–88A Package: –3 mW/°C from 65° to 125°C TSOP5 Package: –3 mW/°C from 65° to 125°C
- 2. Tested to EIA/JESD22-A114-A
- 3. Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- 5. Tested to EIA/JESD78

# **RECOMMENDED OPERATING CONDITIONS**

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	3.0	5.5	V
V <sub>IN</sub>	DC Input Voltage	0.0	5.5	V
V <sub>OUT</sub>	DC Output Voltage V <sub>CC</sub> High or Low St		5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time $ V_{CC} = 3.3 \ V \pm 0.3 \\ V_{CC} = 5.0 \ V \pm 0.8 \\ $	0 0 0	100 20	ns/V

# **DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES**

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

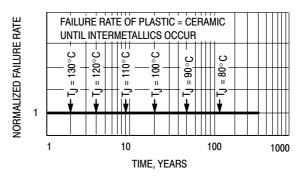


Figure 3. Failure Rate vs. Time **Junction Temperature** 

# DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	1	A = 25°(	С	T <sub>A</sub> ≤	85°C	-55 ≤ T <sub>A</sub>	. ≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
	$V_{IN} = V_{IH}$ or $V_{IL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		<b>V</b>
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50 \mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
	$V_{IN} = V_{IH}$ or $V_{IL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.0		20		40	μΑ
I <sub>CCT</sub>	Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.65	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	μΑ

# AC ELECTRICAL CHARACTERISTICS $C_{load}$ = 50 pF, Input $t_r$ = $t_f$ = 3.0 ns

				Т	_A = 25°(	0	T <sub>A</sub> ≤	85°C	-55 ≤ T <sub>A</sub>	≤ 125°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay,	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		5.0 6.2	11.0 14.5		13.0 16.5		15.5 19.5	ns
	Input A or B to Y	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		3.1 4.2	6.8 8.8		8.0 10.0		10.0 12.0	
C <sub>IN</sub>	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Note 6)	11	pF

<sup>6.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

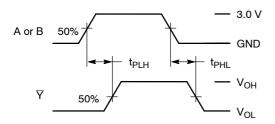
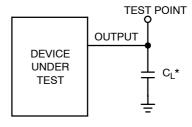


Figure 4. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

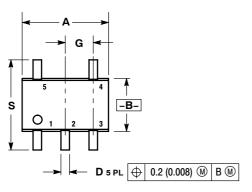
# **DEVICE ORDERING INFORMATION**

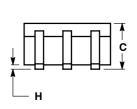
Device Order Number	Package Type	Tape and Reel Size <sup>†</sup>
MC74VHC1GT86DFT1	SC-88A / SOT-353 / SC-70	3000 / Tape & Reel
M74VHC1GT86DFT1G	SC-88A / SOT-353 / SC-70 (Pb-Free)	3000 / Tape & Reel
MC74VHC1GT86DFT2	SC-88A / SOT-353 / SC-70	3000 / Tape & Reel
M74VHC1GT86DFT2G	SC-88A / SOT-353 / SC-70 (Pb-Free)	3000 / Tape & Reel
MC74VHC1GT86DTT1	TSOPS / SOT-23 / SC-59	3000 / Tape & Reel
M74VHC1GT86DTT1G	TSOPS / SOT-23 / SC-59 (Pb-Free)	3000 / Tape & Reel

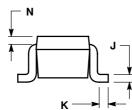
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **PACKAGE DIMENSIONS**

SC-88A, SOT-353, SC-70 CASE 419A-02 **ISSUE J** 







- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

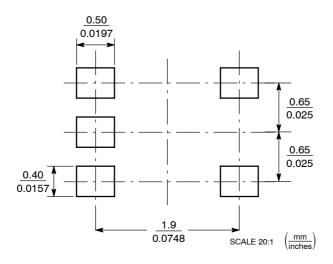
  2. CONTROLLING DIMENSION: INCH.

  3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.

  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65 BSC	
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20	REF
S	0.079	0.087	2.00	2.20

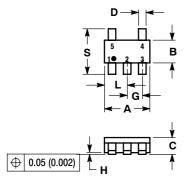
# **SOLDERING FOOTPRINT\***

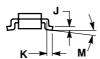


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

TSOP-5/SOT-23/SC-59 CASE 483-02 ISSUE D



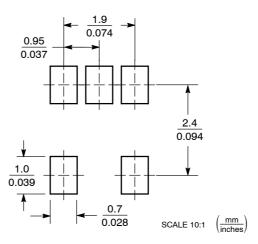


#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.1142	0.1220
В	1.30	1.70	0.0512	0.0669
С	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
Н	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
Κ	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
М	0 °	10°	0°	10°
s	2.50	3.00	0.0985	0.1181

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice on semiconductor and are registered readerlands of semiconductor Components industries, Ite (SCILLC) solicit esserves the right to make changes without further holice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative