MMBT4124LT1

General Purpose Transistor

NPN Silicon

Features

- Pb−Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	25	Vdc
Collector−Base Voltage	V_{CBO}	30	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	200	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) @T_A = 25°C Derate above 25°C	P_D	 225 1.8	 W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate (Note 2) @T_A = 25°C Derate above 25°C	P_D	 300 2.4	 W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

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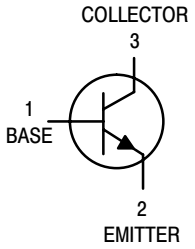
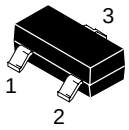
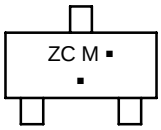




SOT−23 (TO−236)
CASE 318
STYLE 6

MARKING DIAGRAM



ZC = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping
MMBT4124LT1	SOT−23	3000 / Tape & Reel
MMBT4124LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CEO}$	25	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	30	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	−	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	−	50	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	−	50	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	 120 60	 360 −	−
Collector−Emitter Saturation Voltage (Note 3) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	−	0.3	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	−	0.95	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	300	−	MHz
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	−	8.0	pF
Collector−Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 1.0 MHz)	C_{cb}	−	4.0	pF
Small−Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_S = 10 k Ω, f = 1.0 kHz)	h_{fe}	120	480	−
Current Gain − High Frequency (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	$\|h_{fe}\|$	 3.0 120	 − 480	−
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	NF	−	5.0	dB

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

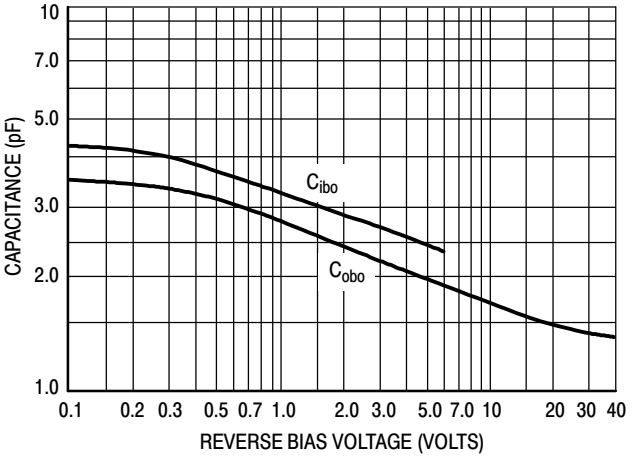


Figure 1. Capacitance

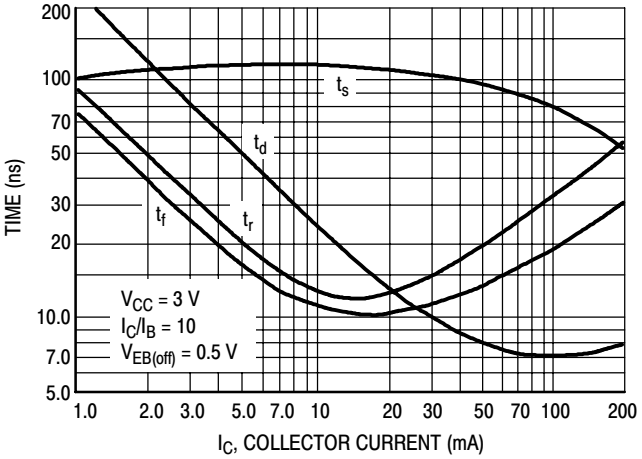


Figure 2. Switching Times

AUDIO SMALL−SIGNAL CHARACTERISTICS

NOISE FIGURE

(V_{CE} = 5 Vdc, T_A = 25°C)

Bandwidth = 1.0 Hz

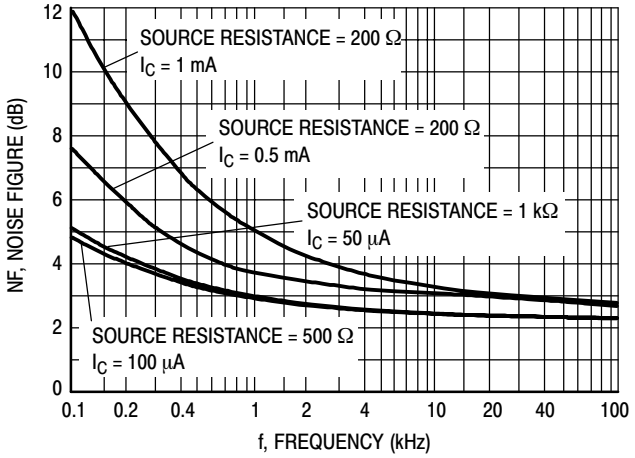


Figure 3. Frequency Variations

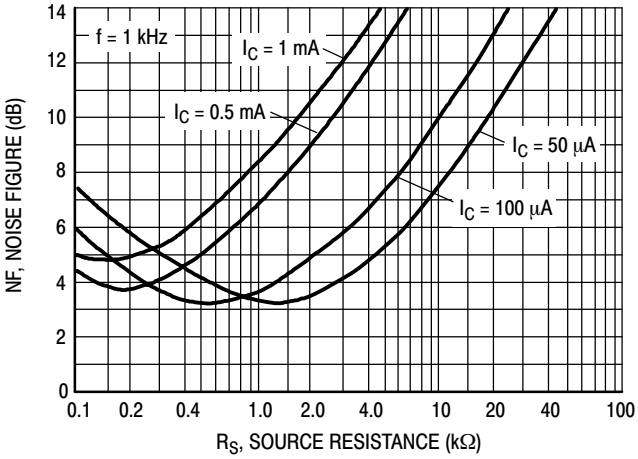


Figure 4. Source Resistance

h PARAMETERS

(V_{CE} = 10 V, f = 1 kHz, T_A = 25°C)

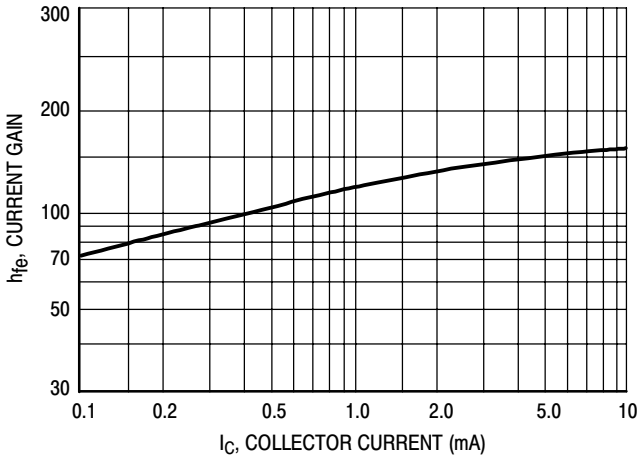


Figure 5. Current Gain

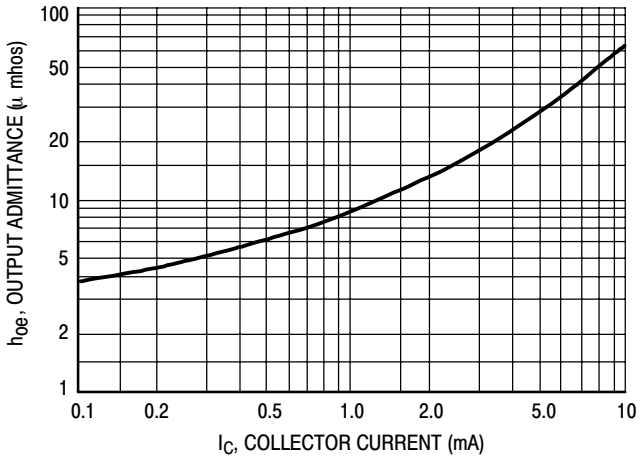


Figure 6. Output Admittance

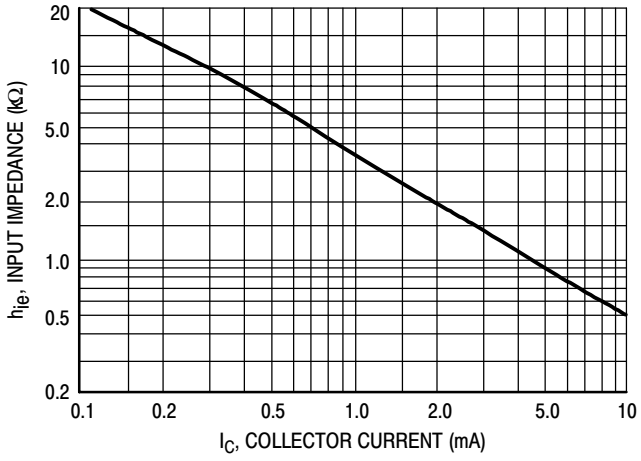


Figure 7. Input Impedance

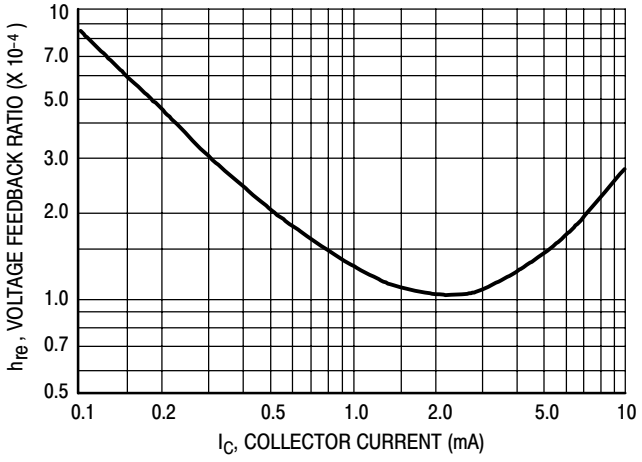


Figure 8. Voltage Feedback Ratio

STATIC CHARACTERISTICS

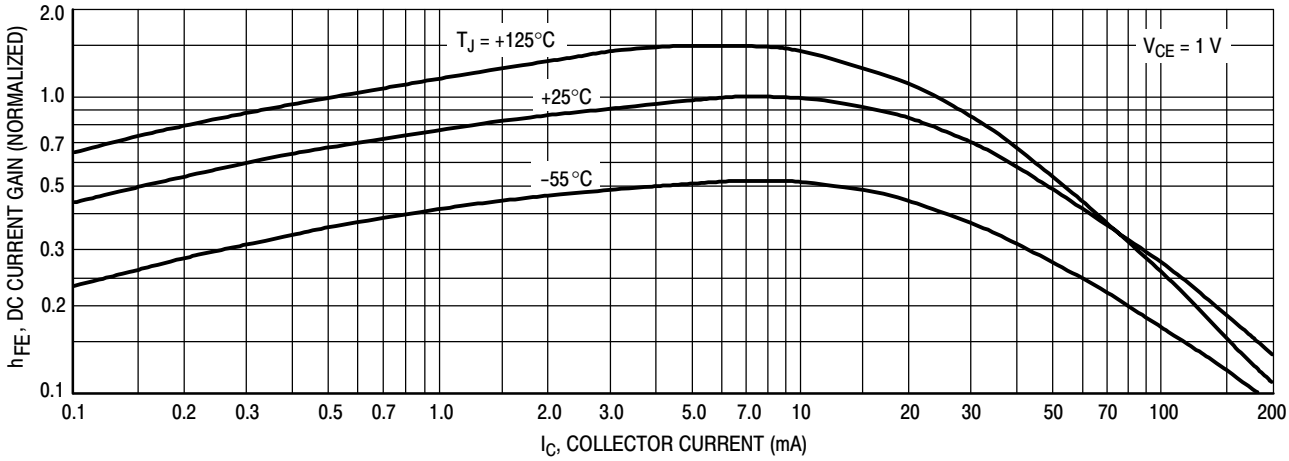


Figure 9. DC Current Gain

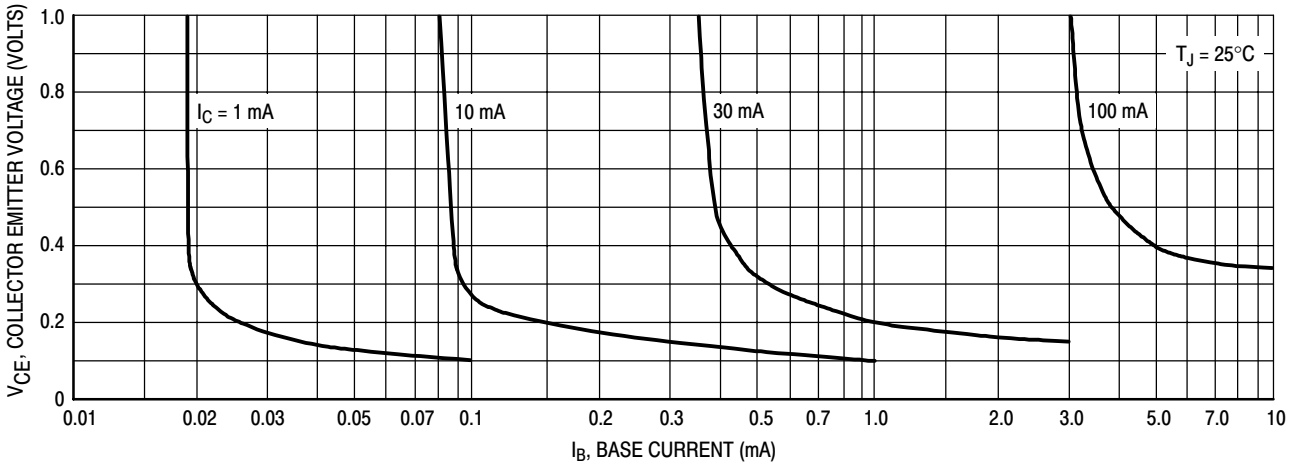


Figure 10. Collector Saturation Region

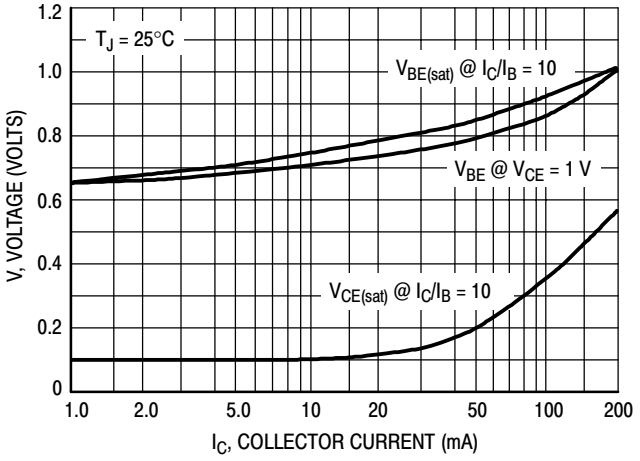


Figure 11. “On” Voltages

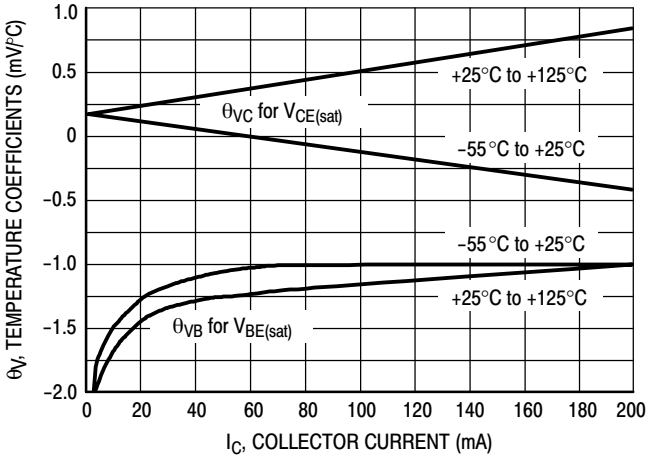
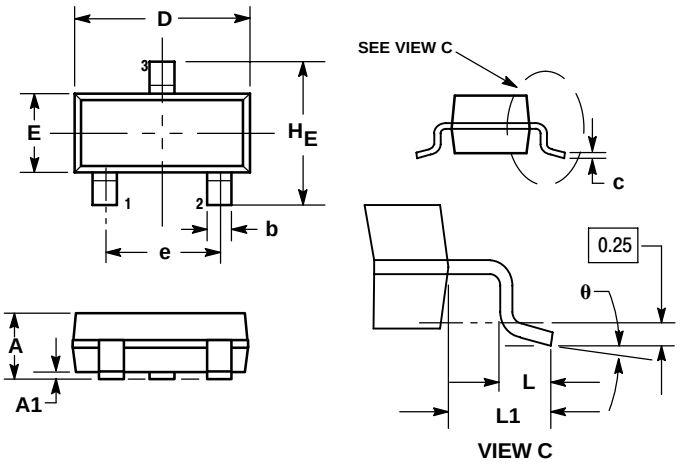


Figure 12. Temperature Coefficients

MMBT4124LT1

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

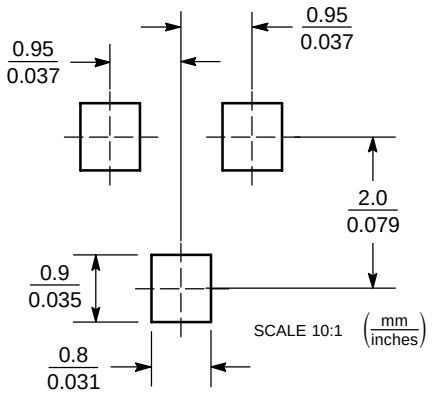


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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