

NLX1G11

3-Input AND Gate

The NLX1G11 is an advanced high-speed 3-input CMOS AND gate in ultra-small footprint.

The NLX1G11 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 2.4 \text{ ns}$ (Typ) @ $V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- 24 mA Balanced Output Source and Sink Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra-Small Packages
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

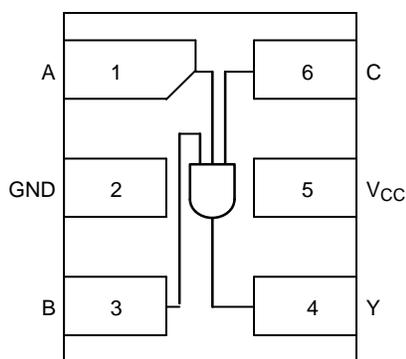


Figure 1. Pinout (Top View)

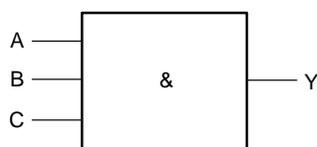


Figure 2. Logic Symbol

PIN ASSIGNMENT

Pin	Function
1	A
2	GND
3	B
4	Y
5	V_{CC}
6	C

FUNCTION TABLE

Input			Output
A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

H – HIGH Logic Level

L – LOW Logic Level

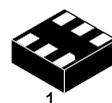
X = Either LOW or HIGH Logic Level



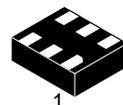
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS



ULLGA6
1.0 x 1.0
CASE 613AD



ULLGA6
1.2 x 1.0
CASE 613AE



ULLGA6
1.45 x 1.0
CASE 613AF



UDFN6
1.0 x 1.0
CASE 517BX



UDFN6
1.2 x 1.0
CASE 517AA



UDFN6
1.45 x 1.0
CASE 517AQ



X = Device Marking

M = Date Code

▪ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NLX1G11

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	-50	mA
I _O	DC Output Source/Sink Current	±50	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	150	°C
θ _{JA}	Thermal Resistance (Note 1)	496	°C/W
P _D	Power Dissipation in Still Air @ 85°C	252	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125 °C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _{IN}	Digital Input Voltage (Note 6)	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 1.8 V ± 0.15 V V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Unused inputs may not be left open. All inputs must be tied to a high or low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Low-Level Input Voltage		1.65	0.75 x V _{CC}			0.75 x V _{CC}		V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65			0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 – 5.5			0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -100 μA	1.65 – 5.5	V _{CC} -0.1	V _{CC}		V _{CC} -0.1		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA	1.65	1.29	1.52		1.29		
		I _{OH} = -8 mA	2.3	1.9	2.15		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.8		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.68		2.3		
I _{OH} = -32 mA	4.5	3.8	4.2		3.8				
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 100 μA	1.65 – 5.5			0.1		0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA	1.65		0.08	0.24		0.24	
		I _{OH} = 8 mA	2.3		0.1	0.3		0.3	
		I _{OH} = 12 mA	2.7		0.12	0.4		0.4	
		I _{OH} = 16 mA	3.0		0.15	0.4		0.4	
		I _{OH} = 24 mA	3.0		0.22	0.55		0.55	
		I _{OH} = 32 mA	4.5		0.22	0.55		0.55	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5V	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Power-Off Output Leakage Current	V _{IN} or V _{OUT} = 5.5 V	0			1.0		10	μA
I _{CC}	Quiescent Supply Current	0 ≤ V _{IN} ≤ V _{CC}	5.5			1.0		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 2.5 nS)

Symbol	Parameter	V _{CC} (V)	Test Condition	T _A = 25 °C			T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	1.65–1.95	R _L = 1 MΩ, C _L = 15 pF	2.0	5.5	18.5	2.0	19	ns
		2.3–2.7	R _L = 1 MΩ, C _L = 15 pF	0.8	3.0	11	0.8	11.5	
		3.0–3.6	R _L = 1 MΩ, C _L = 15 pF	0.5	2.6	7.5	0.5	8.0	
			R _L = 500 Ω, C _L = 50 pF	1.5	3.0	8.5	1.5	9.0	
		4.5–5.5	R _L = 1 MΩ, C _L = 15 pF	0.5	2.2	5.5	0.5	6.0	
			R _L = 500 Ω, C _L = 50 pF	0.8	2.4	7.0	0.8	7.5	
C _{IN}	Input Capacitance	5.5	V _{IN} = 0 V or V _{CC}		4.0				pF
C _{PD}	Power Dissipation Capacitance (Note 7)	3.3	10 MHz		20				pF
		5.5	V _{IN} = 0 V or V _{CC}		26				

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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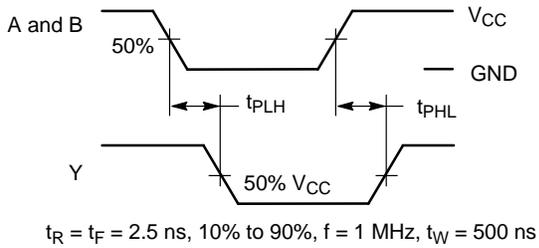
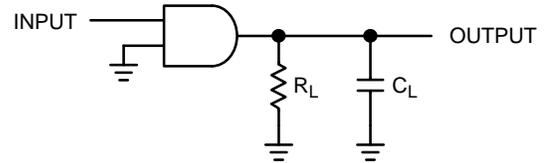


Figure 3. Switching Waveforms



A 1 MHz square input wave is recommended for propagation delay tests

Figure 4. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
NLX1G11AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G11BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G11CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel
NLX1G11MUTCG (In Development)	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G11AMUTCG	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLVX1G11AMUTCG*	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G11CMUTCG	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

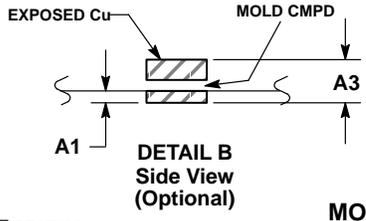
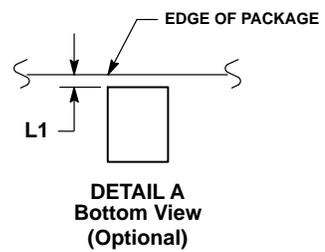
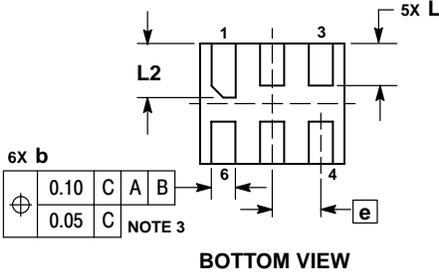
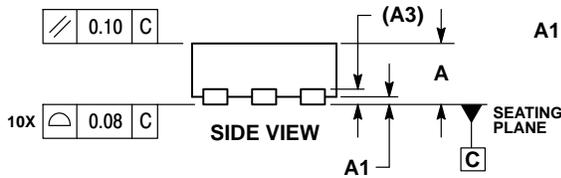
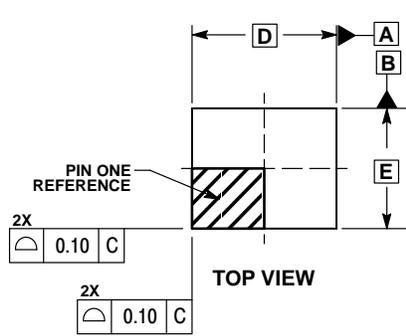
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

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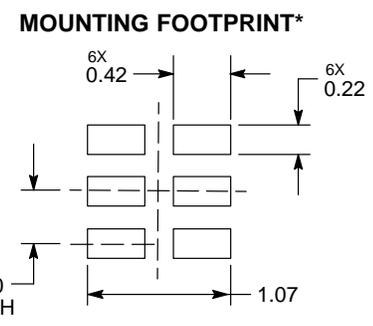
PACKAGE DIMENSIONS

UDFN6 1.2x1.0, 0.4P
CASE 517AA
ISSUE D



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
D	1.20	BSC
E	1.00	BSC
e	0.40	BSC
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50



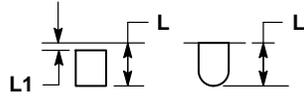
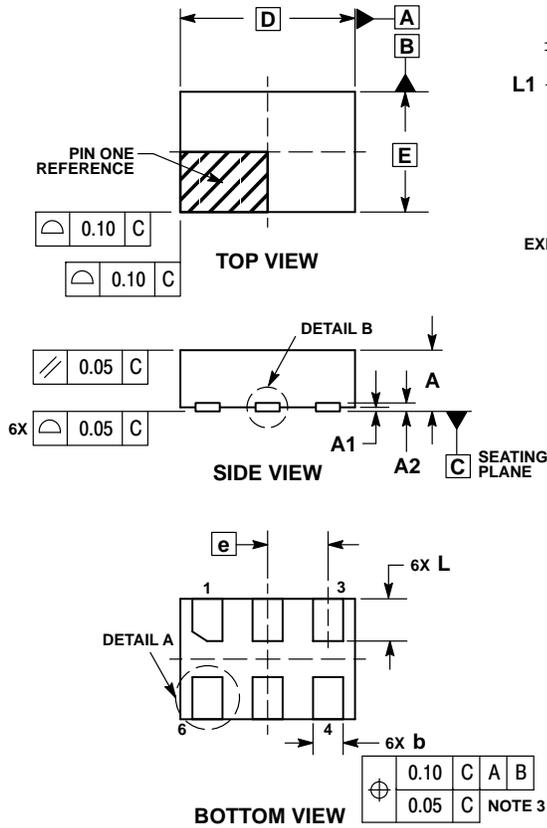
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

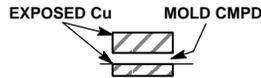
NLX1G11

PACKAGE DIMENSIONS

UDFN6 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O



DETAIL A
OPTIONAL
CONSTRUCTIONS



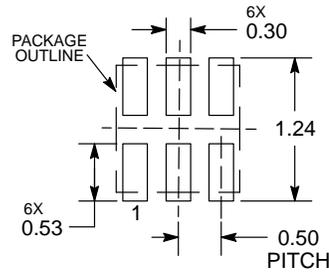
DETAIL B
OPTIONAL
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



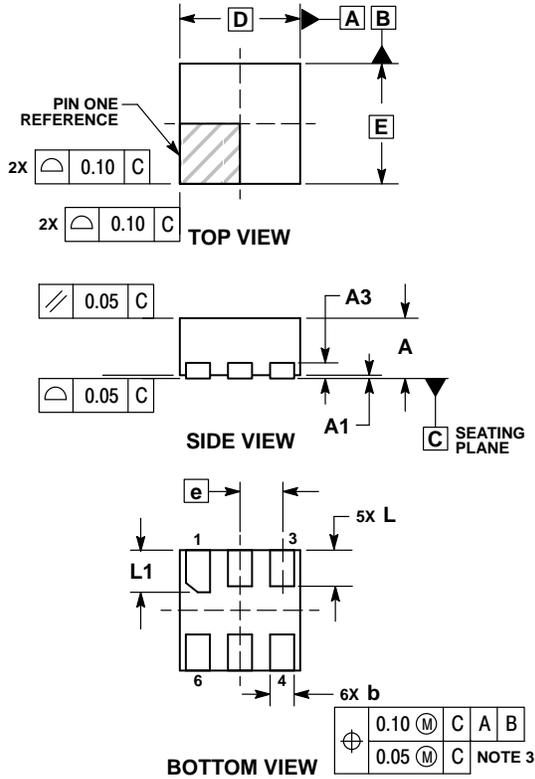
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G11

PACKAGE DIMENSIONS

UDFN6 1.0x1.0, 0.35P
CASE 517BX
ISSUE O

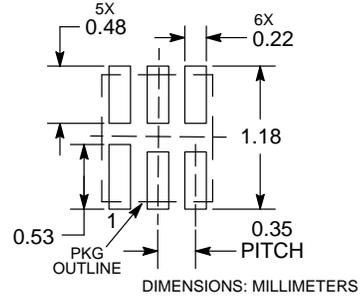


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

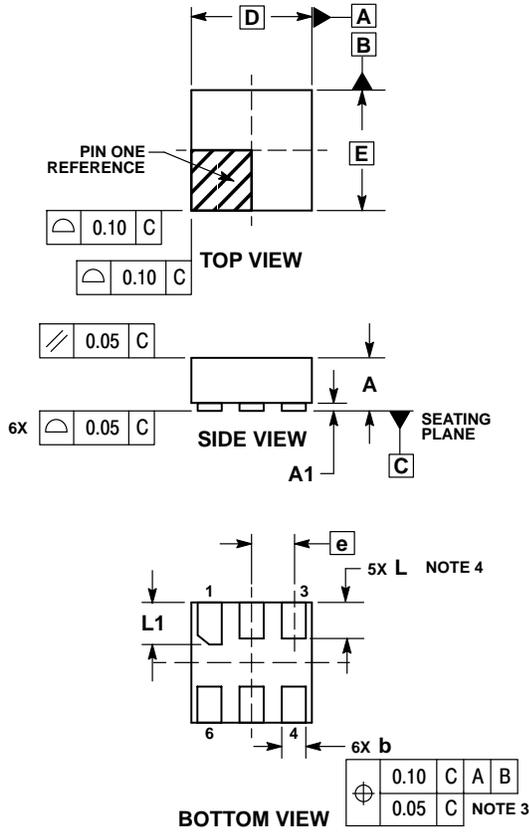


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G11

PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P
CASE 613AD
ISSUE A

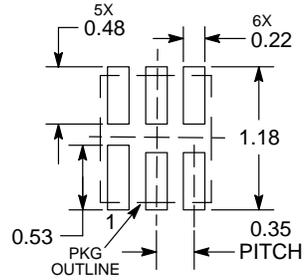


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



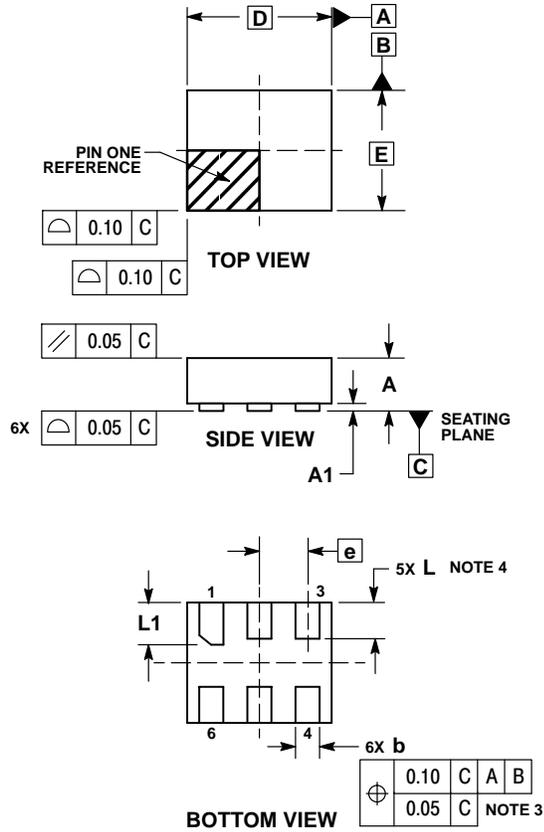
DIMENSIONS: MILLIMETERS

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NLX1G11

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P
CASE 613AE
ISSUE A

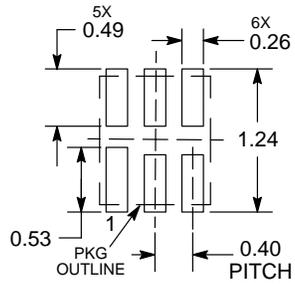


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MILLIMETERS			
DIM	MIN	MAX	
A	---	0.40	
A1	0.00	0.05	
b	0.15	0.25	
D	1.20 BSC		
E	1.00 BSC		
e	0.40 BSC		
L	0.25	0.35	
L1	0.35	0.45	

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



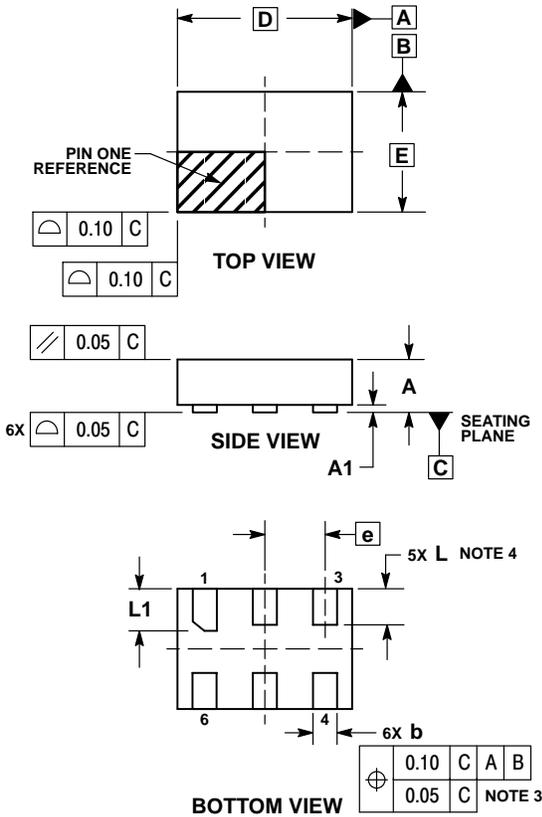
DIMENSIONS: MILLIMETERS

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NLX1G11

PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P
CASE 613AF
ISSUE A

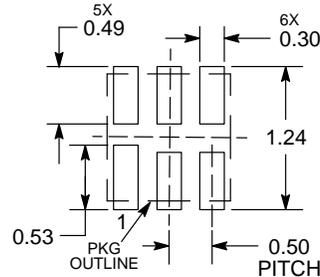


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MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

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