- **Member of the Texas Instruments Widebus™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Pin-to-Pin Compatible With SN74ACT7882, SN74ACT7884, and SN74ACT7811**

- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Expandable in Word Width and/or Word Depth**
- **Fast Access Times of 11 ns With a 50-pF Load**
- **High Output Drive for Direct Bus Interface**
- **Package Options Include 68-Pin Plastic Leaded Chip Carrrier (FN) or 80-Pin Shrink Quad Flat (PN) Package**

FN PACKAGE
(TOP VIEW)

Top pins (left to right): D15 (9), D16 (8), D17 (7), GND (6), RDCLK (5), RDEN1 (4), RDEN2 (3), OE (2), RESET (1), V_CC (68), GND (67), OR (66), V_CC (65), Q17 (64), Q16 (63), GND (62), Q15 (61)

Left pins (top to bottom): D14 (10), D13 (11), D12 (12), D11 (13), D10 (14), D9 (15), V_CC (16), D8 (17), GND (18), D7 (19), D6 (20), D5 (21), D4 (22), D3 (23), D2 (24), D1 (25), D0 (26)

Right pins (top to bottom): V_CC (60), Q14 (59), Q13 (58), GND (57), Q12 (56), Q11 (55), V_CC (54), Q10 (53), Q9 (52), GND (51), Q8 (50), Q7 (49), V_CC (48), Q6 (47), Q5 (46), GND (45), Q4 (44)

Bottom pins (left to right): DAF (27), GND (28), WRTCLK (29), WRTEN1 (30), WRTEN2 (31), V_CC (32), AF/AE (33), GND (34), IR (35), HF (36), V_CC (37), Q0 (38), Q1 (39), GND (40), Q2 (41), Q3 (42), V_CC (43)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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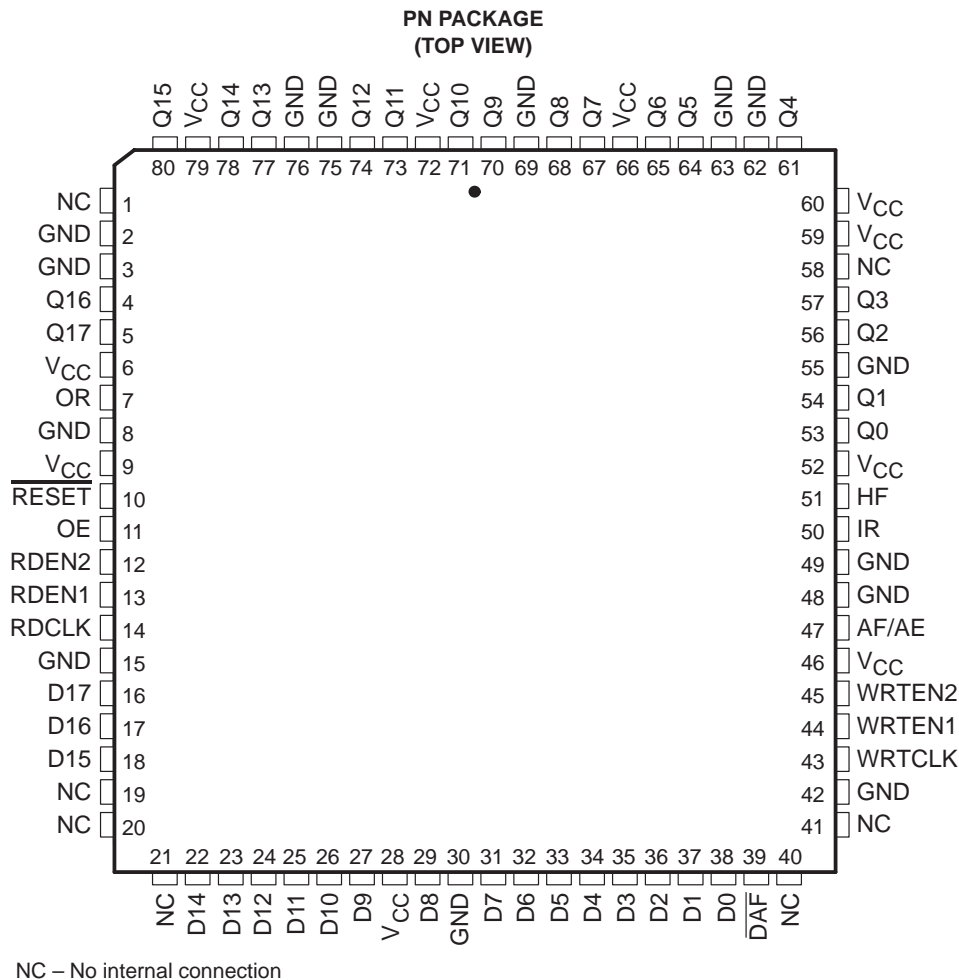
TEXAS INSTRUMENTS

SN74ACT7881
1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY

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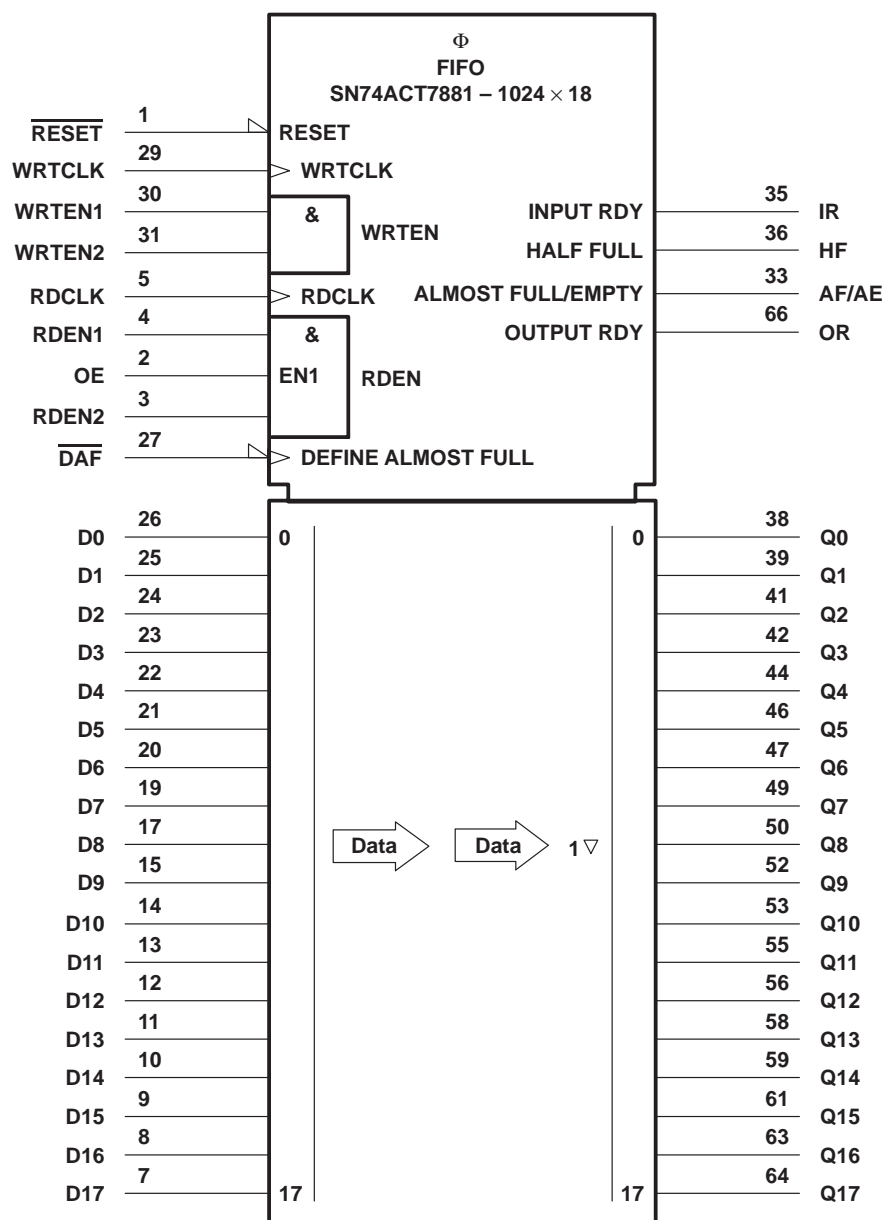**PN PACKAGE**
(TOP VIEW)

Top pins (left to right, 80–61): Q15, V_CC, Q14, Q13, GND, GND, Q12, Q11, V_CC, Q10, Q9, GND, Q8, Q7, V_CC, Q6, Q5, GND, GND, Q4

Left side (pins 1–20):
Pin	Signal
1	NC
2	GND
3	GND
4	Q16
5	Q17
6	V_CC
7	OR
8	GND
9	V_CC
10	RESET
11	OE
12	RDEN2
13	RDEN1
14	RDCLK
15	GND
16	D17
17	D16
18	D15
19	NC
20	NC

Right side (pins 60–41):
Pin	Signal
60	V_CC
59	V_CC
58	NC
57	Q3
56	Q2
55	GND
54	Q1
53	Q0
52	V_CC
51	HF
50	IR
49	GND
48	GND
47	AF/AE
46	V_CC
45	WRTEN2
44	WRTEN1
43	WRTCLK
42	GND
41	NC

Bottom pins (left to right, 21–40): NC, D14, D13, D12, D11, D10, D9, V_CC, D8, GND, D7, D6, D5, D4, D3, D2, D1, D0, $\overline{\text{DAF}}$, NC

NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7881 is organized as 1024 × 18 bits. The SN74ACT7881 processes data at rates up to 67 MHz and access times of 11 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is accomplished easily in both word width and word depth.

The SN74ACT7881 has normal input-bus to output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

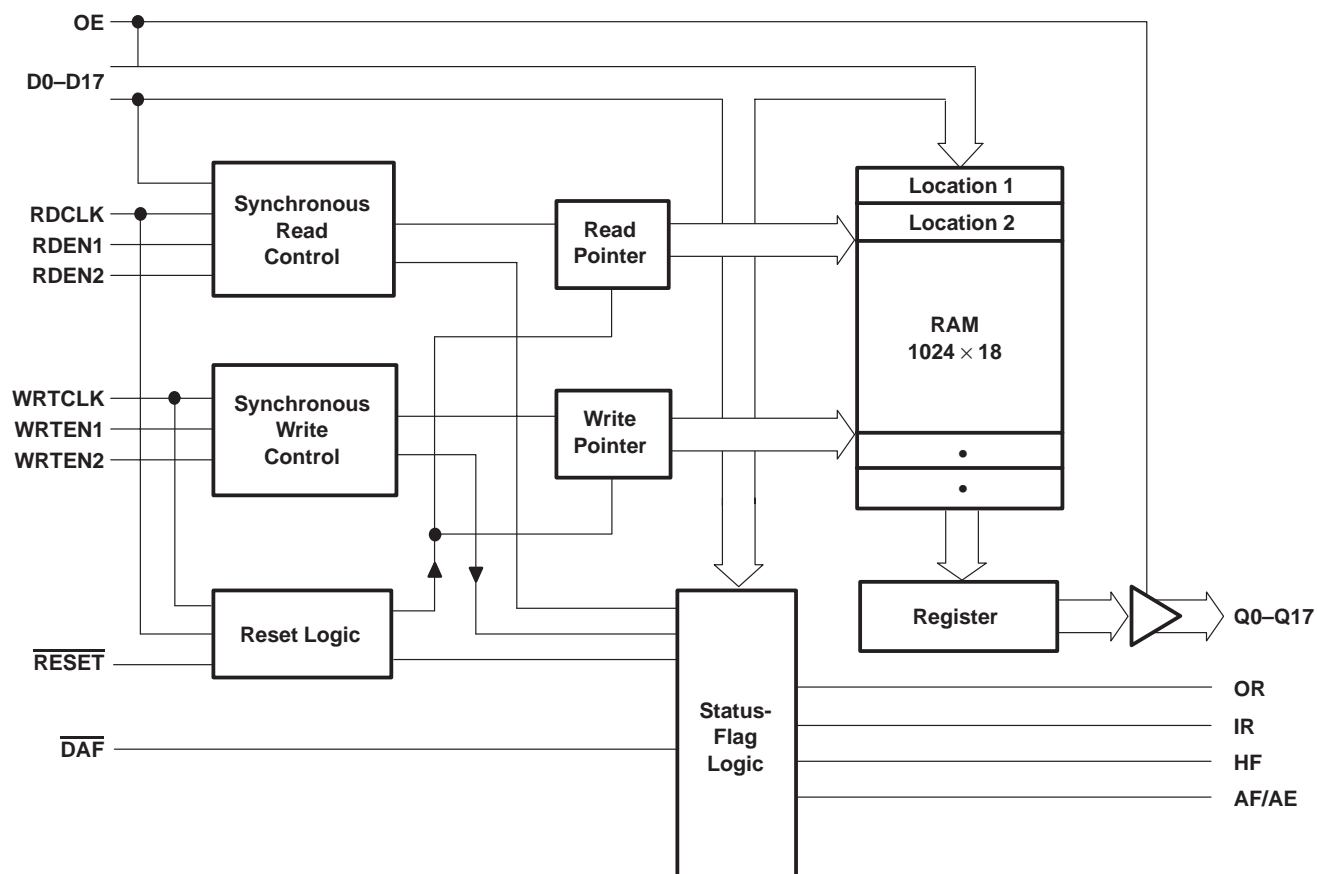The SN74ACT7881 is characterized for operation from 0°C to 70°C.

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram

Terminal Functions

TERMINAL†		I/O	DESCRIPTION
NAME	NO.		
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the AF/AE offset value (X). This value can be programmed during reset, or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or fewer words or (1025 – X) or more words. AF/AE is low when the FIFO contains between (X + 2) and (1024 – X) words. Programming procedure for AF/AE – The AF/AE flag is programmed during each reset cycle. The AF/AE offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: **User-defined X** Step 1: Take DAF from high to low. Step 2: If RESET is not already low, take RESET low. Step 3: With DAF held low, take RESET high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep DAF low. **Default X** To redefine AF/AE using the default value of X = 256, hold DAF high during the reset cycle.
DAF	27	I	Define-almost-full. The high-to-low transition of DAF stores the binary value of data inputs as the AF/AE offset value (X). With DAF held low, a low pulse on RESET defines the AF/AE flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition of DAF captures data for the AF/AE offset (X) from D8–D0.
HF	36	O	Half-full flag. HF is high when the FIFO contains 512 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after RESET goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The Q0–Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when the FIFO is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on the low-to-high transition of RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR also is driven synchronously with respect to the RDCLK signal.
RDEN1 RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
RESET	1	I	Reset. A reset is accomplished by taking RESET low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low, and AF/AE is high. The FIFO must be reset upon power up. With DAF at a low level, a low pulse on RESET defines AF/AE using the AF/AE offset value (X), where X is the value previously stored. With DAF at a high level, a low-level pulse on RESET defines the AF/AE flag using the default value of X = 256.
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR also is driven synchronously with respect to WRTCLK.
WRTEN1 WRTEN2	30 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the AF/AE offset value (X).

† Terminals listed are for the FN package.

Store the Value of Data as X

Define the AF/AE Flag Using the Programmed Value of X
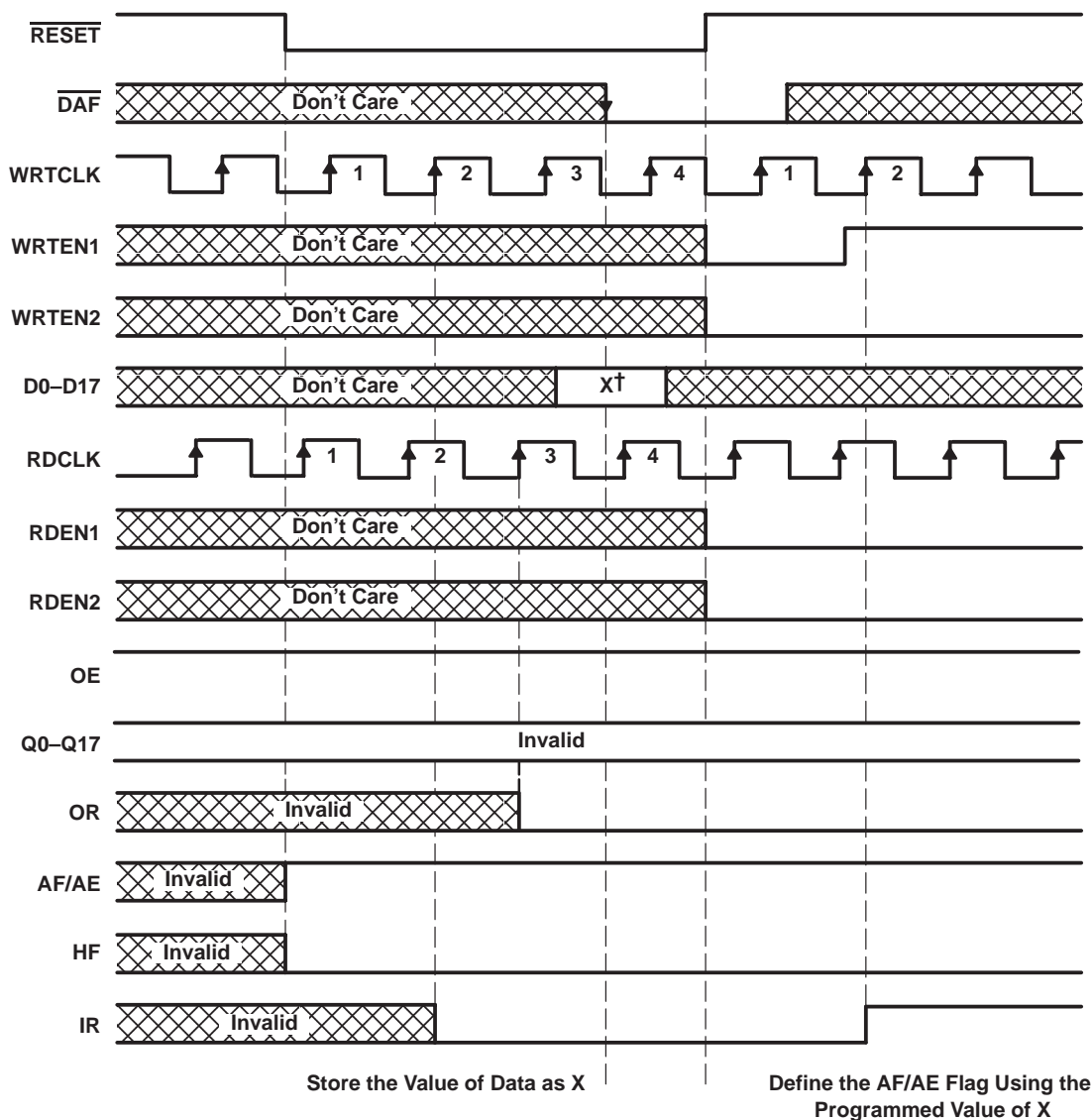
† X is the binary value on D8–D0.

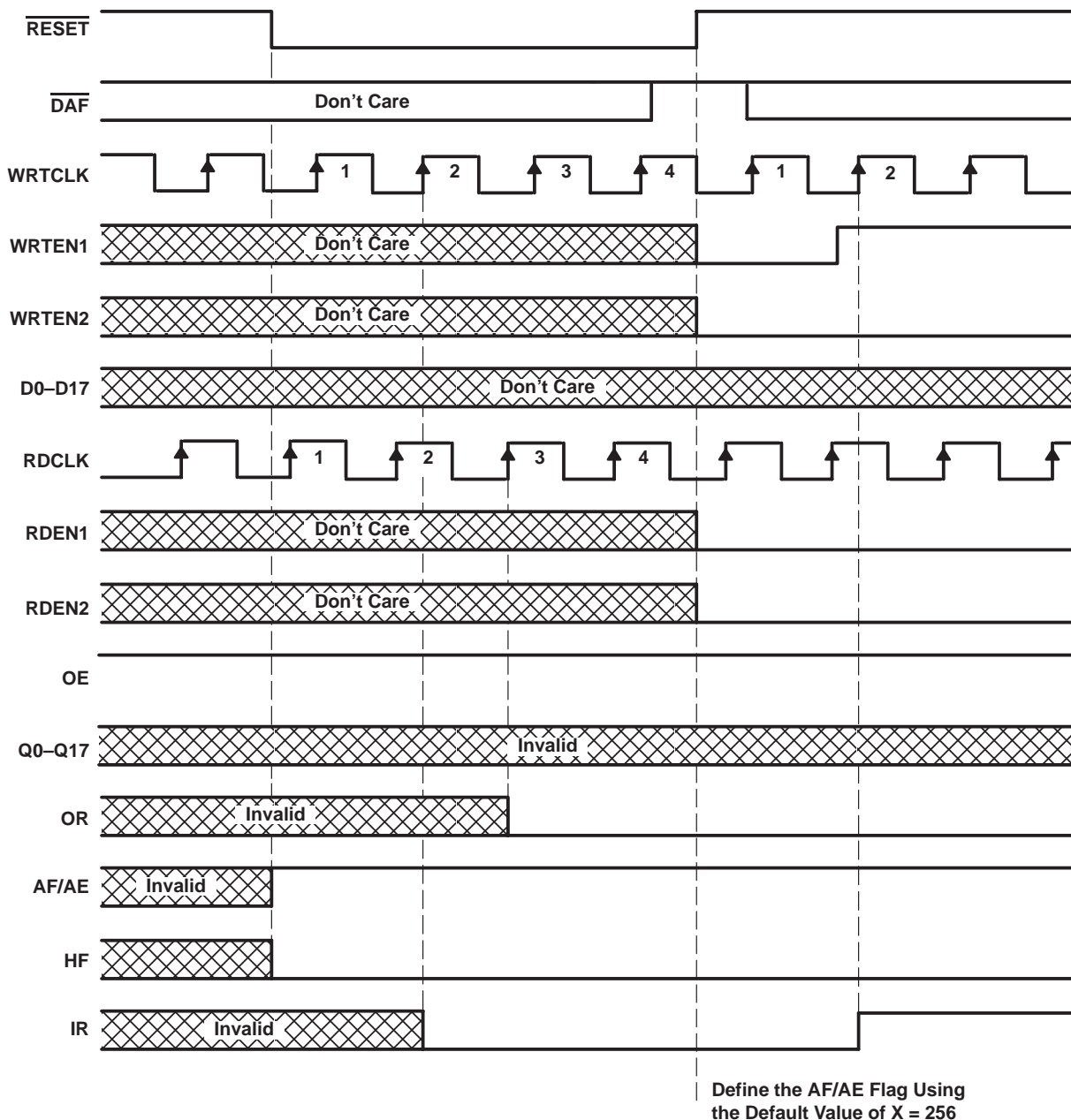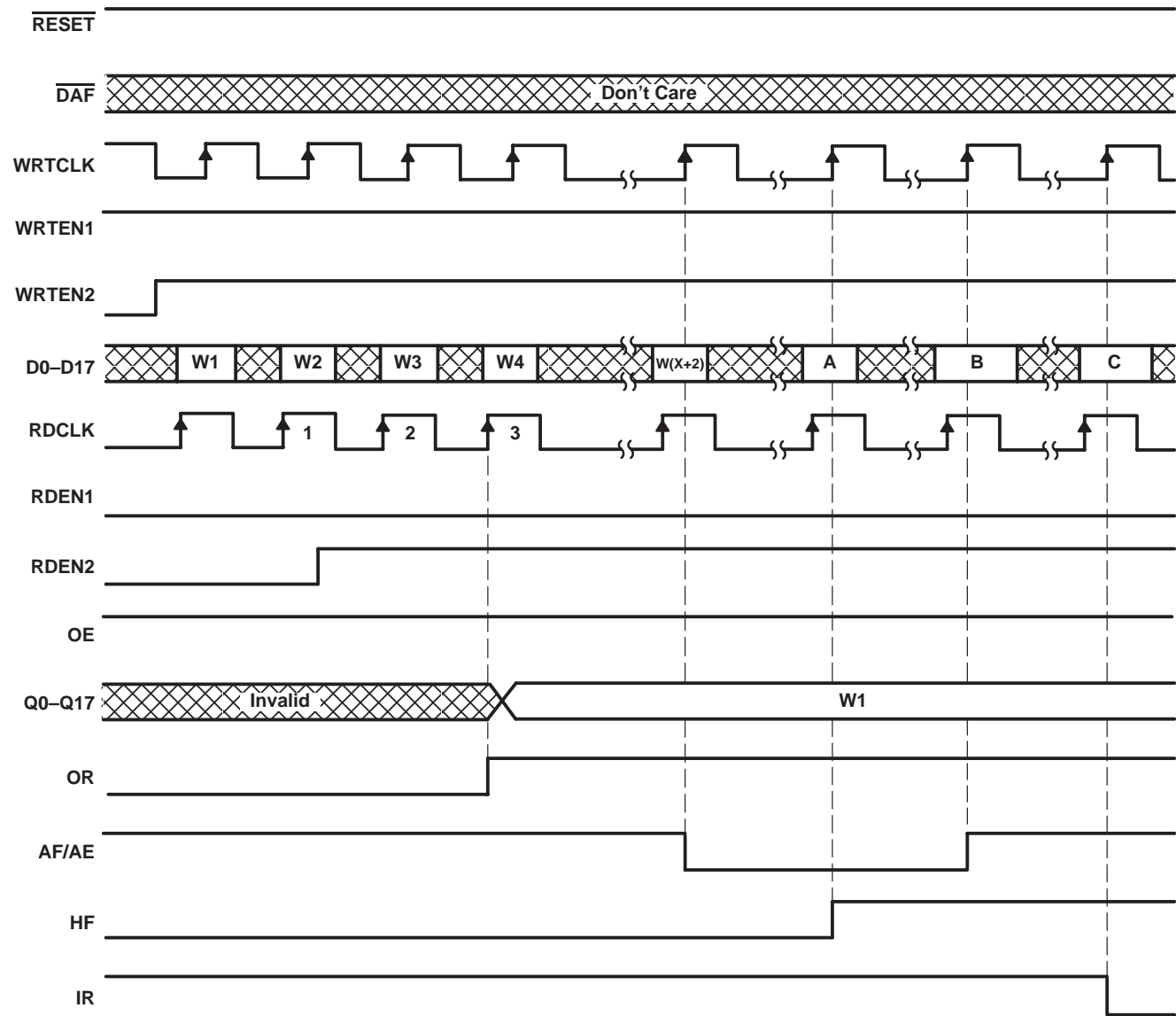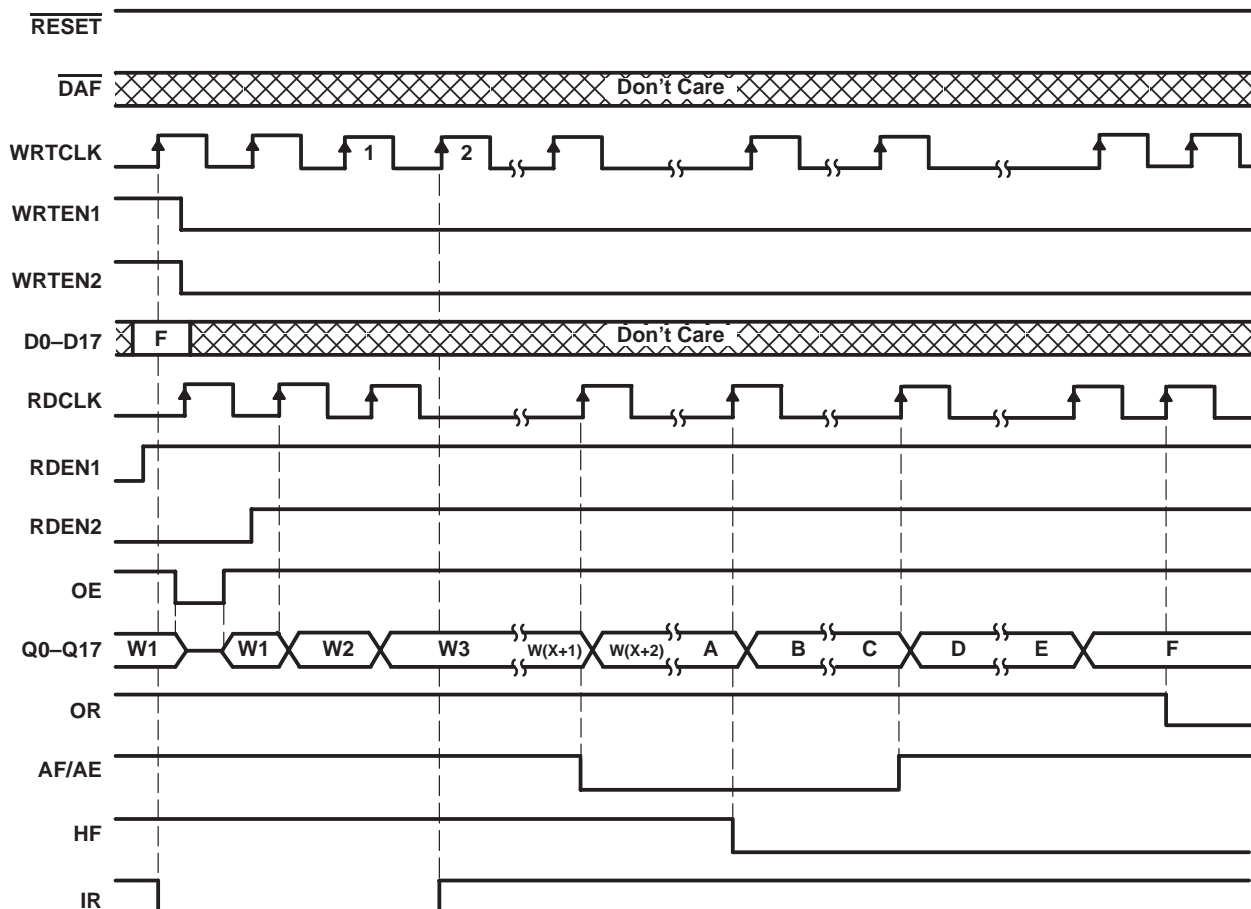**Figure 1. Reset Cycle: Define AF/AE Flag Using a Programmed Value of X**

Figure 2. Reset Cycle: Define AF/AE Flag Using the Default Value of X = 256

DATA-WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	B	C
W513	W(1025 – X)	W1025

Figure 3. Write Cycle

DATA-WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	B	C	D	E	F
W513	W514	W(1024 – X)	W(1025 – X)	W1024	W1025

Figure 4. Read Cycle

SN74ACT7881
1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I .... −0.5 V to 7 V
Voltage range applied to a disabled 3-state output .... −0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): FN package .... 39°C/W
PN package .... 62°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:   The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	μA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	μA
I_{CC}§	V_I = V_{CC} − 0.2 V or 0				400	μA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1.2	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_O	V_O = 0,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} is tested with outputs open.

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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 5)

		'ACT7881-15		'ACT7881-20		'ACT7881-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		33.4	MHz
t_w	Pulse duration	WRTCLK high						
		WRTCLK high	5		7		8.5		ns
		WRTCLK low	7		7		11		
		RDCLK high	5		7		8.5		
		RDCLK low	7		7		11		
		$\overline{DAF}$ high	7		7		10		
t_{su}	Setup time	D0–D17 before WRTCLK↑	5		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	4		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	4		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		7		
		Define AF/AE: D0–D8 before $\overline{DAF}$↓	3		5		5		
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	3		6		7		
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	4		5		5		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		0		0		
		OE, RDEN1, RDEN2 high after RDCLK↑	0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	0		0		0		
		Define AF/AE: D0–D8 after $\overline{DAF}$↓	0		0		0		
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		0		0		
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	0		0		0		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7881-15		'ACT7881-20		'ACT7881-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67		50		33.4		MHz
t_{pd}	RDCLK↑	Any Q	3	12	3	13	3	18	ns
t_{pd}‡	RDCLK↑	Any Q							ns
t_{pd}	WRTCLK↑	IR	2	8	2	9.5	2	12	ns
	RDCLK↑	OR	2	8	2	9.5	2	12	
	WRTCLK↑	AF/AE	6	17	6	19	6	22	
	RDCLK↑		6	17	6	19	6	22	
t_{PLH}	WRTCLK↑	HF	6	14	6	17	6	21	ns
t_{PHL}	RDCLK↑	HF	6	14	6	17	6	21	ns
t_{PLH}	$\overline{RESET}$↓	AF/AE	3	12	3	17	3	21	ns
t_{PHL}	$\overline{RESET}$↓	HF	3	14	3	19	3	23	ns
t_{en}	OE	Any Q	2	9	2	11	2	11	ns
t_{dis}	OE	Any Q	2	10	2	14	2	14	ns

‡ This parameter is measured with C_L = 30 pF (see Figure 6).

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operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

PARAMETER MEASUREMENT INFORMATION

PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open

LOAD CIRCUIT

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTE A: C_L includes probe and jig capacitance.
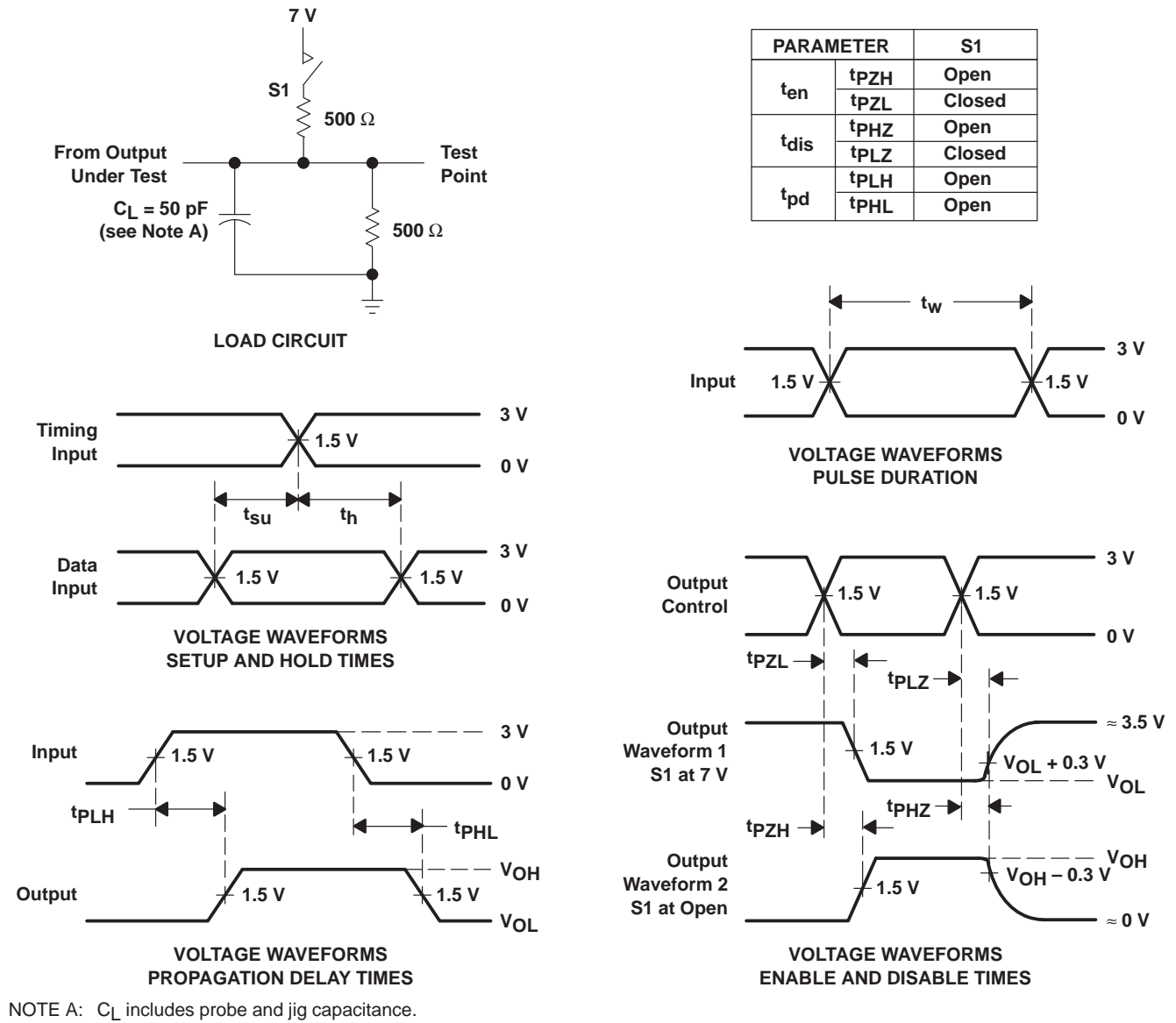
Figure 5. Load Circuit and Voltage Waveforms

TEXAS
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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE
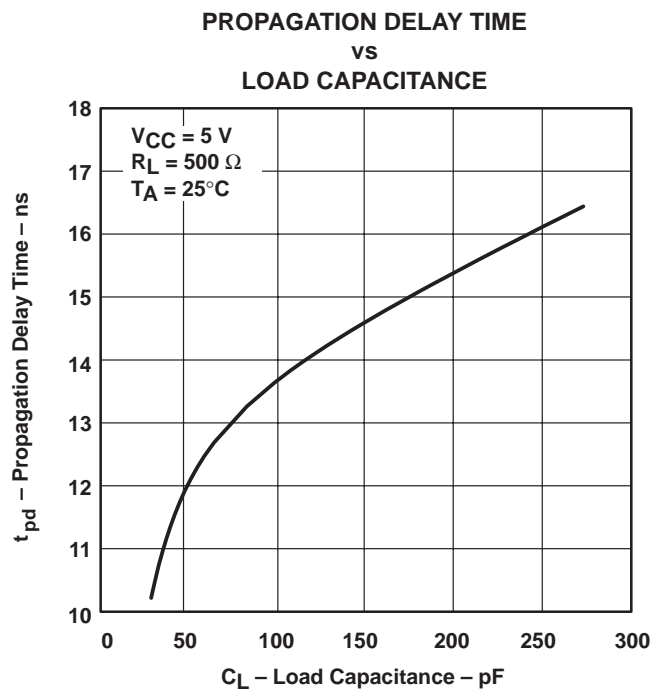
Figure 6

APPLICATION INFORMATION

expanding the SN74ACT7881

The SN74ACT7881 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 8 shows two SN74ACT7881 devices configured for word-depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready (OR) flag of the previous device and the input-ready (IR) flag of the next device maintain data flow to the last device in the chain whenever space is available.

Figure 9 shows two SN74ACT7881 devices in word-width expansion. Word-width expansion is accomplished by simply connecting all common control signals between the devices and creating composite IR and OR signals. The almost-full/almost-empty (AF/AE) flag and half-full (HF) flag can be sampled from any one device. Word-depth expansion and word-width expansion can be used together.
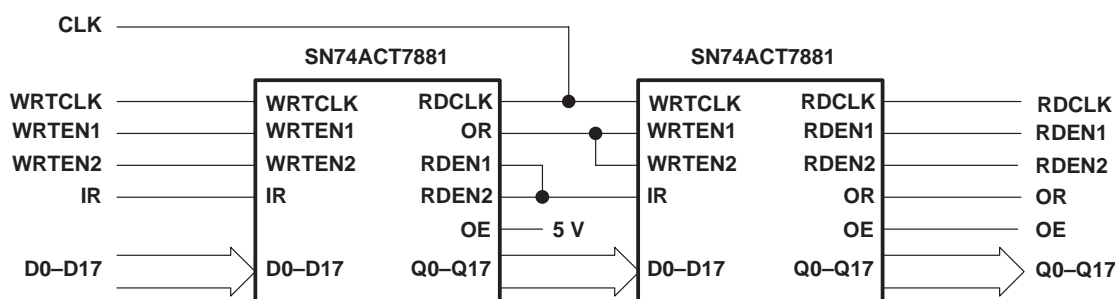
Figure 7. Word-Depth Expansion: 2048/4096/8192 × 18 Bits, N = 2
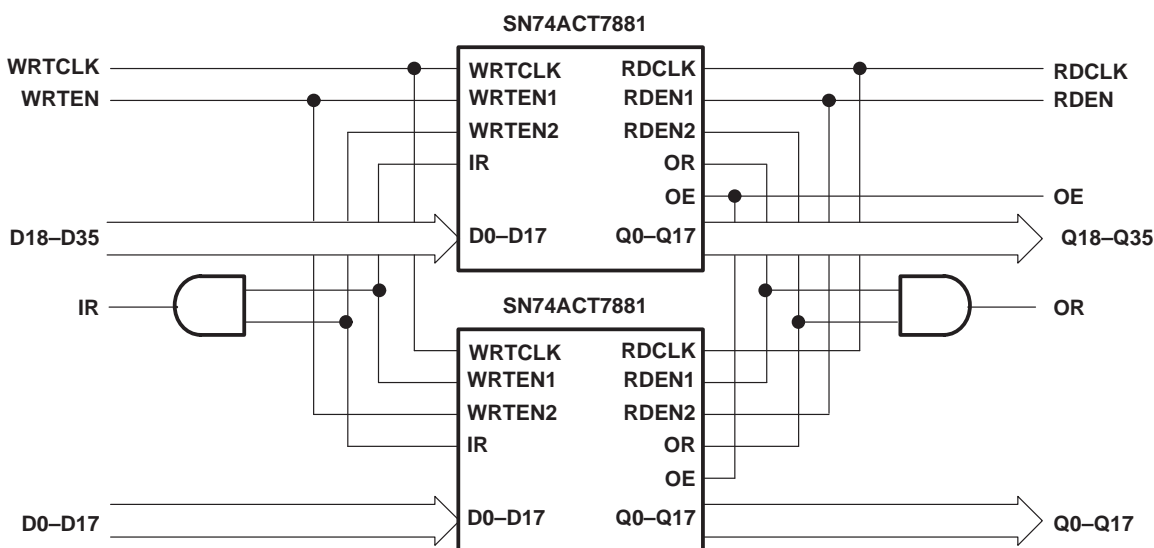
Figure 8. Word-Width Expansion: 1024 × 36 Bits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT7881-15FN	ACTIVE	PLCC	FN	68	18	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	SN74 ACT7881-15FN	Samples
SN74ACT7881-15PN	LIFEBUY	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	ACT7881-15	
SN74ACT7881-20FN	ACTIVE	PLCC	FN	68	18	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	SN74 ACT7881-20FN	Samples
SN74ACT7881-20PN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	ACT7881-20	Samples
SN74ACT7881-30PN	LIFEBUY	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	ACT7881-30	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74ACT7881 :

● Military: SN54ACT7881

NOTE: Qualified Version Definitions:

    ● Military - QML certified for Military and Defense Applications

FN (S-PQCC-J**)

20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER

Seating Plane

0.004 (0,10)

0.180 (4,57) MAX
0.120 (3,05)
0.090 (2,29)
0.020 (0,51) MIN

0.032 (0,81)
0.026 (0,66)

D2/E2

D2/E2

0.050 (1,27)

0.021 (0,53)
0.013 (0,33)

0.008 (0,20) NOM

⊕ 0.007 (0,18) Ⓜ

NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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1

PN (S-PQFP-G80)　　　　　　　　　　　　　　　　　　**PLASTIC QUAD FLATPACK**

4040135 / B 11/96
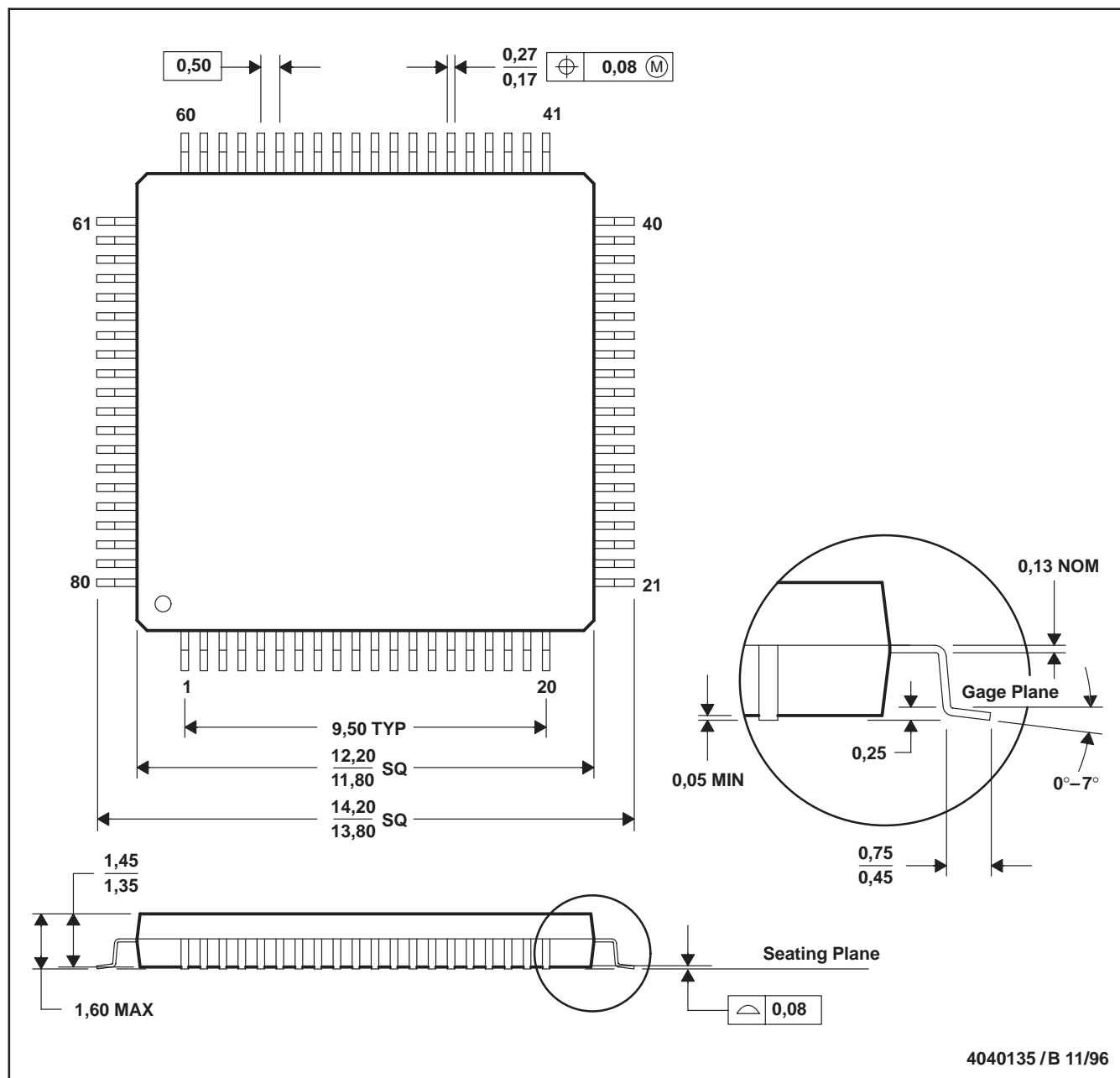
NOTES: A. All linear dimensions are in millimeters.
　　　　B. This drawing is subject to change without notice.
　　　　C. Falls within JEDEC MS-026

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