

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

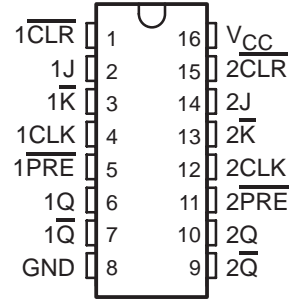
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS109A	50	6
'AS109A	129	29

## description

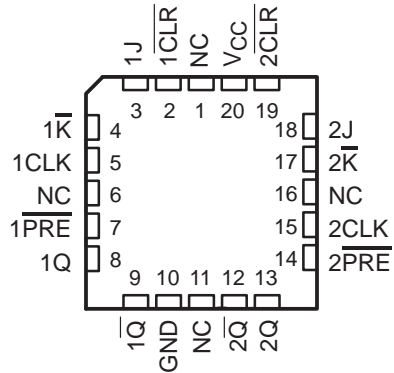
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the J and  $\overline{\text{K}}$  inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and  $\overline{\text{K}}$  inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\overline{\text{K}}$  and tying J high. They also can perform as D-type flip-flops if J and  $\overline{\text{K}}$  are tied together.

The SN54ALS109A and SN54AS109A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS109A and SN74AS109A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS109A, SN54AS109A ... J PACKAGE  
SN74ALS109A, SN74AS109A ... D OR N PACKAGE  
(TOP VIEW)



SN54ALS109A, SN54AS109A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{\text{Q}}0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{\text{Q}}0$

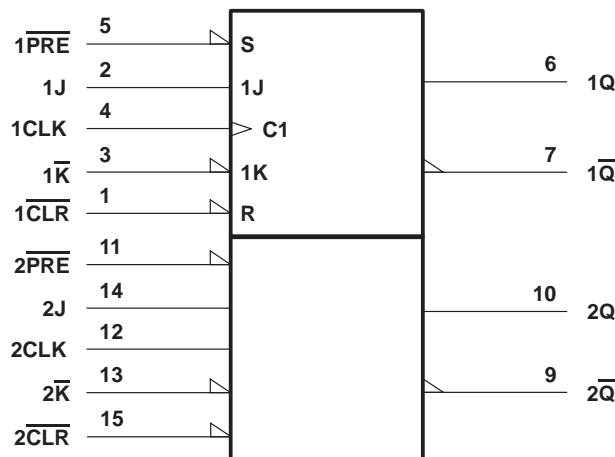
<sup>†</sup> The output levels in this configuration are not specified to meet the minimum levels for  $V_{OH}$  if the lows at  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS109A	–55°C to 125°C
SN74ALS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V <sub>IH</sub>	High-level input voltage		2			2			V		
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V		
I <sub>OH</sub>	High-level output current		−0.4			−0.4			mA		
I <sub>OL</sub>	Low-level output current		4			8			mA		
f <sub>clock</sub>	Clock frequency		0	30		0	34		MHz		
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	15			15			ns		
		CLK high	16.5			14.5					
		CLK low	16.5			14.5					
t <sub>su</sub>	Setup time before CLK↑	Data	15			15			ns		
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	10			10					
t <sub>h</sub>	Hold time after CLK↑	Data	0			0			ns		
T <sub>A</sub>	Operating free-air temperature		−55			125			0	70	°C

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS109A		SN74ALS109A		UNIT
			MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA	−1.5		−1.5		V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −0.4 mA	V <sub>CC</sub> − 2		V <sub>CC</sub> − 2		V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA		0.25 0.4		V
			I <sub>OL</sub> = 8 mA		0.35 0.5		
I <sub>I</sub>	CLK, J, or $\overline{K}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V	0.1		0.1		mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		0.2		0.2		
I <sub>IH</sub>	CLK, J, or $\overline{K}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20		20		μA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		40		40		
I <sub>IL</sub>	CLK, J, or $\overline{K}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	−0.2		−0.2		mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		−0.4		−0.4		
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	−20	−112	−30	−112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, See Note 1	2.4	4	2.4	4	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J,  $\overline{K}$ , CLK, and  $\overline{\text{PRE}}$  grounded, then with J,  $\overline{K}$ , CLK, and  $\overline{\text{CLR}}$  grounded.

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			30		34		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	17	3	13	ns
t <sub>PHL</sub>			5	17	5	15	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	5	21	5	16	ns
t <sub>PHI</sub>			5	20	5	18	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS109A	–55°C to 125°C
SN74AS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54AS109A			SN74AS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V
I <sub>OH</sub>	High-level output current		−2			−2			mA
I <sub>OL</sub>	Low-level output current		20			20			mA
f <sub>clock</sub> *	Clock frequency		0	90		0	105		MHz
t <sub>w</sub> *	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t <sub>su</sub> *	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2			2			
t <sub>h</sub> *	Hold time after CLK↑	Data	0			0			ns
T <sub>A</sub>	Operating free-air temperature		−55	125		0	70		°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109A			SN74AS109A			UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				–1.2			–1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$			0.25	0.5		0.25	0.5	V
$I_I$		$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$				0.1			0.1	mA
$I_{IH}$	CLK, J, or $\overline{K}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$				20			20	$\mu\text{A}$
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
$I_{IL}$	CLK, J, or $\overline{K}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$				–0.5			–0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					–1.8			–1.8	
$I_{O}^{\S}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$		–30		–112	–30		–112	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , See Note 1			11.5	17		11.5	17	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J, K, CLK, and  $\overline{PRE}$  grounded, then with J, K, CLK, and  $\overline{CLR}$  grounded.

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

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#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS109A		SN74AS109A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			90		105		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	2	9	2	8	ns
t <sub>PHL</sub>			3.5	11.5	3.5	10.5	
t <sub>PLH</sub>	CLK	Q or Q̄	2.5	10	2.5	9	ns
t <sub>PHL</sub>			3.5	10.5	3.5	9	

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

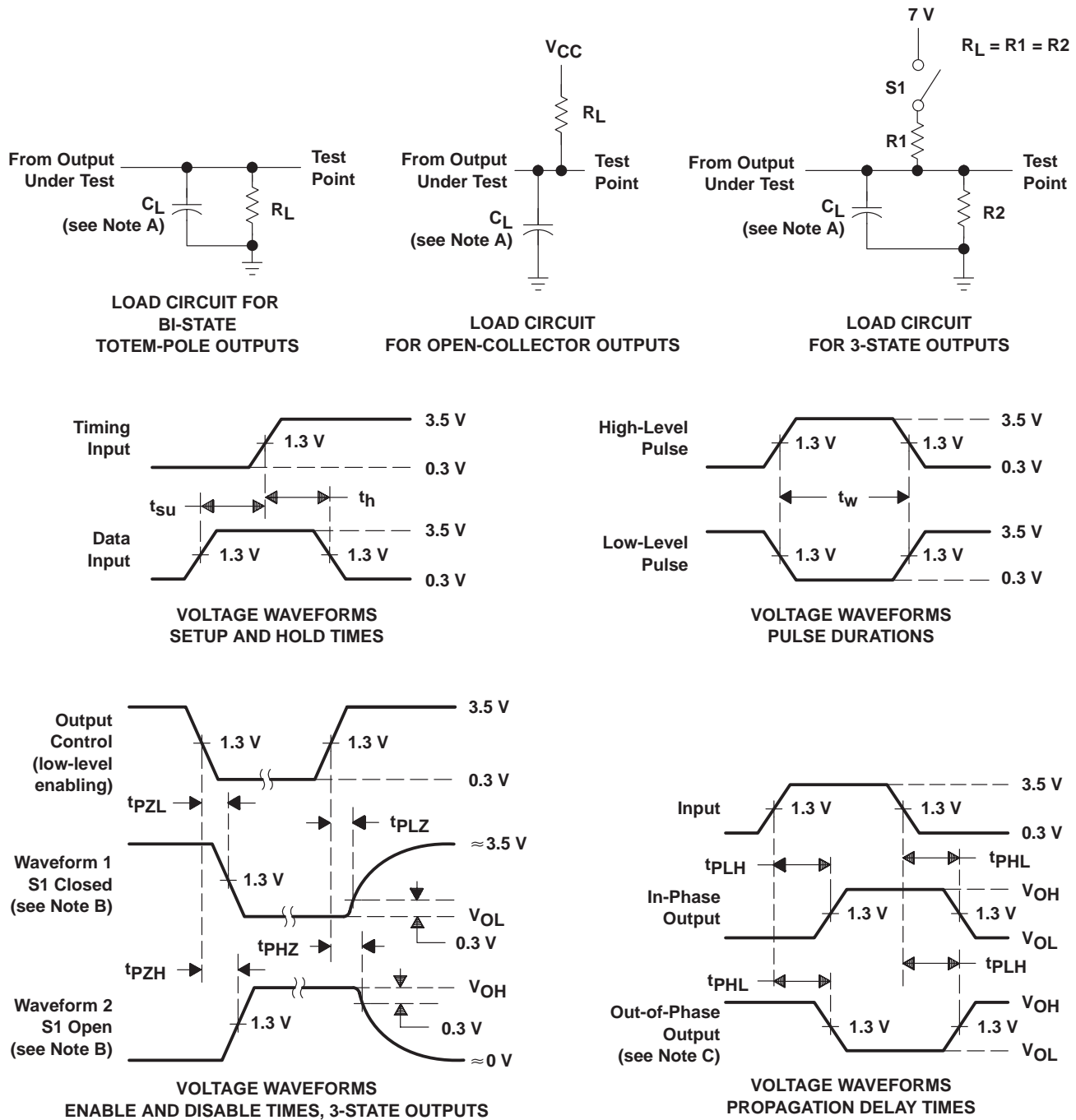
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. When measuring propagation delay items of 3-state outputs, switch S1 is open.

D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.

E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84000012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84000012A SNJ54ALS 109AFK	<a href="#">Samples</a>
8400001EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8400001EA SNJ54ALS109AJ	<a href="#">Samples</a>
8400001FA	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		
JM38510/37102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37102B2A	<a href="#">Samples</a>
JM38510/37102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37102BEA	<a href="#">Samples</a>
M38510/37102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37102B2A	<a href="#">Samples</a>
M38510/37102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37102BEA	<a href="#">Samples</a>
SN54ALS109AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS109AJ	<a href="#">Samples</a>
SN74ALS109AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A	<a href="#">Samples</a>
SN74ALS109ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A	<a href="#">Samples</a>
SN74ALS109ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A	<a href="#">Samples</a>
SN74ALS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS109AN	<a href="#">Samples</a>
SN74ALS109AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74ALS109ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS109AN	<a href="#">Samples</a>
SN74ALS109ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A	<a href="#">Samples</a>
SN74AS109AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS109A	<a href="#">Samples</a>
SN74AS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS109AN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS109ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS109A	<a href="#">Samples</a>
SNJ54ALS109AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84000012A SNJ54ALS 109AFK	<a href="#">Samples</a>
SNJ54ALS109AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8400001EA SNJ54ALS109AJ	<a href="#">Samples</a>
SNJ54AS109AFK	LIFEBUY	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54AS 109AFK	
SNJ54AS109AJ	LIFEBUY	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54AS109AJ	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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**OTHER QUALIFIED VERSIONS OF SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A :**

- Catalog: [SN74ALS109A](#), [SN74AS109A](#)
- Military: [SN54ALS109A](#), [SN54AS109A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS109ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS109ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS109ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS109ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS109ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74AS109ANSR	SO	NS	16	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP2-F16

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



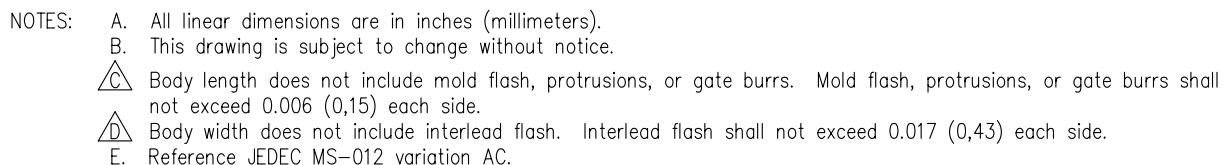
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.





D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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