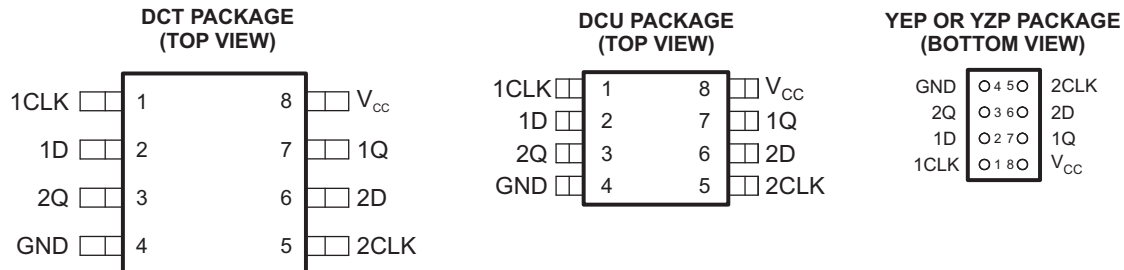


FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial Power-Down-Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.9 ns at 1.8 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽²⁾ |
|----------------|--|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP | Reel of 3000 | SN74AUC2G79YEPR | __ _UR_ |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74AUC2G79YZPR | |
| | SSOP – DCT | Reel of 3000 | SN74AUC2G79DCTR | U79_ _ _ |
| | VSSOP – DCU | Reel of 3000 | SN74AUC2G79DCUR | U79_ |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
 DCU: The actual top-side marking has one additional character that designates the assembly/test site.
 YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



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SN74AUC2G79

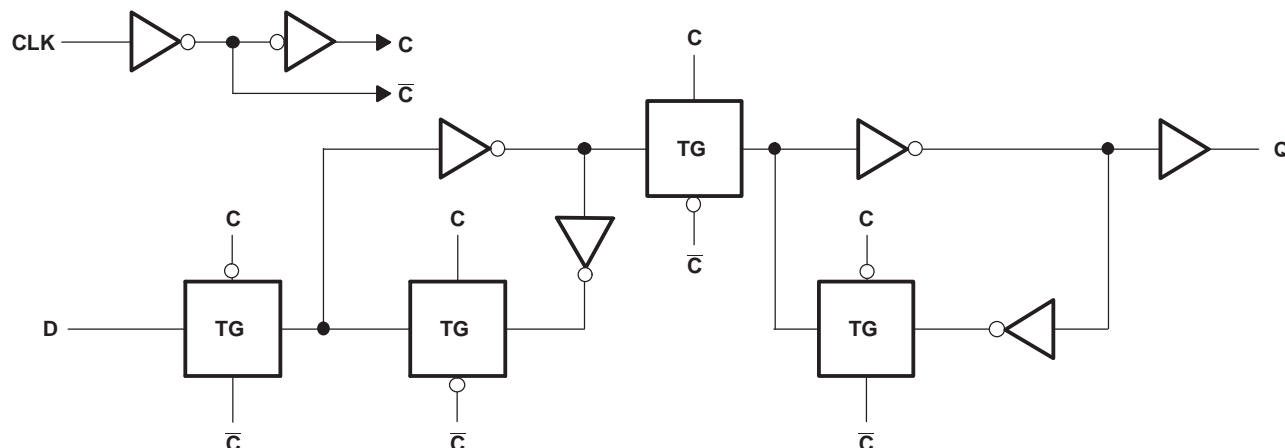
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES536B–DECEMBER 2003–REVISED JUNE 2006

FUNCTION TABLE

| INPUTS | | OUTPUT Q |
|--------|---|----------------|
| CLK | D | |
| ↑ | H | H |
| ↑ | L | L |
| L | X | Q ₀ |

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|-----------------|-----------------------|------|
| V _{CC} | Supply voltage range | −0.5 | 3.6 | V |
| V _I | Input voltage range ⁽²⁾ | −0.5 | 3.6 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | −0.5 | 3.6 | V |
| V _O | Output voltage range ⁽²⁾ | −0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | | −50 | mA |
| I _{OK} | Output clamp current | | −50 | mA |
| I _O | Continuous output current | | ±20 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| θ _{JA} | Package thermal impedance ⁽³⁾ | DCT package | 220 | °C/W |
| | | DCU package | 227 | |
| | | YEP/YZP package | 102 | |
| T _{stg} | Storage temperature range | −65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|------------------------------------|--|------------------------|-----------------|------|
| V _{CC} | Supply voltage | | 0.8 | 2.7 | V |
| V _{IH} | High-level input voltage | V _{CC} = 0.8 V | V _{CC} | | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.65 × V _{CC} | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 0.8 V | 0 | | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.35 × V _{CC} | | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | |
| V _I | Input voltage | | 0 | 3.6 | V |
| V _O | Output voltage | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 0.8 V | −0.7 | | mA |
| | | V _{CC} = 1.1 V | −3 | | |
| | | V _{CC} = 1.4 V | −5 | | |
| | | V _{CC} = 1.65 V | −8 | | |
| | | V _{CC} = 2.3 V | −9 | | |
| I _{OL} | Low-level output current | V _{CC} = 0.8 V | 0.7 | | mA |
| | | V _{CC} = 1.1 V | 3 | | |
| | | V _{CC} = 1.4 V | 5 | | |
| | | V _{CC} = 1.65 V | 8 | | |
| | | V _{CC} = 2.3 V | 9 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 0.8 V to 1.65 V ⁽²⁾ | 20 | | ns/V |
| | | V _{CC} = 1.65 V to 2.3 V ⁽³⁾ | 20 | | |
| | | V _{CC} = 2.3 V to 2.7 V ⁽³⁾ | 20 | | |
| T _A | Operating free-air temperature | | −40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).

(3) The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).

SN74AUC2G79

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES536B–DECEMBER 2003–REVISED JUNE 2006

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|-----------------|---|-----------------|-----------------------|--------------------|-----|------|
| V _{OH} | | I _{OH} = −100 μA | 0.8 V to 2.7 V | V _{CC} − 0.1 | | | V |
| | | I _{OH} = −0.7 mA | 0.8 V | 0.55 | | | |
| | | I _{OH} = −3 mA | 1.1 V | 0.8 | | | |
| | | I _{OH} = −5 mA | 1.4 V | 1 | | | |
| | | I _{OH} = −8 mA | 1.65 V | 1.2 | | | |
| | | I _{OH} = −9 mA | 2.3 V | 1.8 | | | |
| V _{OL} | | I _{OL} = 100 μA | 0.8 V to 2.7 V | 0.2 | | | V |
| | | I _{OL} = 0.7 mA | 0.8 V | 0.25 | | | |
| | | I _{OL} = 3 mA | 1.1 V | 0.3 | | | |
| | | I _{OL} = 5 mA | 1.4 V | 0.4 | | | |
| | | I _{OL} = 8 mA | 1.65 V | 0.45 | | | |
| | | I _{OL} = 9 mA | 2.3 V | 0.6 | | | |
| I _I | D or CLK inputs | V _I = V _{CC} or GND | 0 to 2.7 V | ±5 | | | μA |
| I _{off} | | V _I or V _O = 2.7 V | 0 | ±10 | | | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 0.8 V to 2.7 V | 10 | | | μA |
| C _i | | V _I = V _{CC} or GND | 2.5 V | 2.5 | | | pF |

(1) All typical values are at T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| | | V _{CC} = 0.8 V | V _{CC} = 1.2 V ± 0.1 V | V _{CC} = 1.5 V ± 0.1 V | V _{CC} = 1.8 V ± 0.15 V | V _{CC} = 2.5 V ± 0.2 V | UNIT |
|--------------------|---------------------------------|-------------------------|------------------------------------|------------------------------------|-------------------------------------|------------------------------------|------|
| | | TYP | MIN MAX | MIN MAX | MIN MAX | MIN MAX | |
| f _{clock} | Clock frequency | 50 | 200 | 225 | 250 | 275 | MHz |
| t _w | Pulse duration, CLK high or low | 2.4 | 1 | 1 | 1 | 1 | ns |
| t _{su} | Setup time before CLK↑ | 1.6 | 0.9 | 0.6 | 0.6 | 0.5 | ns |
| t _h | Hold time, data after CLK↑ | 0 | 0 | 0 | 0.1 | 0.1 | ns |

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 0.8 V | V _{CC} = 1.2 V ± 0.1 V | V _{CC} = 1.5 V ± 0.1 V | V _{CC} = 1.8 V ± 0.15 V | V _{CC} = 2.5 V ± 0.2 V | UNIT |
|------------------|-----------------|----------------|-------------------------|------------------------------------|------------------------------------|-------------------------------------|------------------------------------|------|
| | | | TYP | MIN MAX | MIN MAX | MIN TYP MAX | MIN MAX | |
| f _{max} | | | 50 | 200 | 225 | 250 | 275 | MHz |
| t _{pd} | CLK | Q | 5 | 1 3.9 | 0.8 2.5 | 0.3 1 1.9 | 0.3 1.3 | ns |

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see [Figure 1](#))

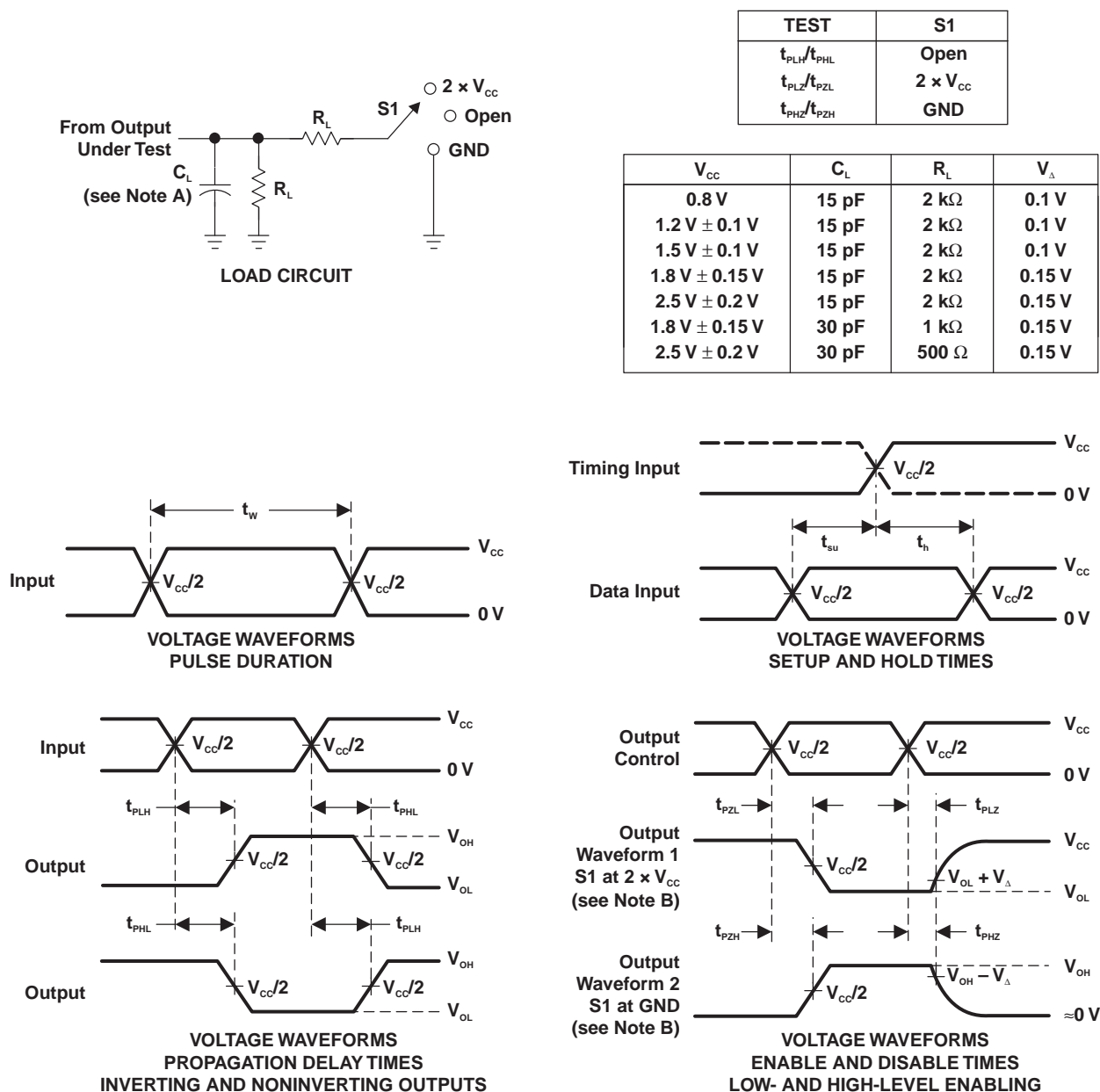
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | | V _{CC} = 2.5 V ± 0.2 V | | UNIT |
|------------------|-----------------|----------------|-------------------------------------|-----|-----|------------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| f _{max} | | | 250 | | | 275 | | ns |
| t _{pd} | CLK | Q | 0.8 | 1.5 | 2.4 | 0.6 | 1.8 | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CC} = 0.8\text{ V}$ | $V_{CC} = 1.2\text{ V}$ | $V_{CC} = 1.5\text{ V}$ | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | UNIT |
|-----------|-------------------------------|-----------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | f = 10 MHz | 16 | 16.2 | 18 | 19.8 | 29.2 | pF |
| | CLK | | 1.1 | 1.1 | 1.2 | 1.5 | 2.7 | |
| | Total | | 17.1 | 17.3 | 19.2 | 21.3 | 31.9 | |

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate \geq 1 V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AUC2G79DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AUC2G79DCTRE4 | ACTIVE | SM8 | DCT | 8 | 3000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AUC2G79DCUR | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AUC2G79DCURE4 | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AUC2G79YEPR | NRND | WCSP | YEP | 8 | 3000 | TBD | SNPB | Level-1-260C-UNLIM |
| SN74AUC2G79YZPR | ACTIVE | WCSP | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

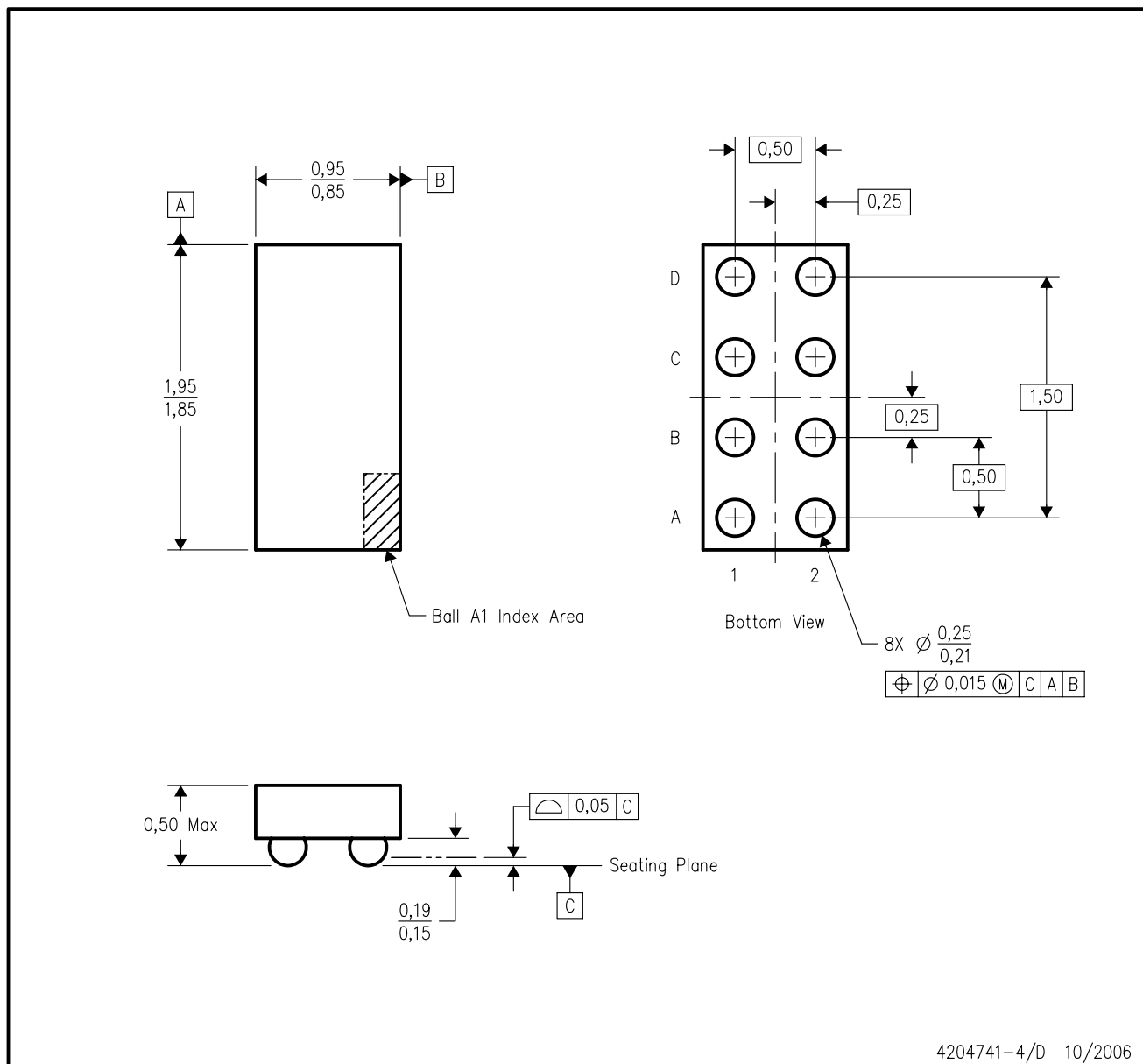


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

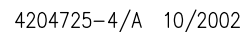
YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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