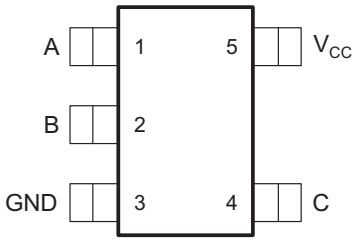
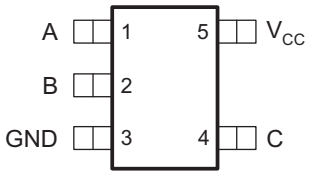
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Wide V_{CC} Range of 0.8 V to 2.7 V**
- **Sub-1-V Operable**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed – Max 0.2 ns (V_{CC} = 1.8 V, C_L = 15 pF)**
- **Low On-State Impedance – Typically 99 Ω (V_{CC} = 2.3 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

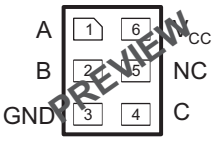
DBV PACKAGE
(TOP VIEW)



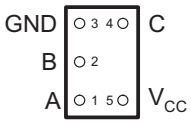
DCK PACKAGE
(TOP VIEW)



DRY PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.
NC– No internal connection

DESCRIPTION/ORDERING INFORMATION

This single analog switch is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G66 can handle both analog and digital signals. The combined AC and DC signal has to be between V_{CC} and GND for it to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

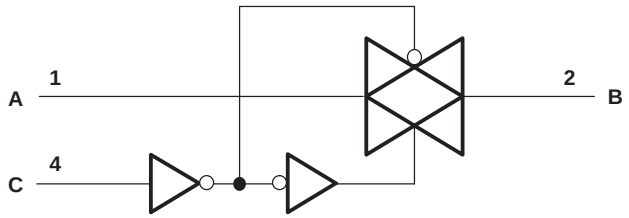
T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoFree™ WCSP (DSBGA) – YZP (Pb-free)	Reel of 3000	SN74AUC1G66YZAR	_ _ _U6_
	SON – DRY	Reel of 5000	SN74AUC1G66DRYR	PREVIEW
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUC1G66DBVR	U66_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUC1G66DCKR	U6_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DBV/DCK/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	3.6	V
V_I	Input voltage range(2)		–0.5	3.6	V
$V_{I/O}$	Switch I/O voltage range(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_I < 0		–50	mA
I_{IOK}	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		±50	mA
I_T	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DBV package		206	°C/W
		DCK package		252	
		DRY package		234	
		YZP package		123	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	$0.65 \times V_{CC}$		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	
		V_{CC} = 2.3 V to 2.7 V		0.7	
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_I	Control input voltage		0	3.6	V
$\Delta t/\Delta v$	Input transition rise or fall rate			20	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
r_{on}	On-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 1)	I_S = 4 mA	1.65 V		10	20	Ω
			I_S = 8 mA	2.3 V		9	15	
$r_{on(p)}$	Peak on resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 1)	I_S = 4 mA	1.65 V		32	80	Ω
			I_S = 8 mA	2.3 V		15	20	
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 2)		2.7 V			±1	µA
							±0.1[1]	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see Figure 3)		2.7 V			±1	µA
							±0.1[1]	
I_I	Control input current	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND,	I_O = 0	0.8 V to 2.7 V			10	µA
C_{ic}	Control input capacitance			2.5 V		2		pF
$C_{io(off)}$	Switch input/output capacitance			2.5 V		3.5		pF
$C_{io(on)}$	Switch input/output capacitance			2.5 V		7		pF

(1) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}[1]	A or B	B or A	0.9		0.3		0.2			0.2		0.1	ns
t_{en}	C	A or B	4.1	0.5	2.6	0.5	1.7	0.5	0.8	1.1	0.5	1	ns
t_{dis}	C	A or B	5	0.7	3.6	0.5	2.6	0.5	1.7	2.9	0.5	2.2	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd} (1)	A or B	B or A			0.3		0.3	ns
t_{en}	C	A or B	0.5	1.4	2.3	0.8	1.4	ns
t_{dis}	C	A or B	0.5	1.7	2.9	0.5	1.5	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (1) (switch ON)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 5)	0.8 V	60	MHz
				1.1 V	60	
				1.4 V	80	
				1.65 V	120	
				2.3 V	170	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 5)	0.8 V	>500	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 6)	0.8 V	9	mV
				1.1 V	14	
				1.4 V	15	
				1.65 V	16	
				2.3 V	20	
Feedthrough attenuation (2) (switch OFF)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	–60	dB
				1.1 V	–60	
				1.4 V	–60	
				1.65 V	–60	
				2.3 V	–60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	–55	
				1.1 V	–55	
				1.4 V	–55	
				1.65 V	–55	
				2.3 V	–55	
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 8)	0.8 V	7.5	%
				1.1 V	0.16	
				1.4 V	0.04	
				1.65 V	0.03	
				2.3 V	0.02	
	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 8)	0.8 V	4.2	
				1.1 V	0.2	
				1.4 V	0.03	
				1.65 V	0.02	
				2.3 V	0.02	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	3	3	3	pF

PARAMETER MEASUREMENT INFORMATION

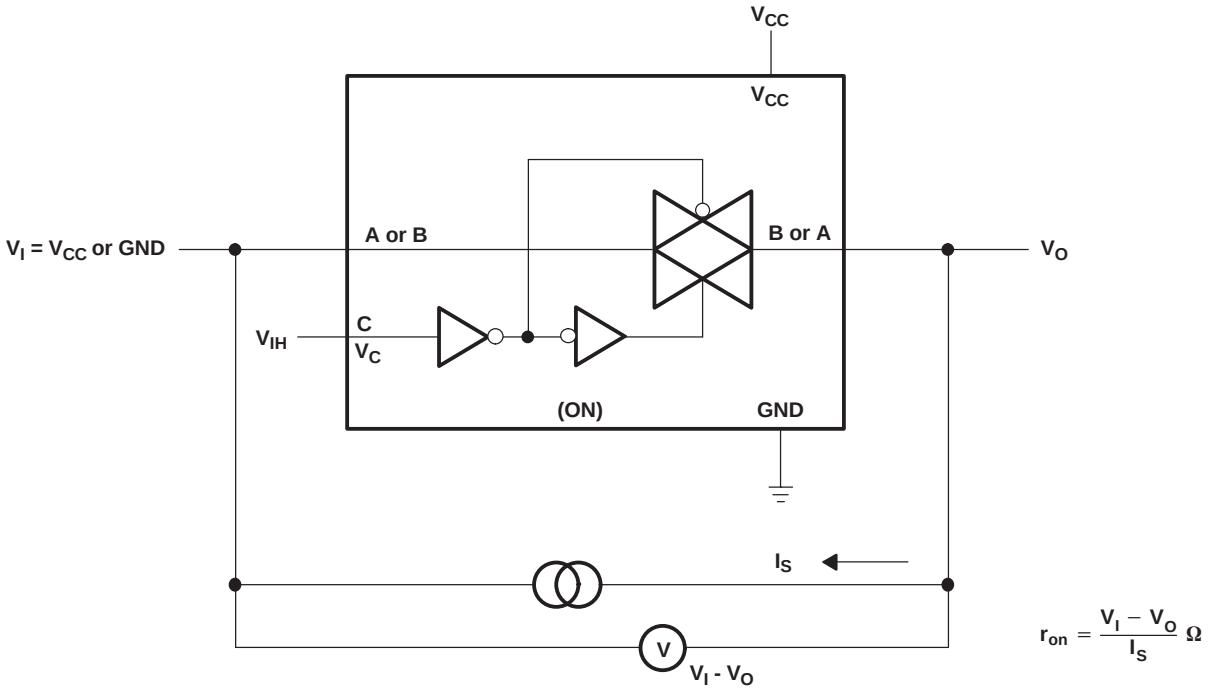


Figure 1. On-State Resistance Test Circuit

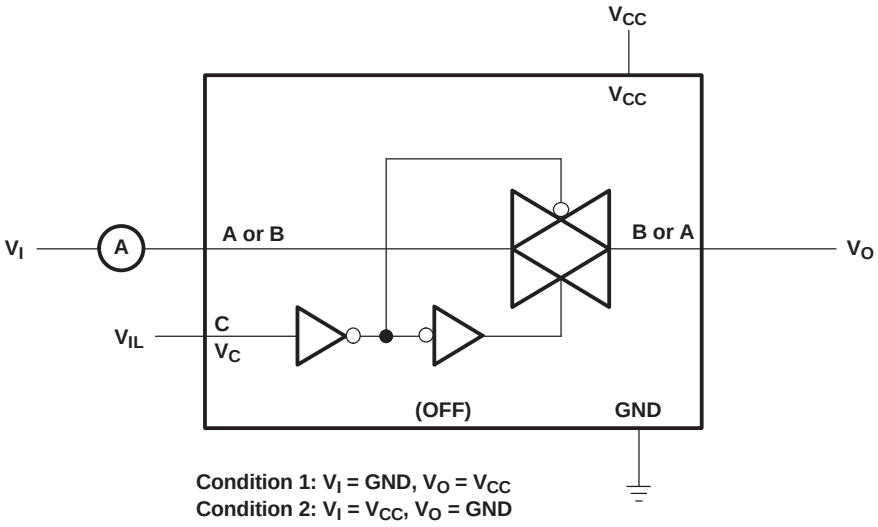


Figure 2. Off-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION (Continued)

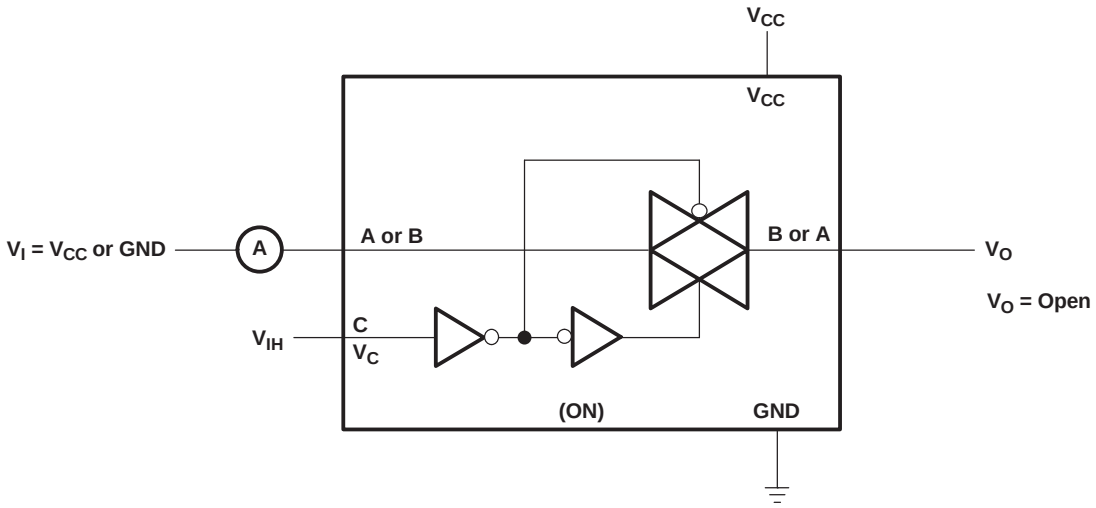
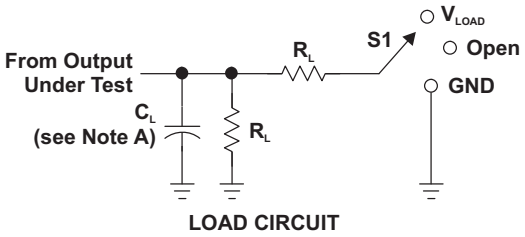


Figure 3. On-State Leakage-Current Test Circuit

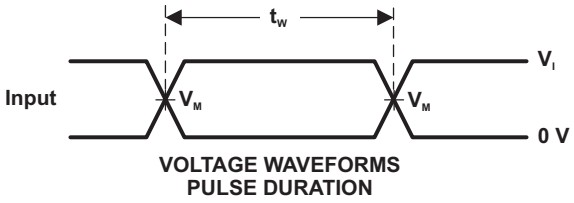
PARAMETER MEASUREMENT INFORMATION (Continued)



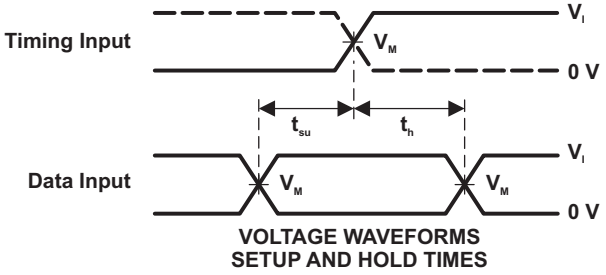
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

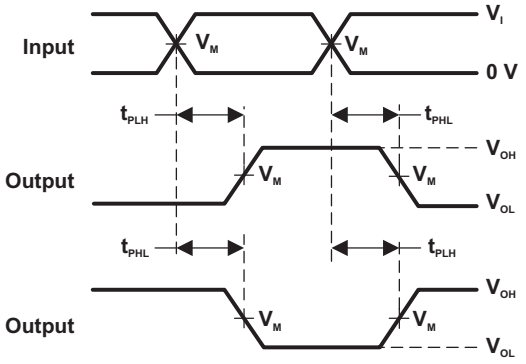
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V



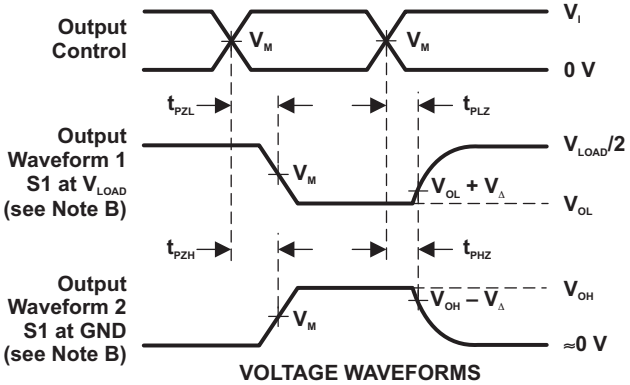
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, Slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (Continued)

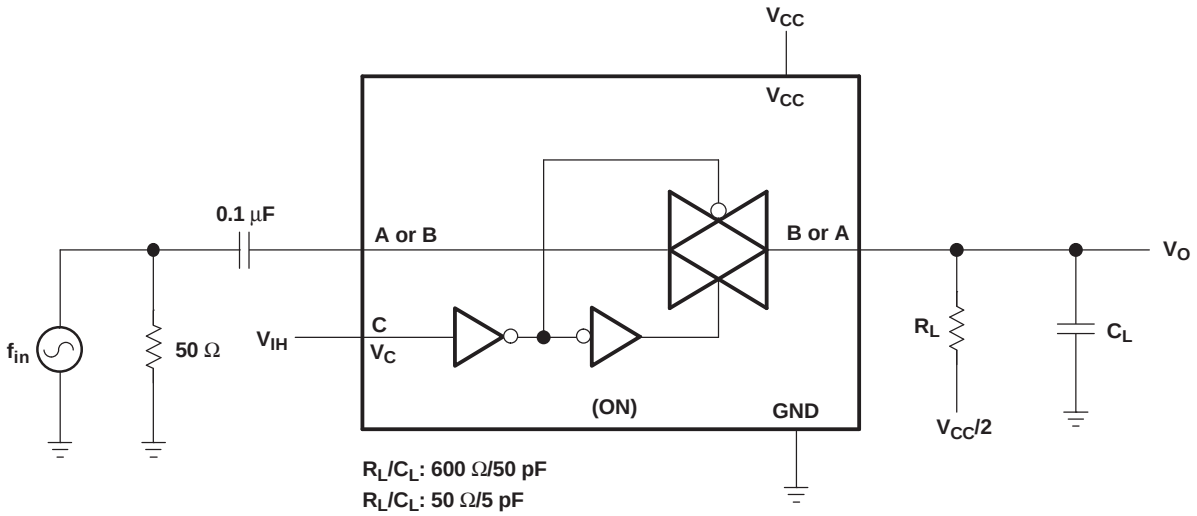


Figure 5. Frequency Response (Switch ON)

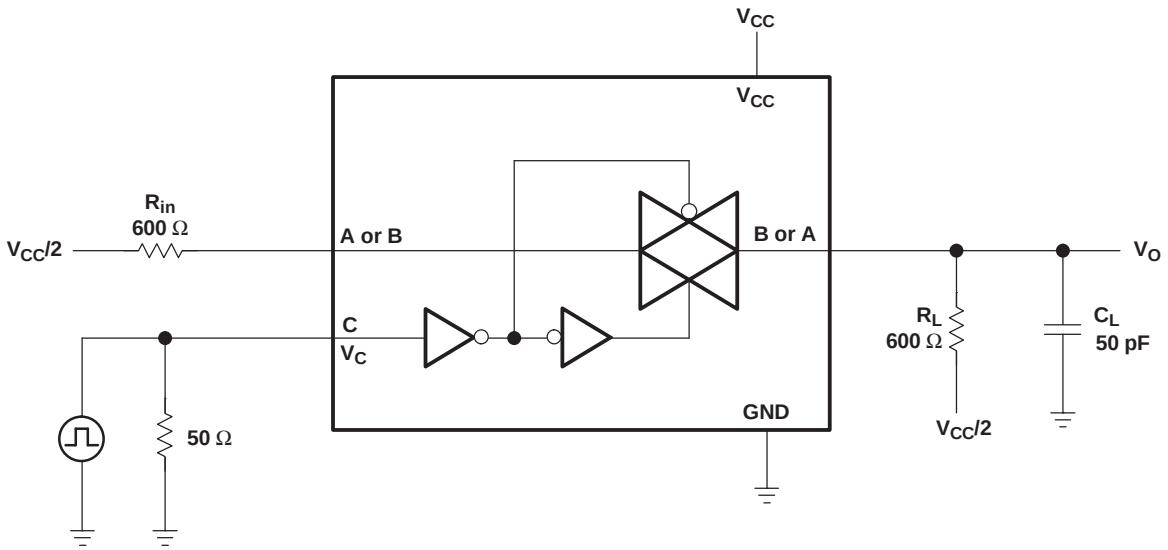


Figure 6. Crosstalk (Control Input – Switch Output)

PARAMETER MEASUREMENT INFORMATION (Continued)

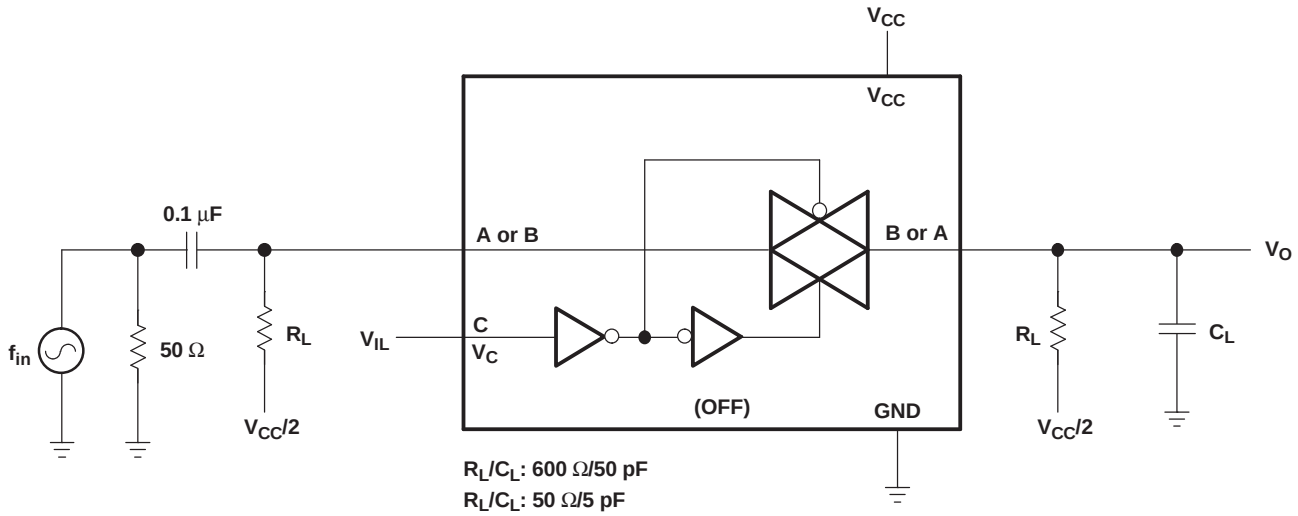


Figure 7. Feedthrough (Switch OFF)

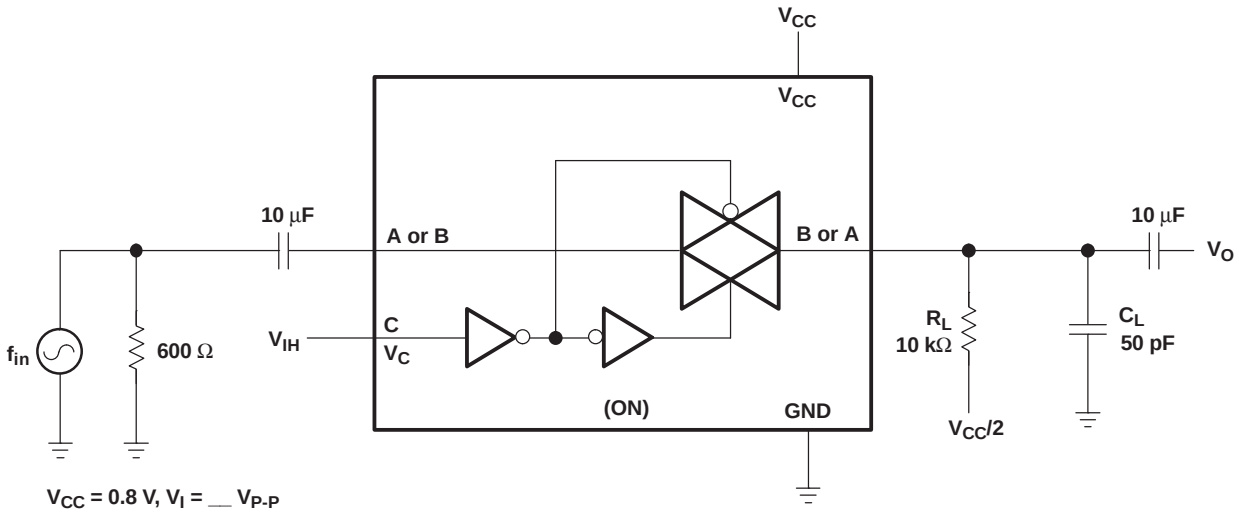


Figure 8. Sine-Wave Distortion

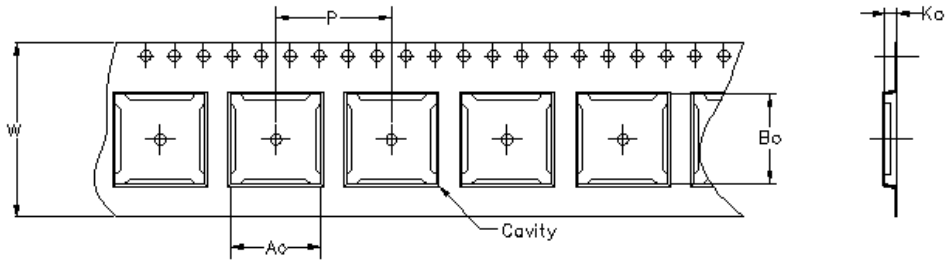
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74AUC1G66DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G66DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G66DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G66DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G66DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G66DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G66YZPR	ACTIVE	WCSP	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

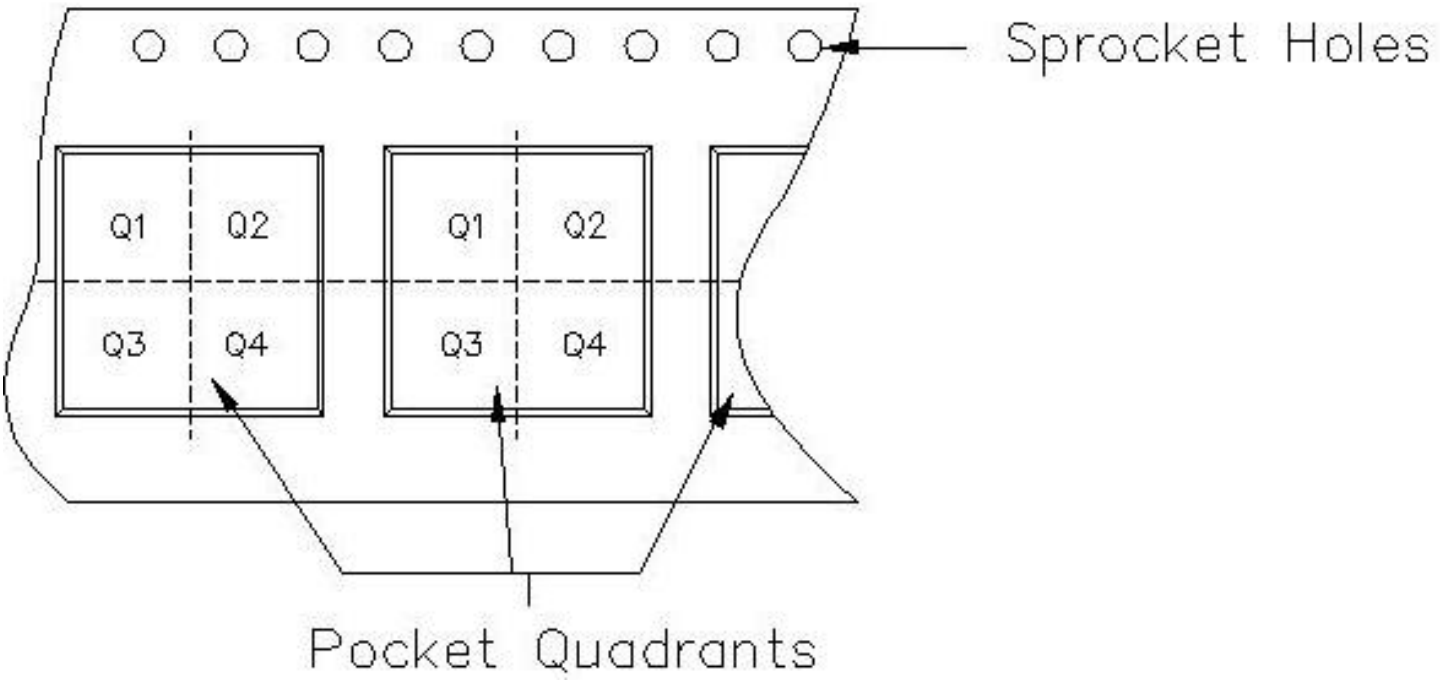
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



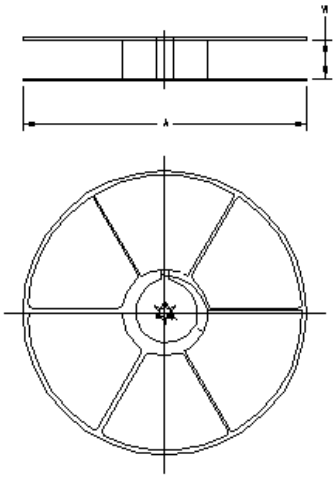
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



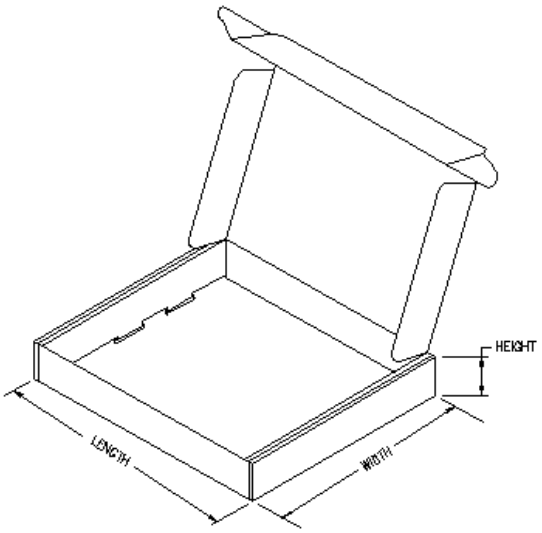
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G66DBVR	DBV	5	HNT	180	9	3.23	3.17	1.37	4	8	Q3
SN74AUC1G66DCKR	DCK	5	HNT	180	9	2.24	2.34	1.22	4	8	Q3
SN74AUC1G66YZPR	YZP	5	ASEK	180	8	1.02	1.52	0.66	4	8	Q1

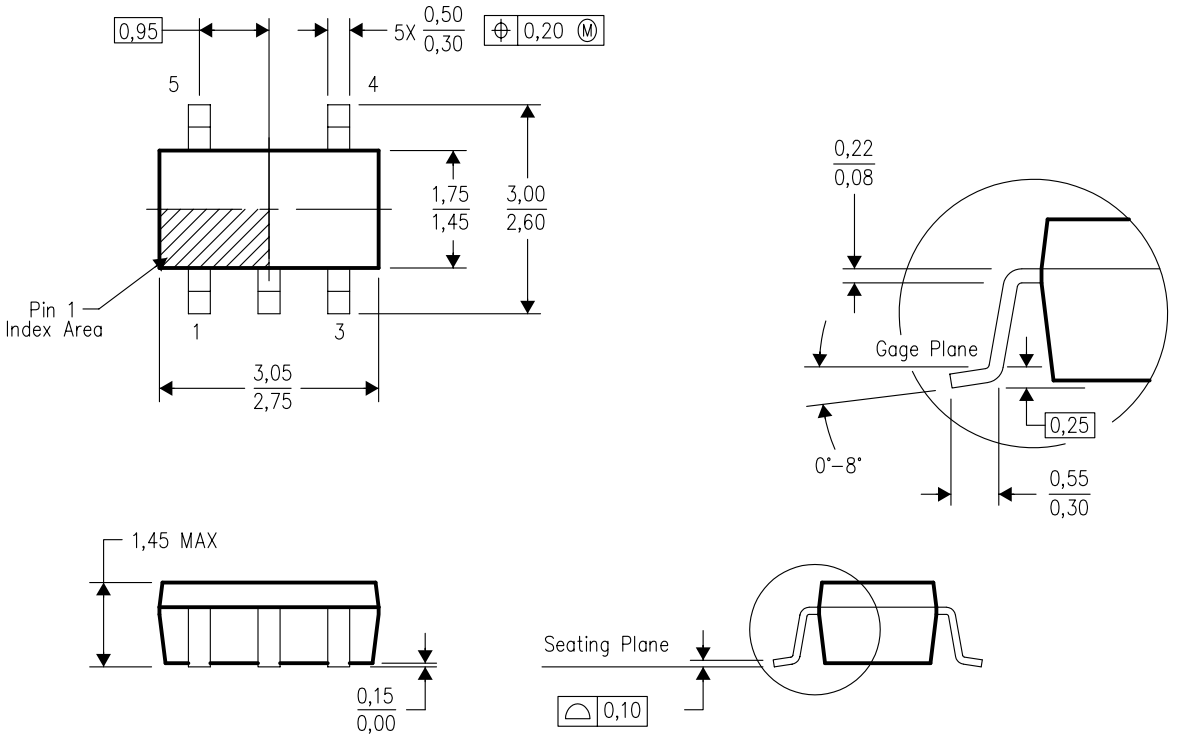


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G66DBVR	DBV	5	HNT	202.0	201.0	28.0
SN74AUC1G66DCKR	DCK	5	HNT	202.0	201.0	28.0
SN74AUC1G66YZPR	YZP	5	ASEK	220.0	220.0	34.0


HEIGHT
LENGTH
WIDTH

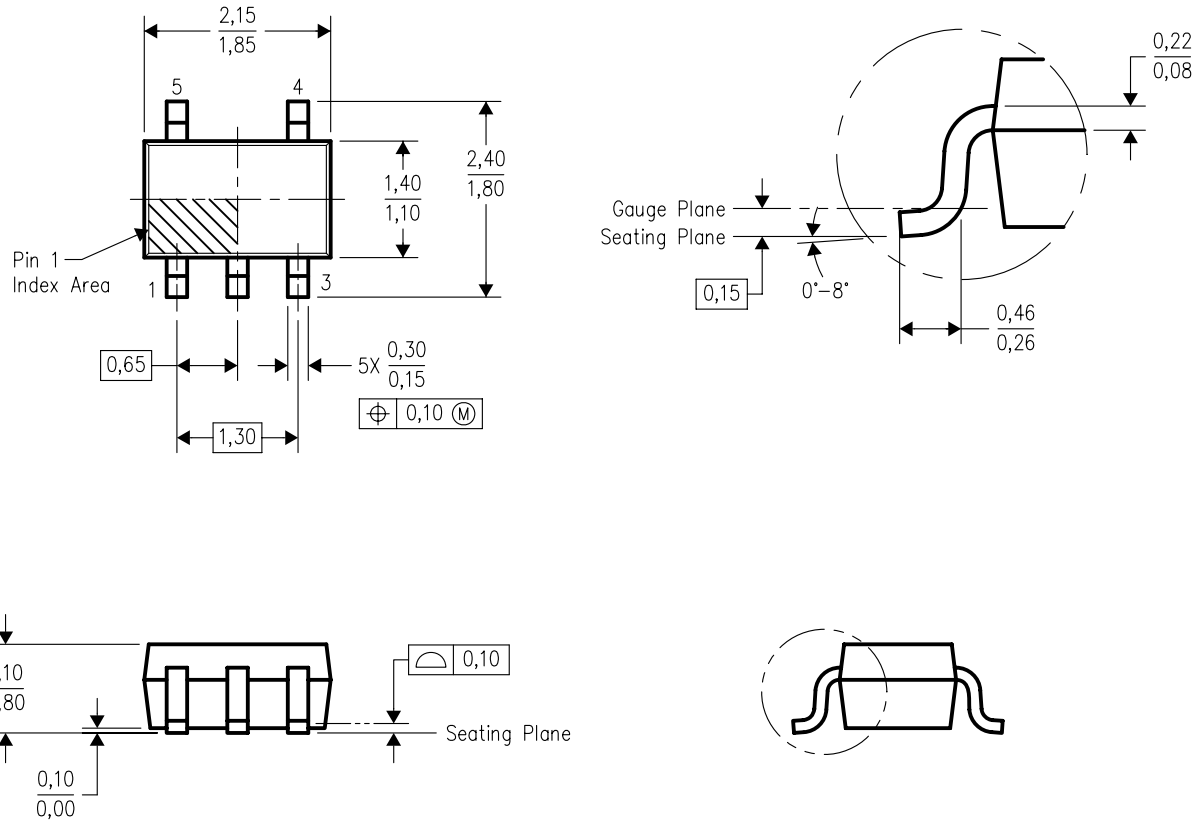
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

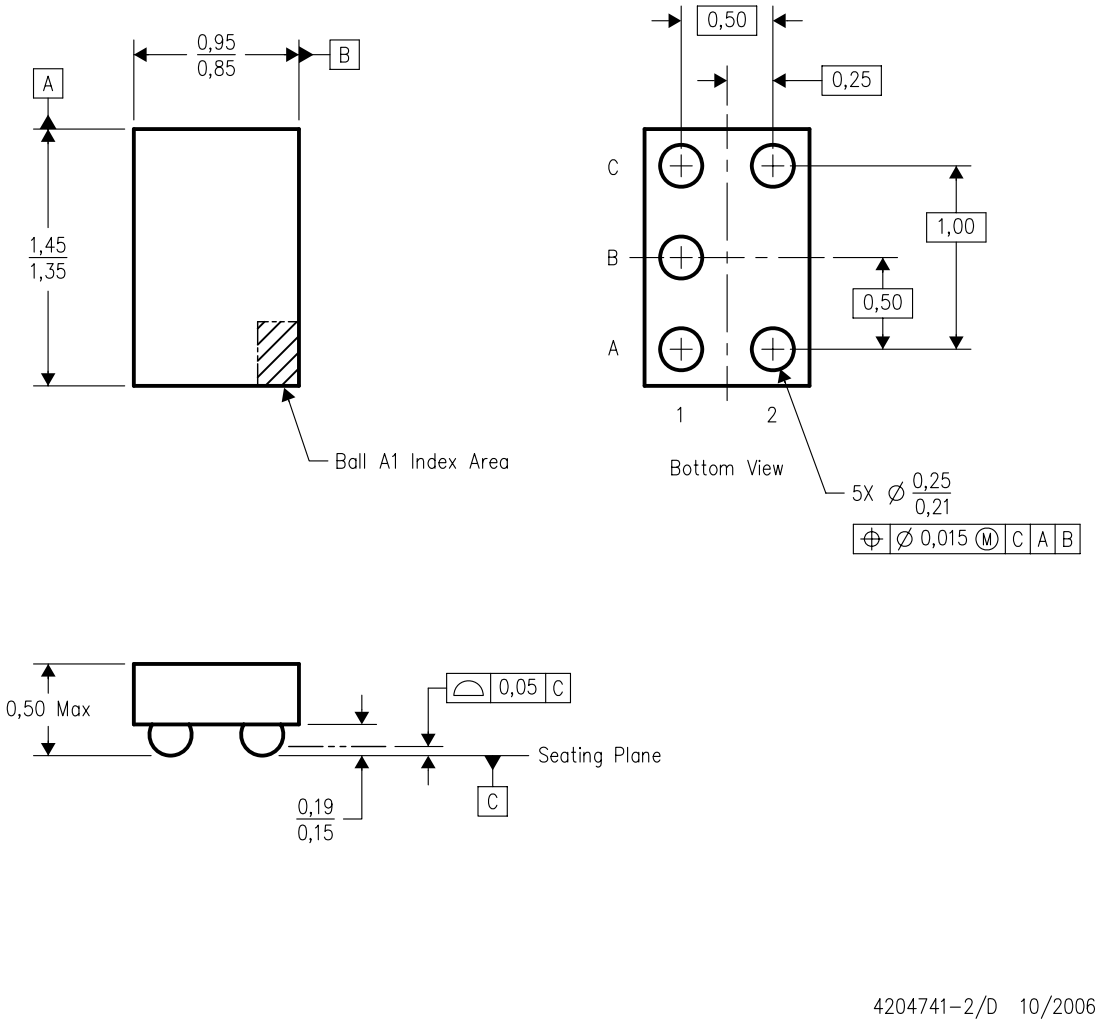
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

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