

# SN74CBTK16245

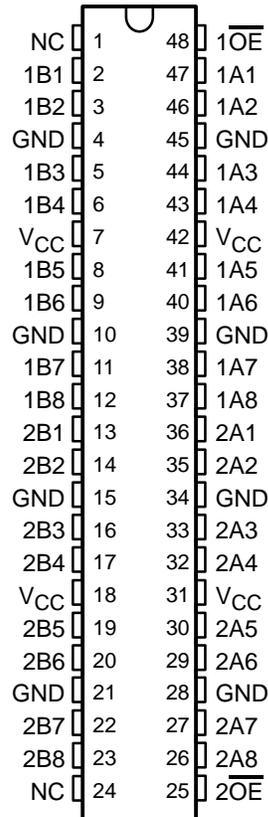
## 16-BIT FET BUS SWITCH

### WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS105D – APRIL 2000 – REVISED NOVEMBER 2001

- Member of the Texas Instruments Widebus™ Family
- Standard '16245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots up to -2 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

#### description

The SN74CBTK16245 device provides 16 bits of high-speed TTL-compatible bus switching in a standard '16245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled, and current from V<sub>CC</sub> is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as two 8-bit low-impedance switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on, and data can flow from the A port to the B port, or vice versa. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBTK16245DL	CBTK16245
		Tape and reel	SN74CBTK16245DLR	
	TSSOP – DGG	Tape and reel	SN74CBTK16245DGGR	CBTK16245
		TVSOP – DGV	Tape and reel	SN74CBTK16245DGVR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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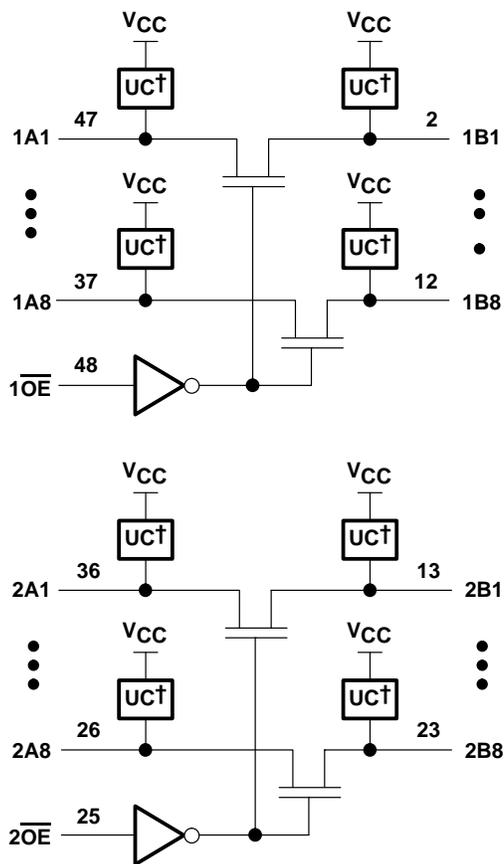
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**FUNCTION TABLE**  
 (each 8-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
H	Disconnect

**logic diagram (positive logic)**



† Undershoot clamp



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>†</sup>	A or B	B or A	0.35		0.25		ns
t <sub>en</sub>	$\overline{\text{OE}}$	A or B	7.4		1.6	4.9	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	A or B	7.4		4.2	7.5	ns

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**undershoot characteristics**

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OUTU</sub>	See Figures 1 and 2, and Table 1	2	V <sub>OH</sub> -0.3		V

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

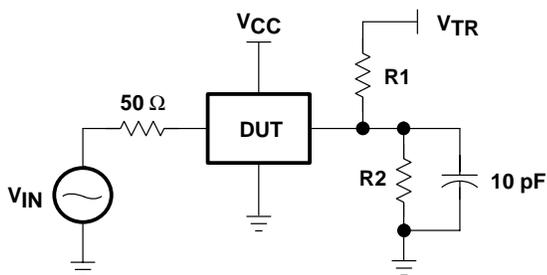


Figure 1. Device Test Setup

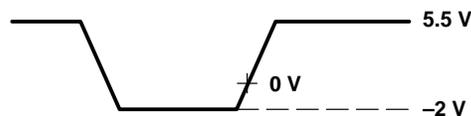


Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

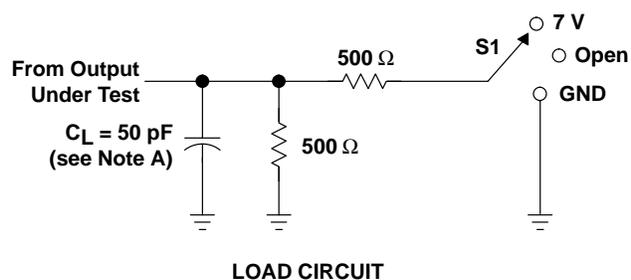
PARAMETER	VALUE	UNIT
B port under test <sup>§</sup>	See Figure 1	
V <sub>IN</sub>	See Figure 2	V
t <sub>w</sub>	20	ns
t <sub>r</sub>	2	ns
t <sub>f</sub>	2	ns
R1 = R2	100	kΩ
V <sub>TR</sub>	11	V
V <sub>CC</sub>	5.5	V

<sup>§</sup> Other B-port outputs are open.

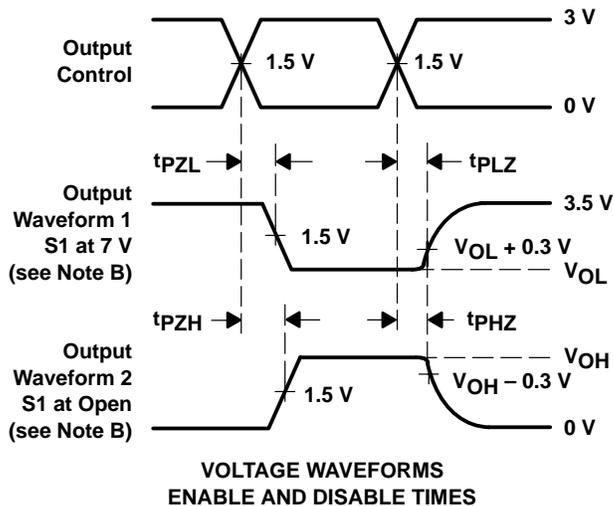
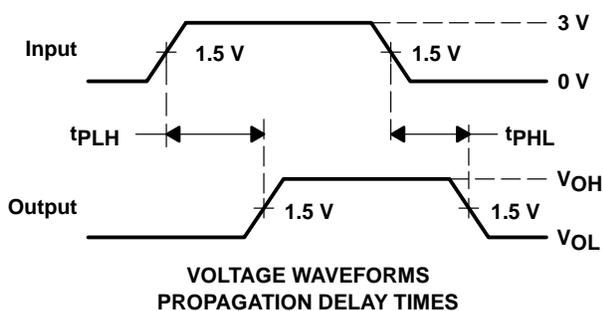
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**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTK16245DGGR	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	CBTK16245	
SN74CBTK16245DGVR	OBSOLETE	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85	CP245	
SN74CBTK16245DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85	CBTK16245	
SN74CBTK16245DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85	CBTK16245	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

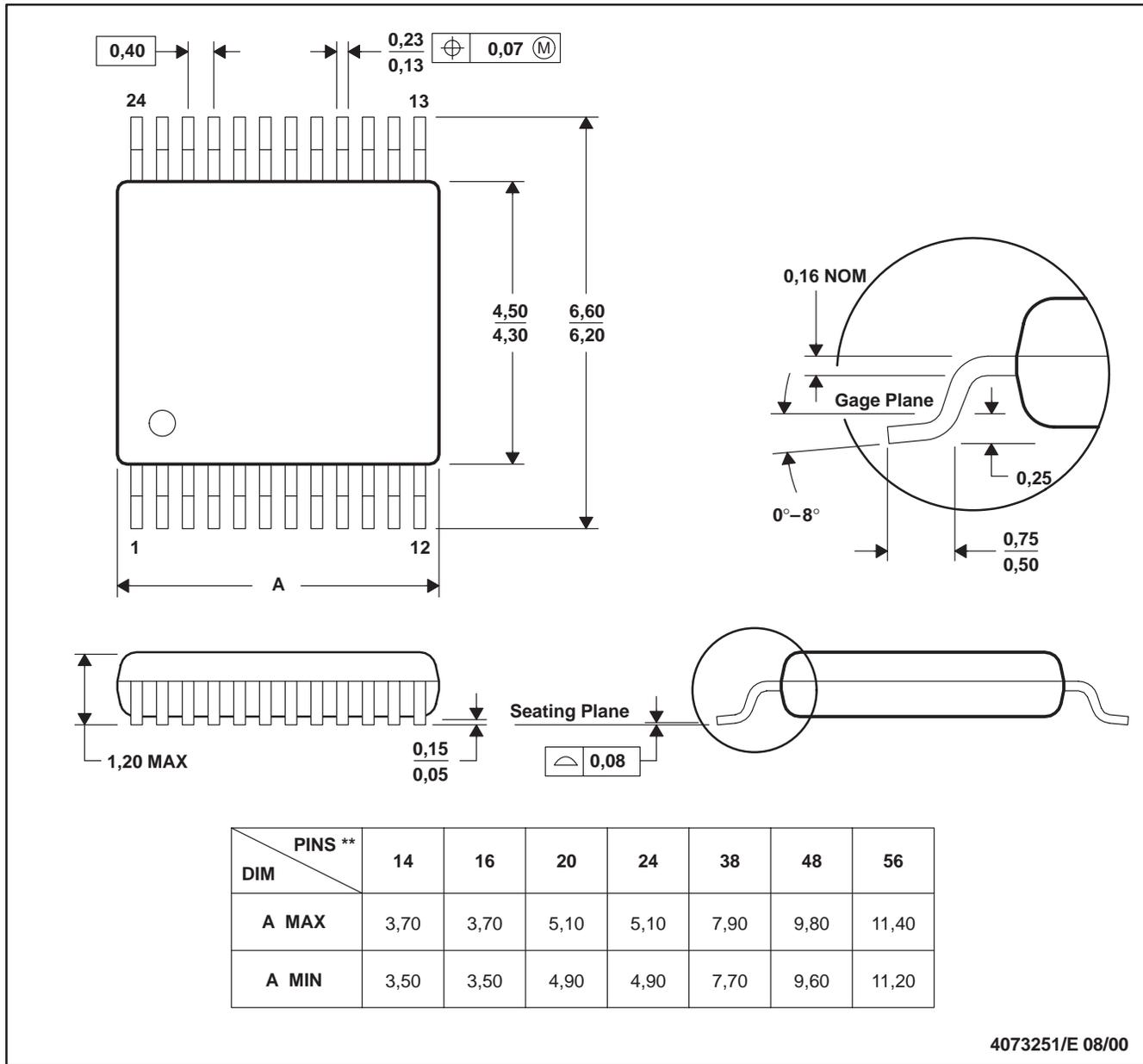
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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

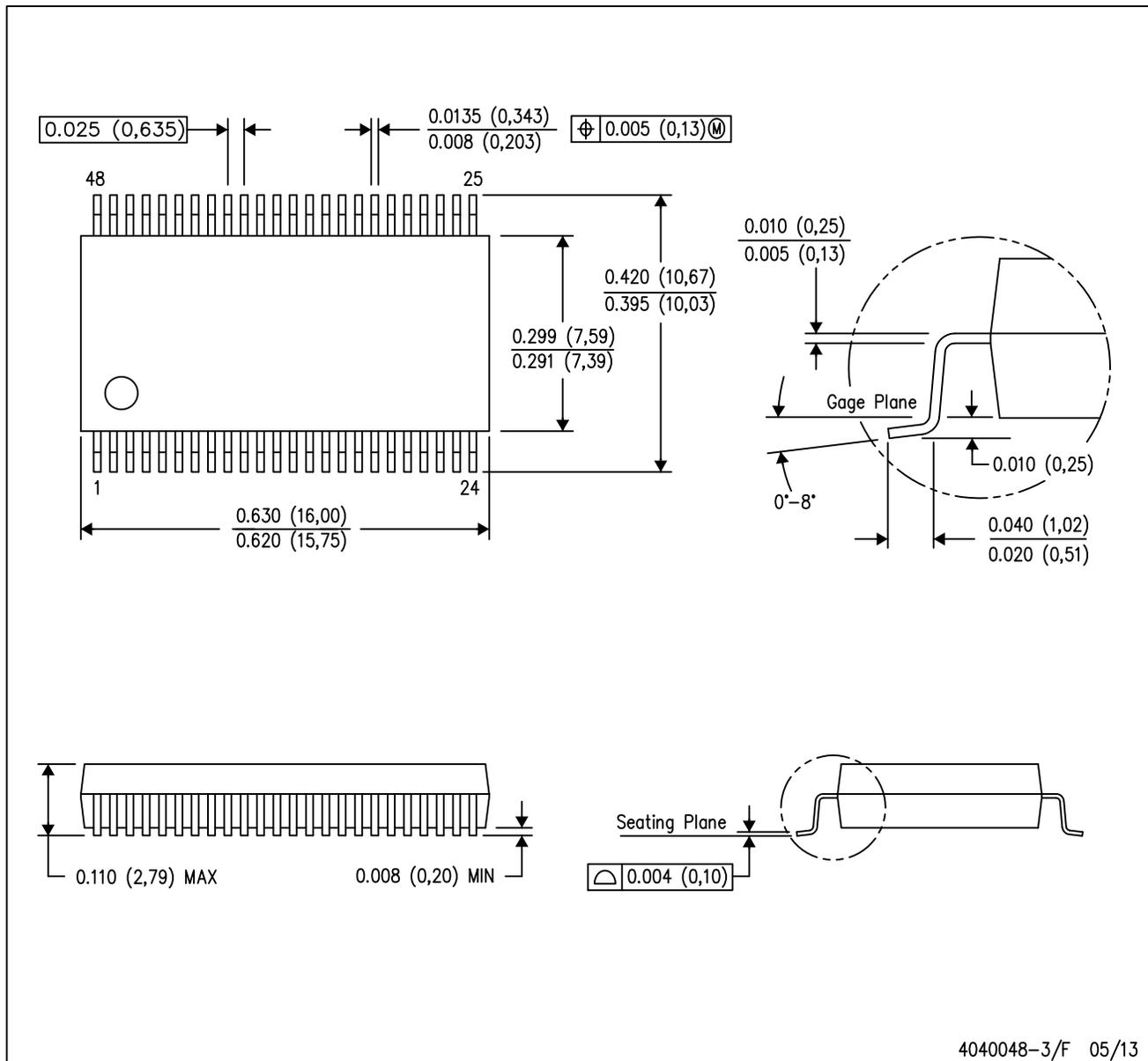


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



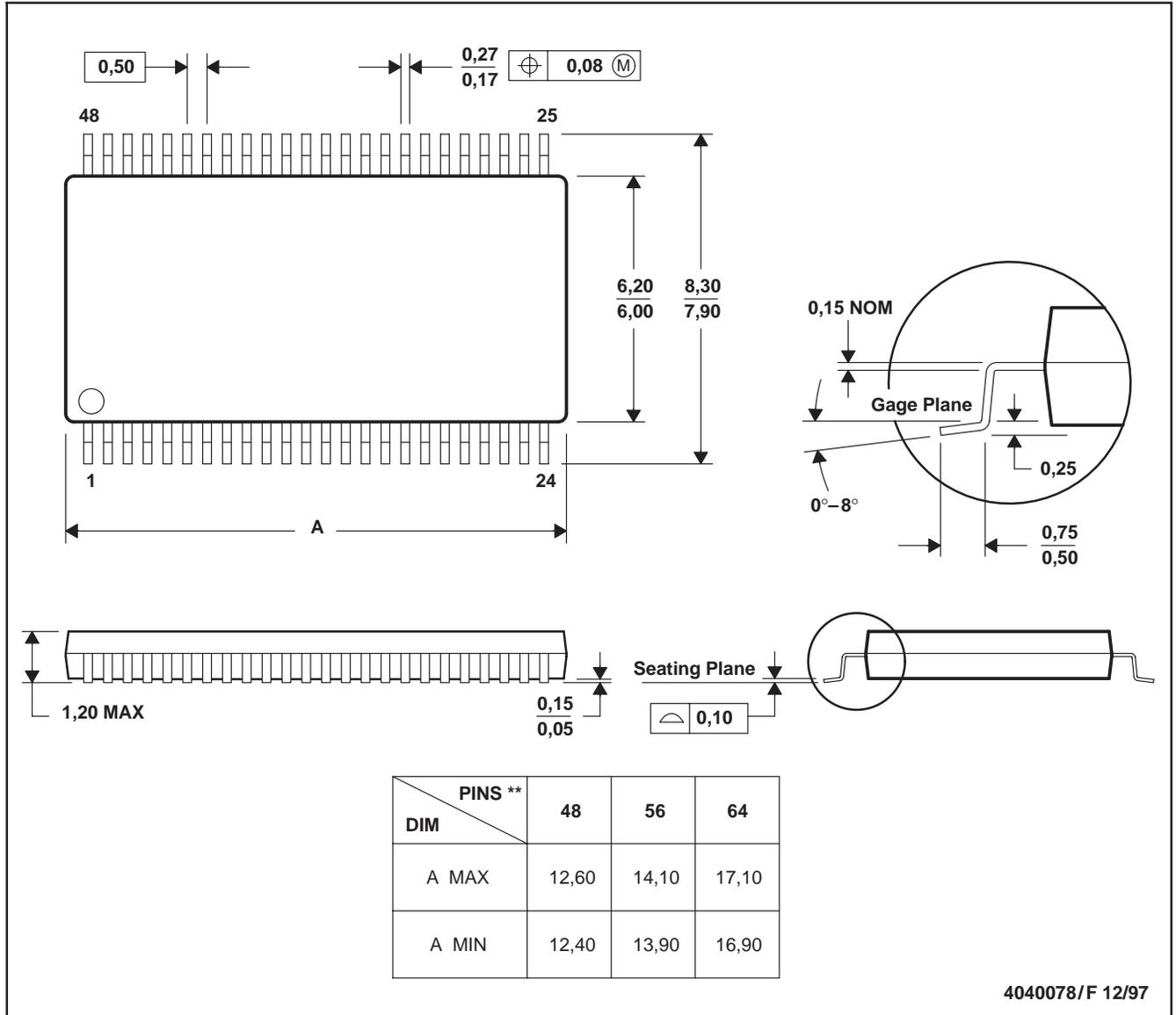
- NOTES:
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  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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