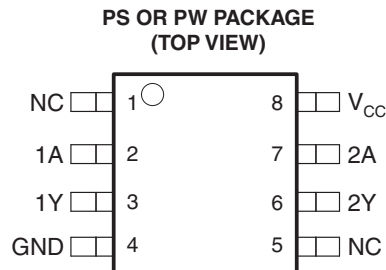


FEATURES

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 7$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Unbuffered Outputs



DESCRIPTION/ORDERING INFORMATION

The SN74HCU7204 contains two independent unbuffered inverters. The device performs the Boolean function $Y = \bar{A}$ in positive logic.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOP – PS	SN74HCU7204PS	HU7204
		Reel of 2000 SN74HCU7204PSR	
	TSSOP – PW	Tube of 90 SN74HCU7204PW	HU7204
		Reel of 2000 SN74HCU7204PWR	
		Reel of 250 SN74HCU7204PWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND			± 50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	PS package		TBD	°C/W
		PW package		TBD	
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.7			V
		$V_{CC} = 4.5$ V	3.6			
		$V_{CC} = 6$ V	4.8			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.3	V
		$V_{CC} = 4.5$ V			0.8	
		$V_{CC} = 6$ V			1.1	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.5$ V			-4	mA
		$V_{CC} = 6$ V			-5.2	
I_{OL}	Low-level output current	$V_{CC} = 4.5$ V			4	mA
		$V_{CC} = 6$ V			5.2	
t_t	Transition time	$V_{CC} = 2$ V	0		1000	ns
		$V_{CC} = 4.5$ V	0		500	
		$V_{CC} = 6$ V	0		400	
T_A	Operating free-air temperature		-40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V _{OH}	V _I = V _{CC} or GND	I _{OH} = –20 µA	2 V	1.8			1.8		V
			4.5 V	4			4		
			6 V	5.5			5.5		
		I _{OH} = –4 mA	4.5 V	3.86			3.76		
		I _{OH} = –5.2 mA	6 V	5.36			5.26		
V _{OL}	V _I = V _{CC} or GND	I _{OL} = 20 µA	2 V			0.2		0.2	V
			4.5 V			0.5		0.5	
			6 V			0.5		0.5	
		I _{OL} = 4 mA	4.5 V			0.32		0.37	
		I _{OL} = 5.2 mA	6 V			0.32		0.37	
I _I	V _I = V _{CC} or 0		6 V			±100		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			2		20	µA
C _i			2 V to 6 V			3	10	10	pF

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 1](#))

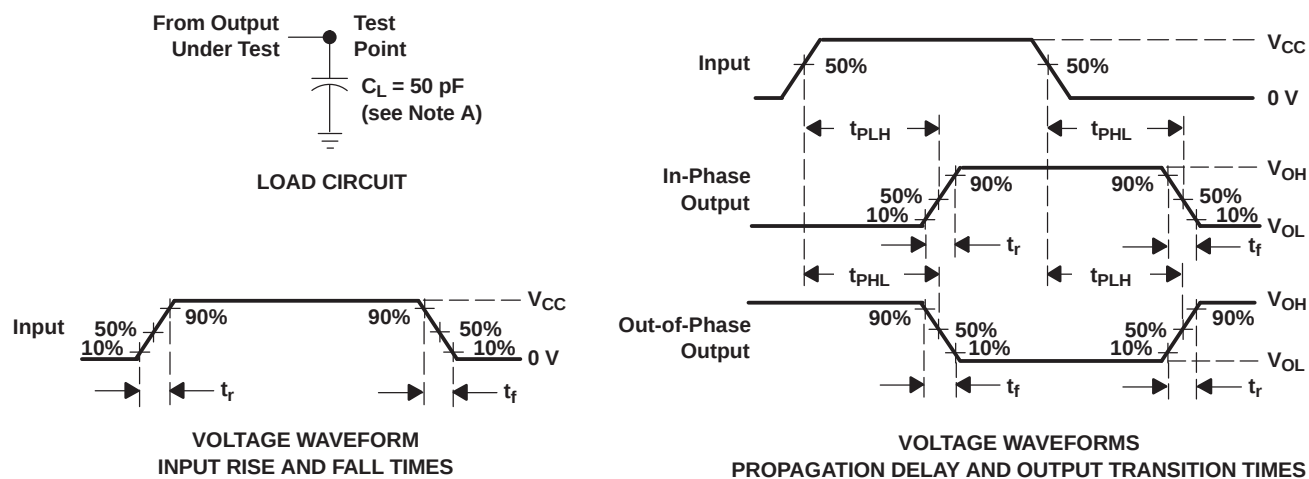
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	A	Y	2 V		40	80		100	ns
			4.5 V		8	16		20	
			6 V		7	14		17	
t _r /t _f		Y	2 V		38	75		95	ns
			4.5 V		8	15		19	
			6 V		6	13		16	

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time, with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCU7204PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		HU7204	Samples
SN74HCU7204PWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI			Samples
SN74HCU7204PWG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI			Samples
SN74HCU7204PWTE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI			Samples
SN74HCU7204PWTG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

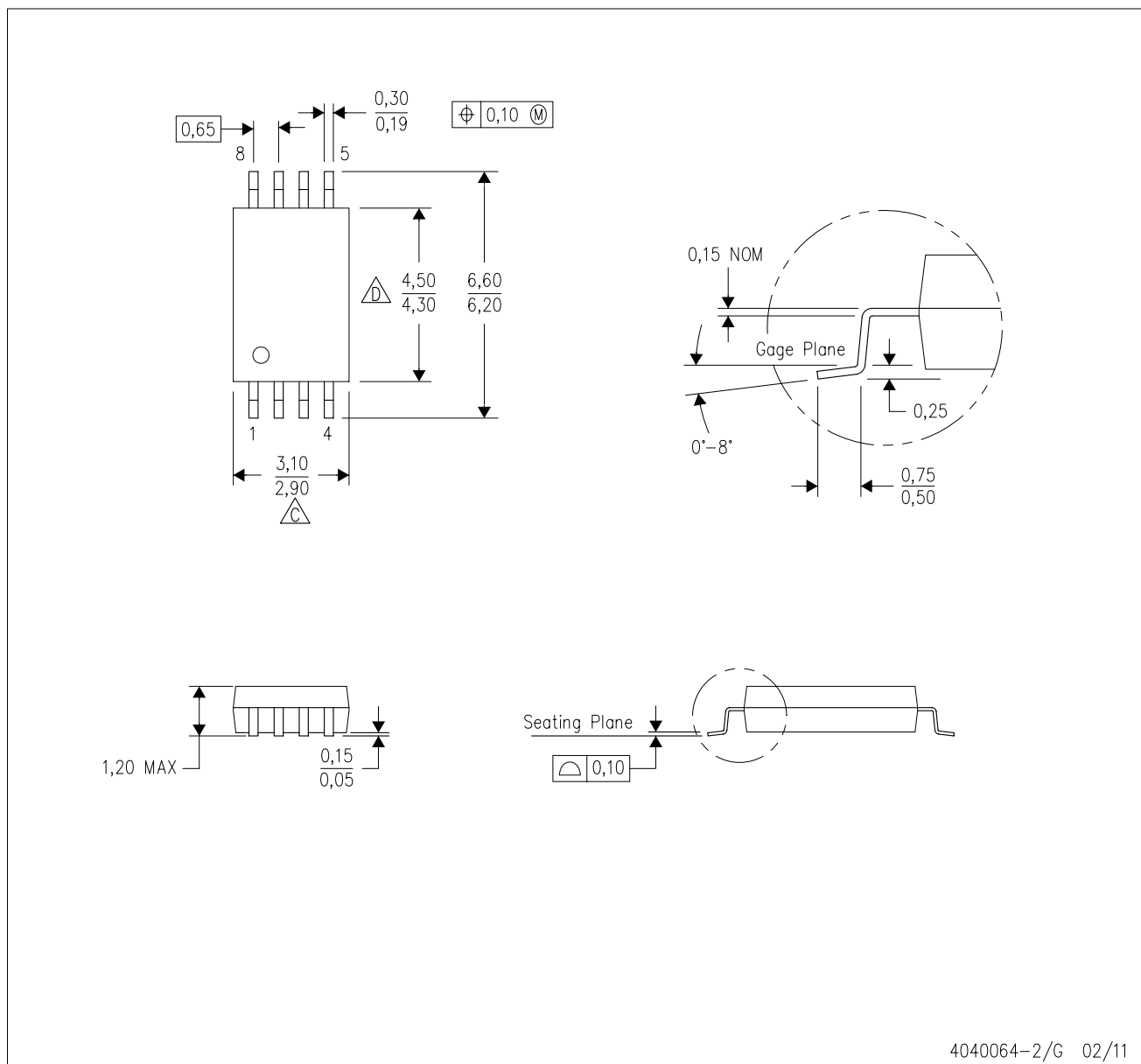
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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