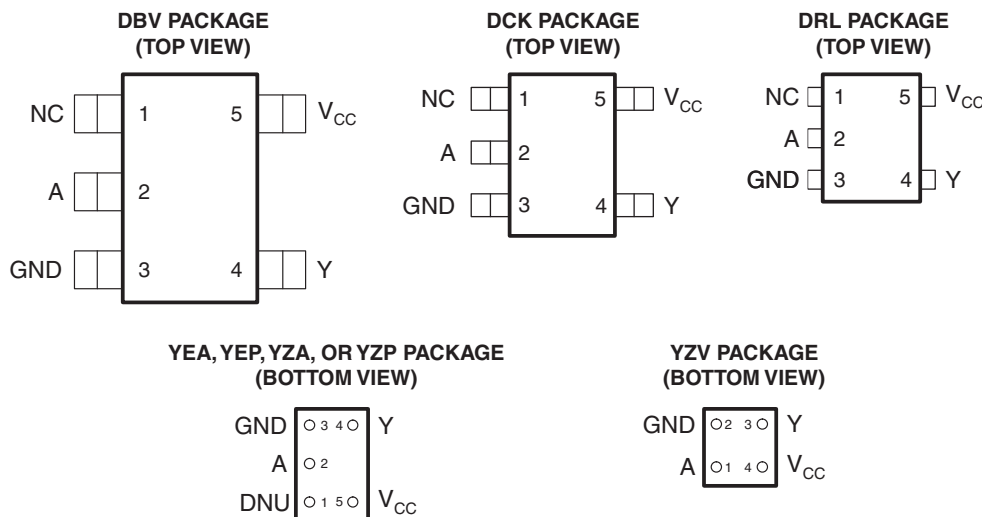


FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Unbuffered Output
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

NC – No internal connection

DNU – Do not use

DESCRIPTION/ORDERING INFORMATION

This single inverter gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1GU04 contains one inverter with an unbuffered output and performs the Boolean function $Y = \bar{A}$.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

SN74LVC1GU04

SINGLE INVERTER GATE

SCES215S–APRIL 1999–REVISED OCTOBER 2006

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Reel of 3000	SN74LVC1GU04YEAR	_ _ _ CD _
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC1GU04YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC1GU04YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1GU04YZPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free)		SN74LVC1GU04YZVR	CD _ _
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1GU04DBVR	CU4 _
		Reel of 250	SN74LVC1GU04DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1GU04DCKR	CD _
		Reel of 250	SN74LVC1GU04DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1GU04DRLR	CD _

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.
 YEA/YEP, YZA/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
 YZV: The actual top-side marking is on two lines. Line 1 has four characters to denote year, month, day, and assembly/test site. Line 2 has two characters which show the family and function code. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC) DBV, DCK, DRL, YEA, YEP, YZA, and YZP PACKAGE



YZV PACKAGE



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		RATING	UNIT
V_{CC}	Supply voltage range	–0.5 to 6.5	V
V_I	Input voltage range ⁽²⁾	0.5 to 6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	–50
I_{OK}	Output clamp current	$V_O < 0$	–50
I_O	Continuous output current	± 50	mA
	Continuous current through V_{CC} or GND	± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DBV package	206
		DCK package	252
		DRL package	142
		YEA/YZA package	154
		YEP/YZP package	132
		YZV package	116
T_{stg}	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	$I_O = -100 \mu A$	$0.75 \times V_{CC}$		V
V_{IL}	Low-level input voltage	$I_O = 100 \mu A$		$0.25 \times V_{CC}$	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 V$		–4	mA
		$V_{CC} = 2.3 V$		–8	
		$V_{CC} = 3 V$		–16	
				–24	
		$V_{CC} = 4.5 V$		–32	
I_{OL}	Low-level output current	$V_{CC} = 1.65 V$		4	mA
		$V_{CC} = 2.3 V$		8	
		$V_{CC} = 3 V$		16	
				24	
		$V_{CC} = 4.5 V$		32	
T_A	Operating free-air temperature		–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

SN74LVC1GU04

SINGLE INVERTER GATE

SCES215S–APRIL 1999–REVISED OCTOBER 2006

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	V _{IL} = 0 V	I _{OH} = –100 µA	1.65 V to 5.5 V		V _{CC} – 0.1	V
		I _{OH} = –4 mA	1.65 V		1.2	
		I _{OH} = –8 mA	2.3 V		1.9	
		I _{OH} = –16 mA	3 V		2.4	
		I _{OH} = –24 mA			2.3	
		I _{OH} = –32 mA	4.5 V		3.8	
V _{OL}	V _{IH} = V _{CC}	I _{OL} = 100 µA	1.65 V to 5.5 V		0.1	V
		I _{OL} = 4 mA	1.65 V		0.45	
		I _{OL} = 8 mA	2.3 V		0.3	
		I _{OL} = 16 mA	3 V		0.4	
		I _{OL} = 24 mA			0.55	
		I _{OL} = 32 mA	4.5 V		0.55	
I _I	A input	V _I = 5.5 V or GND	0 to 5.5 V		±5	µA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	µA
C _i		V _I = V _{CC} or GND	3.3 V		7	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (See [Figure 1](#))

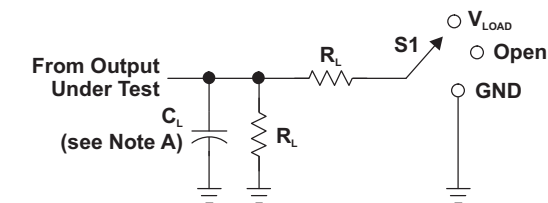
PARAMETER	FROM (INPUT)	TO (INPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.3	5	1	4	1.1	3.7	1	3	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	f = 10 MHz	9	11	13	27	pF

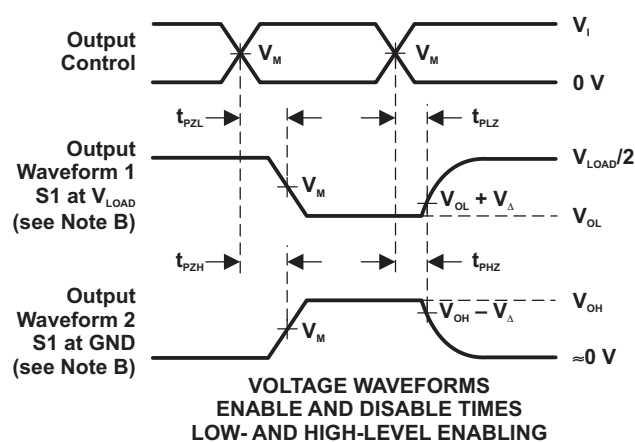
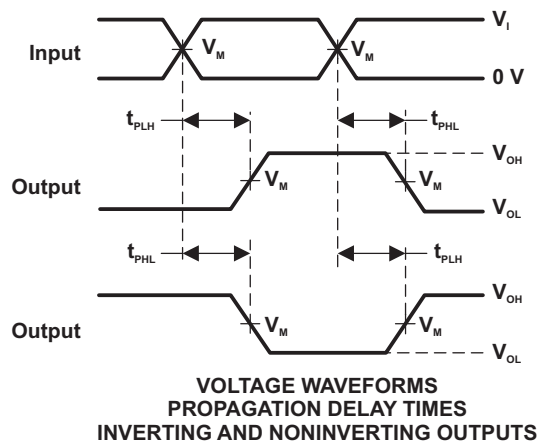
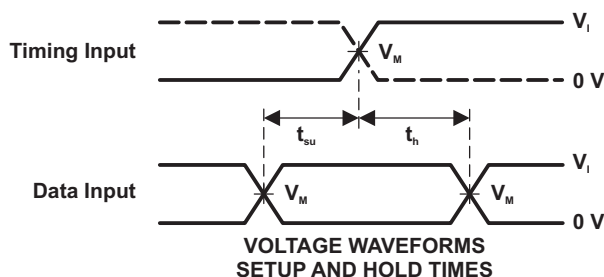
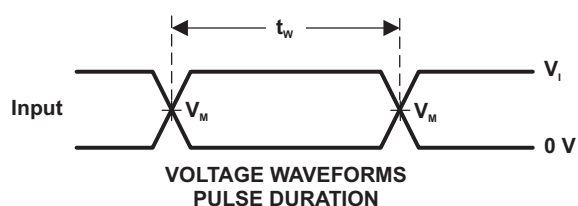
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_i/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVC1GU04DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GU04DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GU04DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GU04DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GU04DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GU04DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1GU04DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GU04DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GU04DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GU04DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GU04DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GU04DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1GU04YEAR	NRND	WCSP	YEA	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1GU04YEPR	NRND	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1GU04YZAR	NRND	WCSP	YZA	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1GU04YZPR	ACTIVE	WCSP	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1GU04YZTR	ACTIVE	DSBGA	YZT	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1GU04YZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

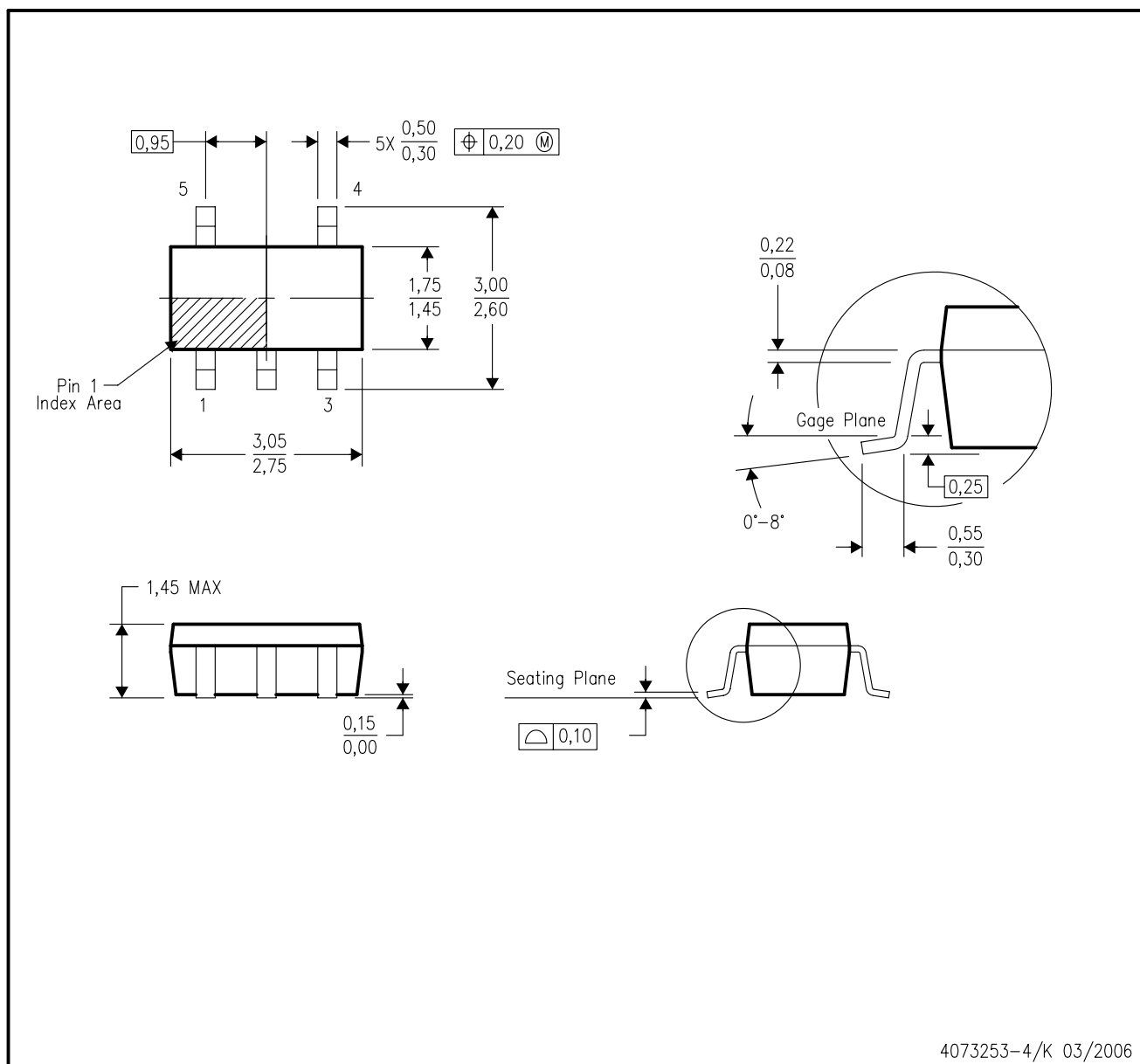
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBV (R-PDSO-G5)

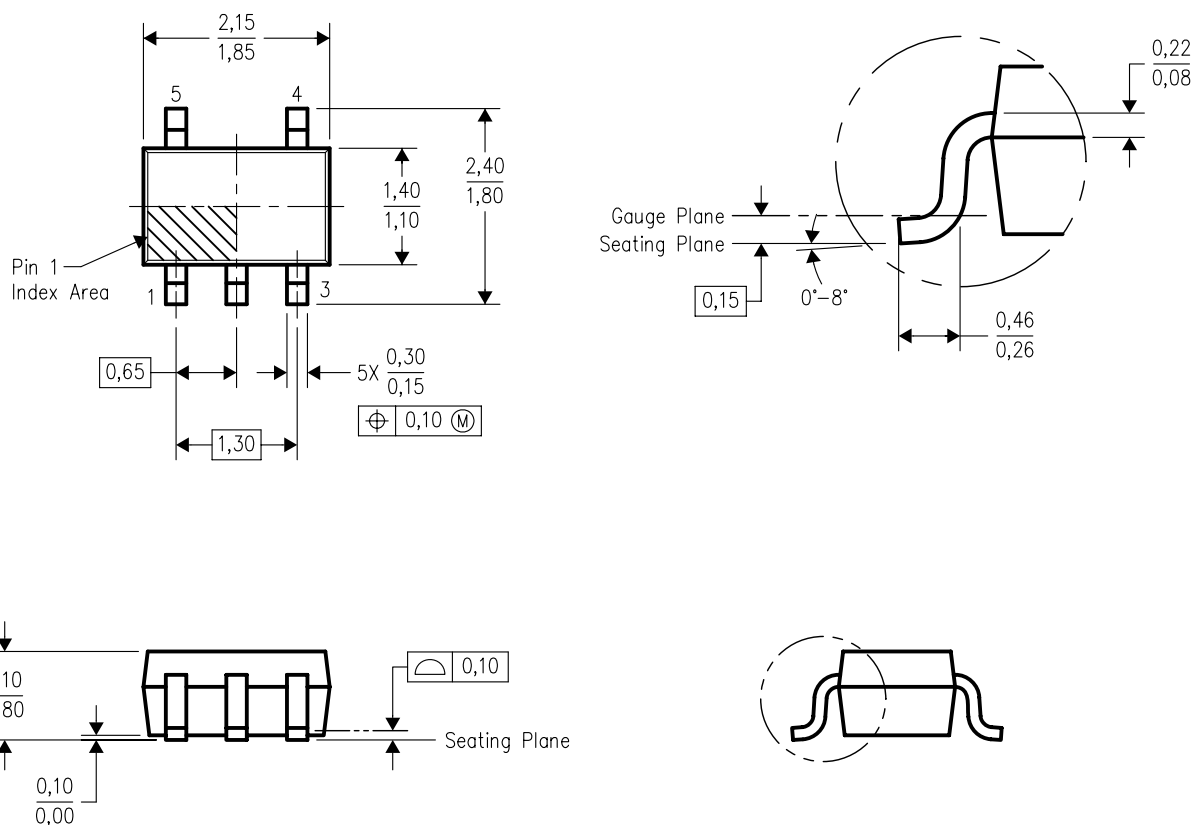
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

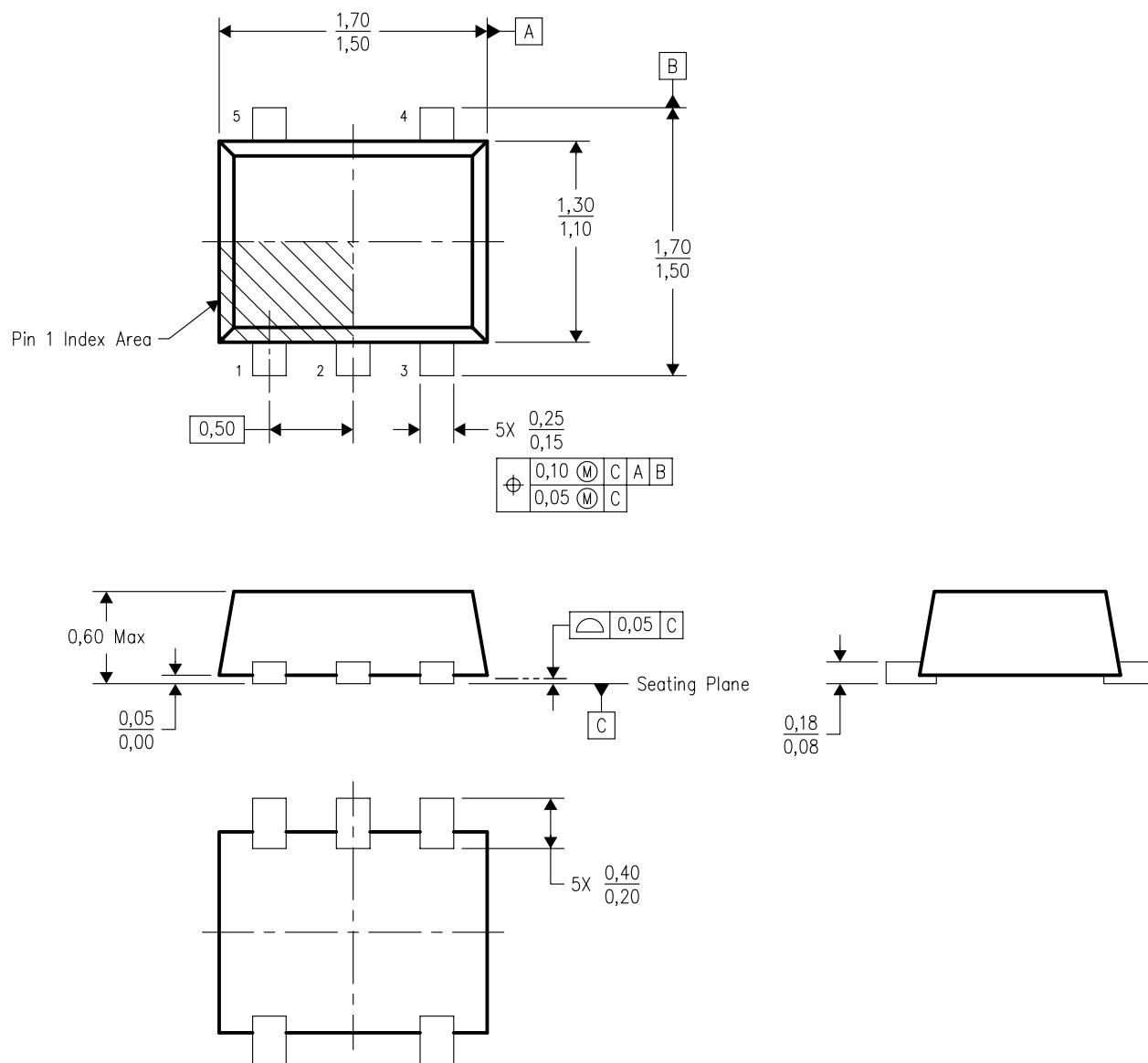
DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/F 07/2006

- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

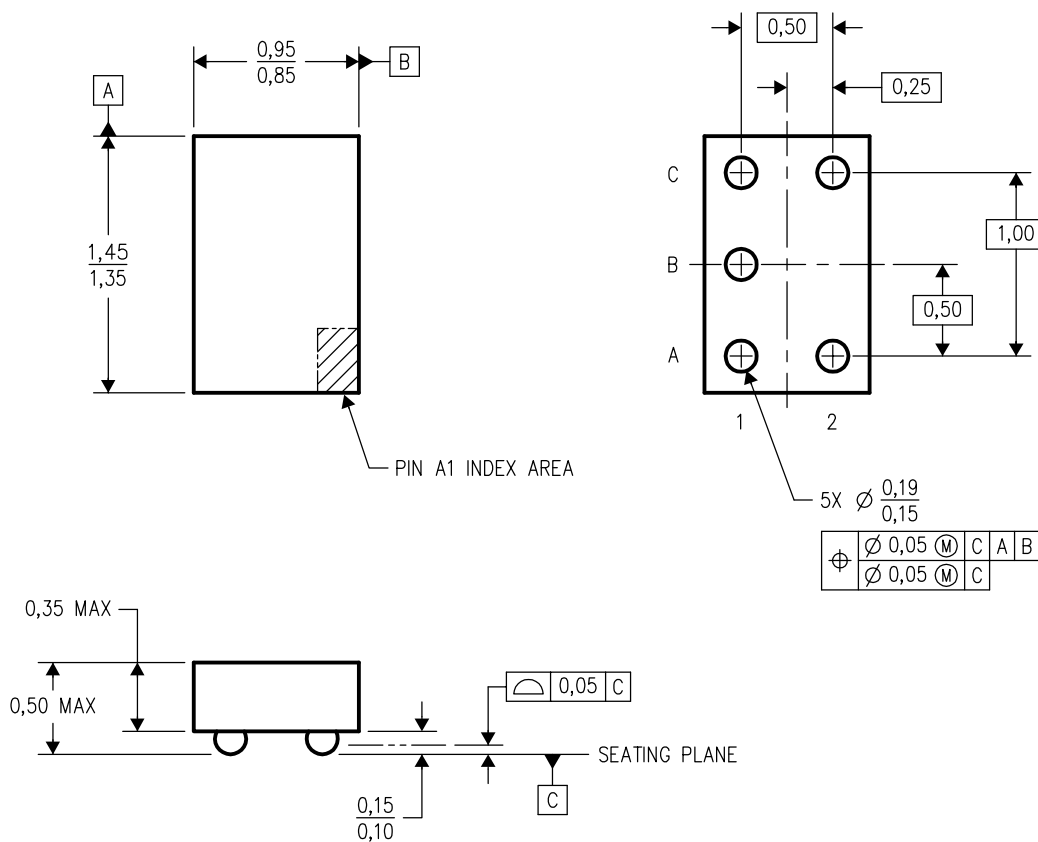


4205622-2/B 07/2004

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. JEDEC package registration is pending.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



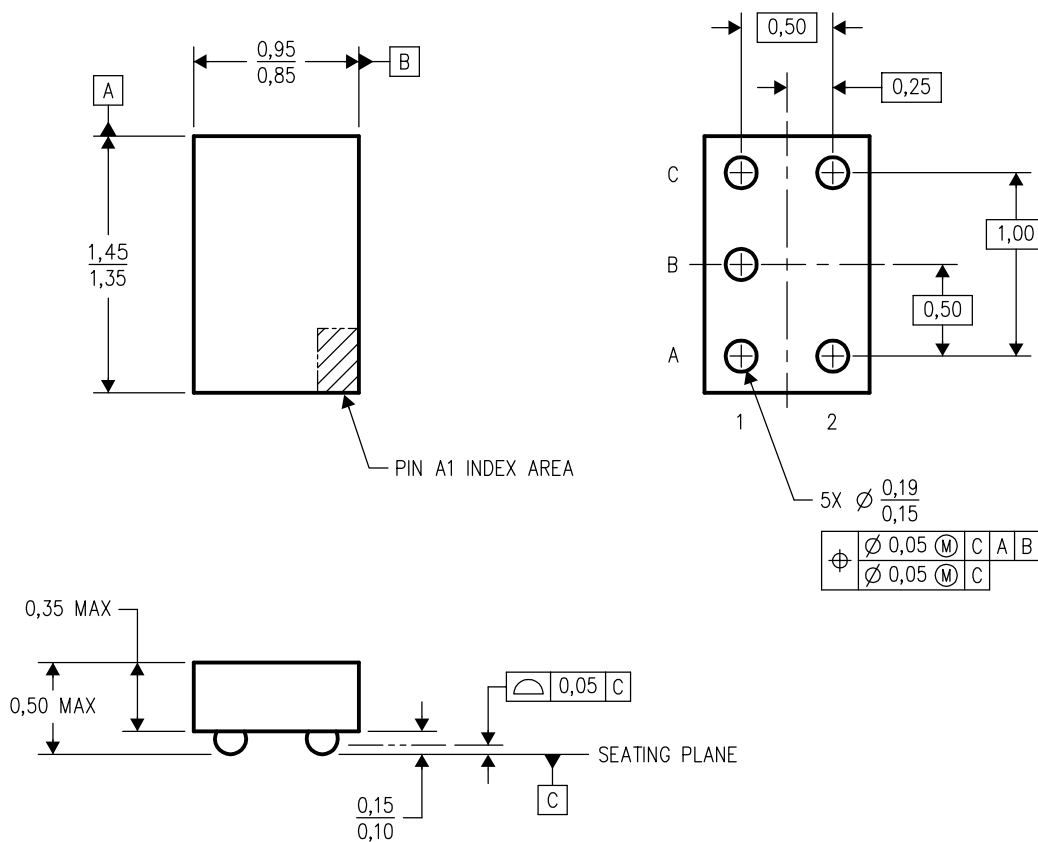
4203167-2/C 04/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoStar™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



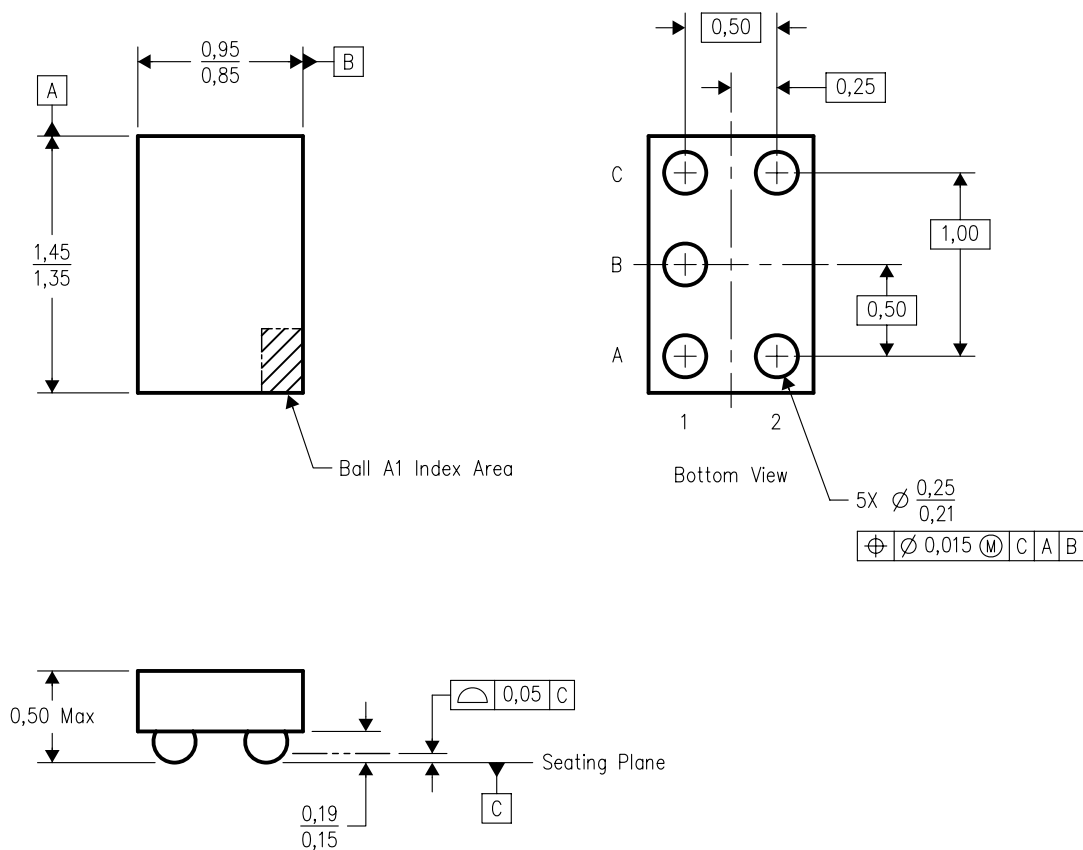
4204151-2/B 03/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



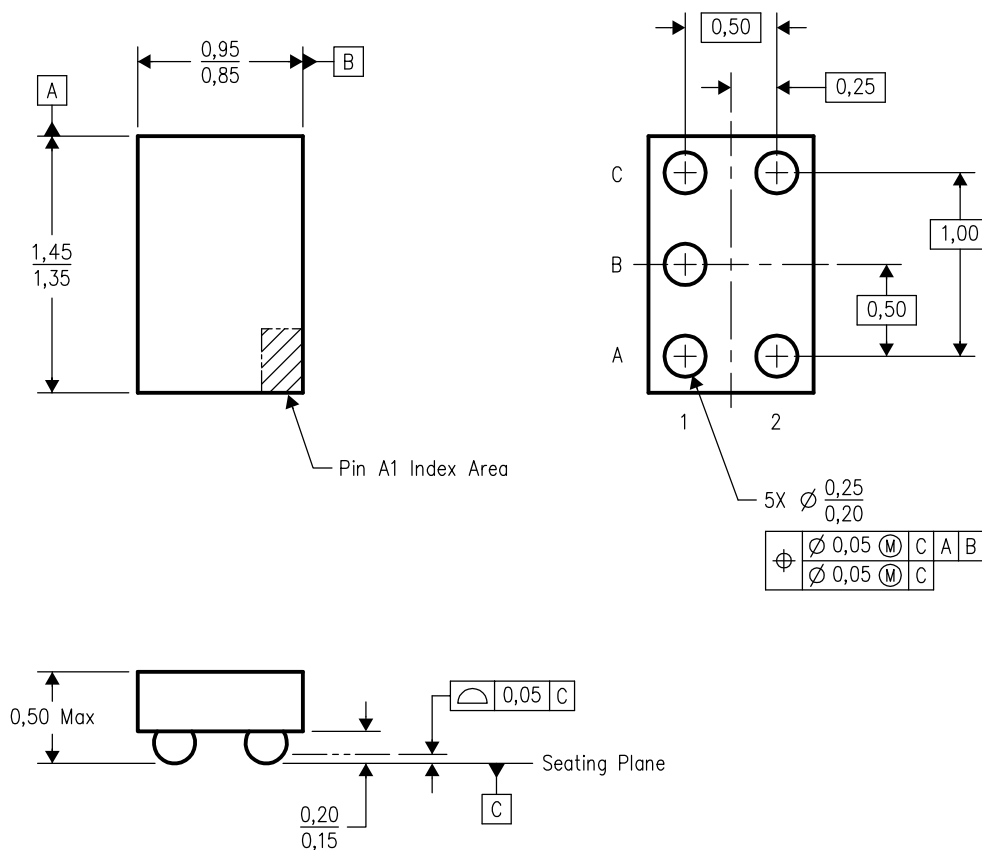
4204741-2/D 10/2006

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



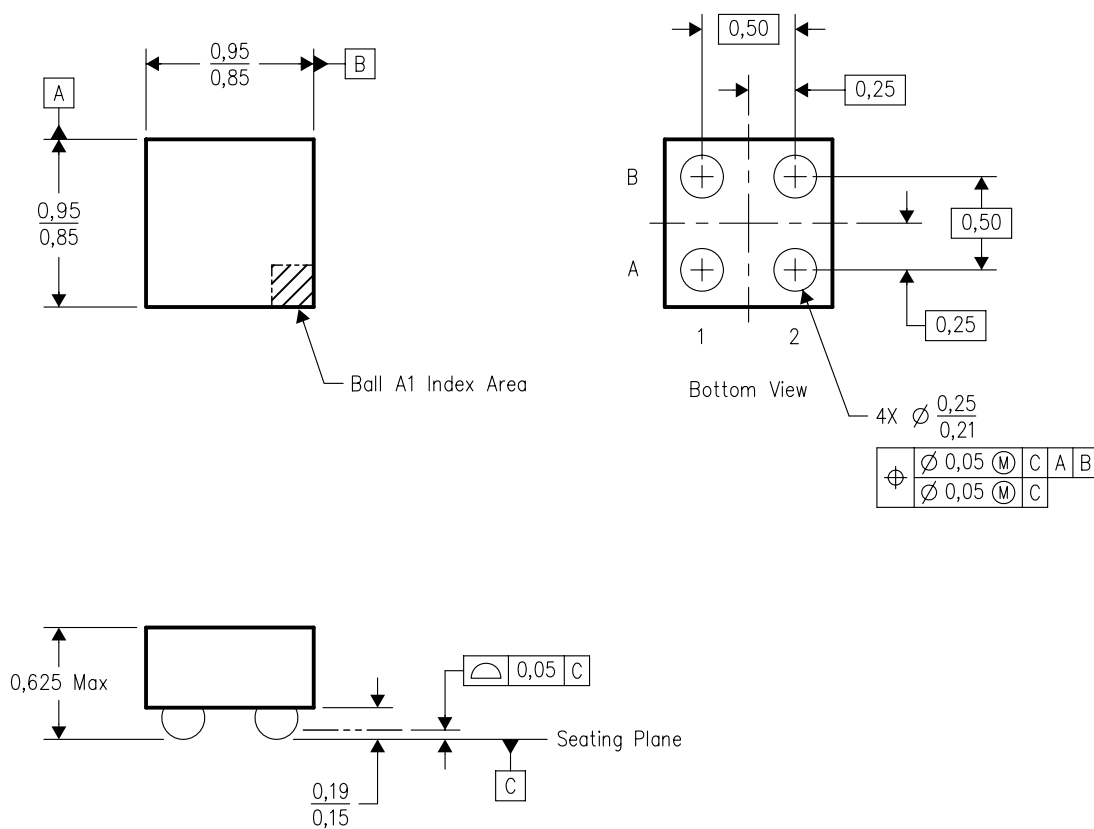
4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZT (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



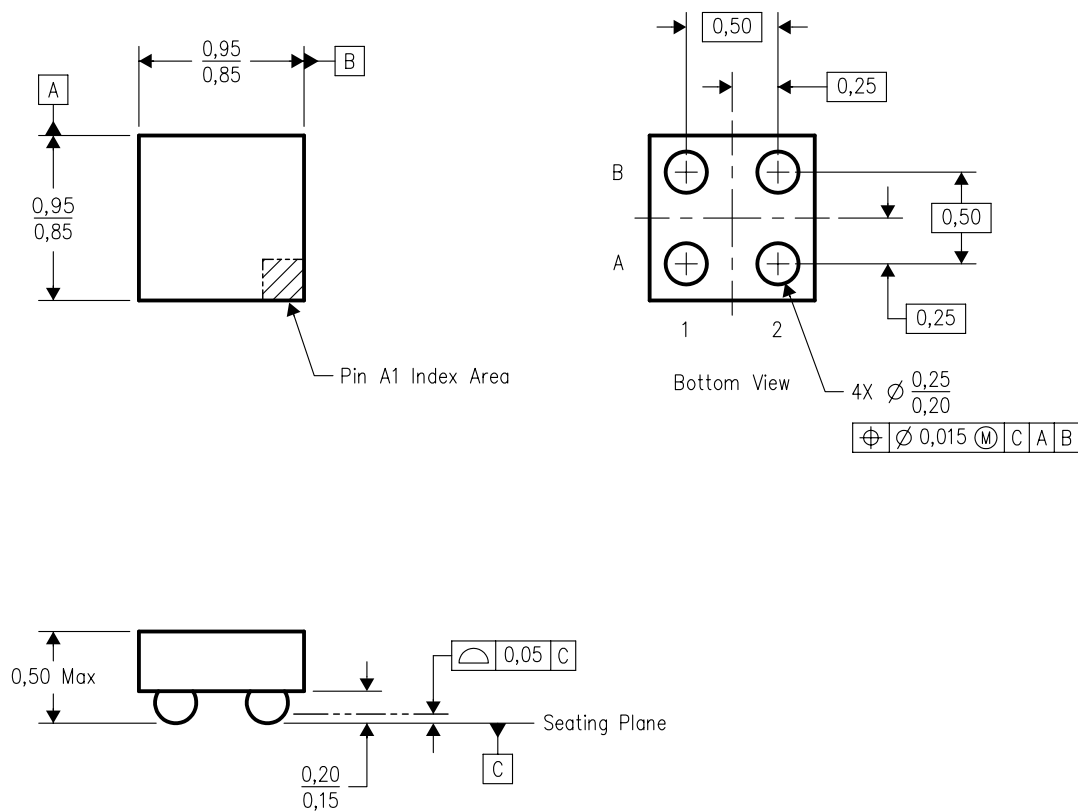
4205418-2/F 10/2006

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - This package is Lead-free. Refer to the 4 YET package (drawing 4205421) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4206083/A 05/2004

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package contains lead-free balls. Refer to the 4 YEV package (drawing 4206082) for tin-lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

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