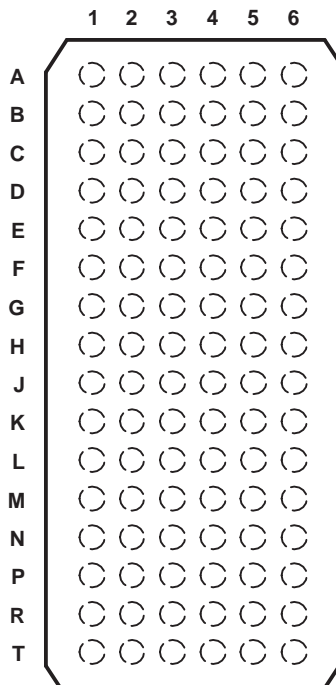


FEATURES

- Member of Texas Instruments Widebus+™ Family
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation (5-V Input/Output Voltage With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

GKE OR ZKE PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1Y2	1Y1	1 \overline{OE}	2 \overline{OE}	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	1 V_{CC}	1 V_{CC}	2A1	2A2
D	2Y4	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	1 V_{CC}	1 V_{CC}	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	4 \overline{OE}	3 \overline{OE}	4A4	4A3
J	5Y2	5Y1	5 \overline{OE}	6 \overline{OE}	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	2 V_{CC}	2 V_{CC}	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	2 V_{CC}	2 V_{CC}	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	8 \overline{OE}	7 \overline{OE}	8A4	8A3

DESCRIPTION/ORDERING INFORMATION

The SN74LVT32240 is a 32-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. The device provides inverted outputs and symmetrical active-low output-enable (\overline{OE}) inputs. It is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA – GKE	SN74LVTH32240GKER	VJ240
	LFBGA – ZKE (Pb-free)	SN74LVTH32240ZKER	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN74LVT32240
3.3-V ABT 32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCBS747D—SEPTEMBER 2000—REVISED NOVEMBER 2006

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

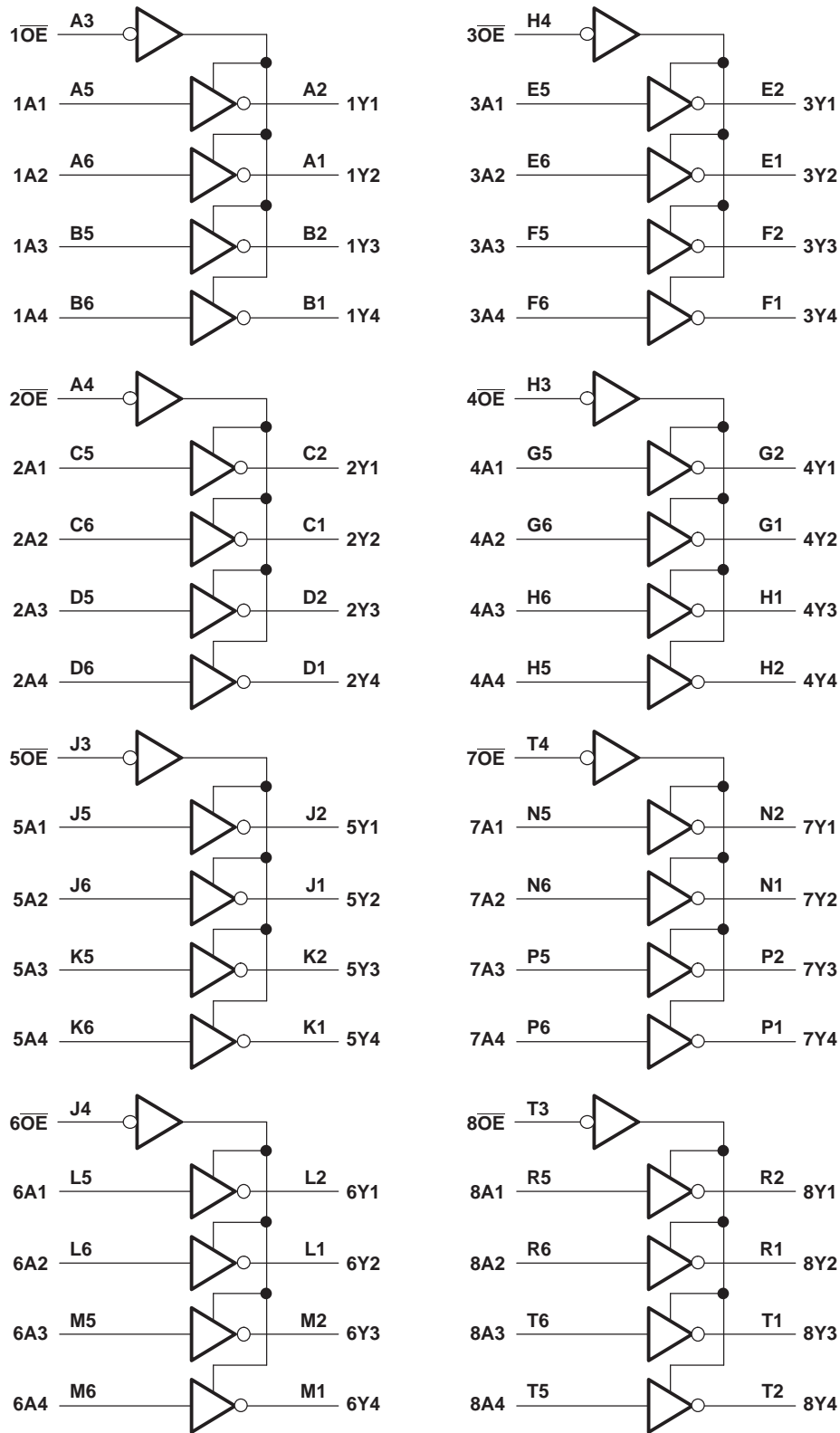
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74LVT32240

3.3-V ABT 32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS747D–SEPTEMBER 2000–REVISED NOVEMBER 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	7	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	
V_O	Voltage range applied to any output in the high state ⁽²⁾	-0.5	$V_{CC} + 0.5$	
I_O	Current into any output in the low state		128	mA
I_O	Current into any output in the high state ⁽³⁾		64	
I_{IK}	Input clamp current	$V_I < 0$	-50	
I_{OK}	Output clamp current	$V_O < 0$	-50	
θ_{JA}	Package thermal impedance ⁽⁴⁾	GKE/ZKE package		40 °C/W
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	2		
V_{IL}	Low-level input voltage		0.8	
V_I	Input voltage		5.5	
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10 ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		µs/V
T_A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 2.7\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$			
		$V_{CC} = 2.7\text{ V}$,	$I_{OH} = -8\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}$,	$I_{OH} = -32\text{ mA}$	2			
V_{OL}		$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
			$I_{OL} = 24\text{ mA}$			0.5	
		$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4	
			$I_{OL} = 32\text{ mA}$			0.5	
			$I_{OL} = 64\text{ mA}$			0.55	
I_I		$V_{CC} = 0\text{ or }3.6\text{ V}$,	$V_I = 5.5\text{ V}$			10	$\mu\text{ A}$
	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}\text{ or GND}$			± 1	
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$			1	
$V_I = 0$					-5		
I_{off}	$V_{CC} = 0$,	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100	
I_{OZH}	$V_{CC} = 3.6\text{ V}$,	$V_O = 3\text{ V}$				5	
I_{OZL}	$V_{CC} = 3.6\text{ V}$,	$V_O = 0.5\text{ V}$				-5	
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$					± 100	
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$					± 100	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high				0.38	mA
		Outputs low				10	
		Outputs disabled				0.38	
$\Delta I_{CC}^{(2)}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$					0.2	
C_i	$V_I = 3\text{ V or }0$				4	pF	
C_o	$V_O = 3\text{ V or }0$				9		

 (1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

 (2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN74LVT32240
3.3-V ABT 32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCBS747D–SEPTEMBER 2000–REVISED NOVEMBER 2006

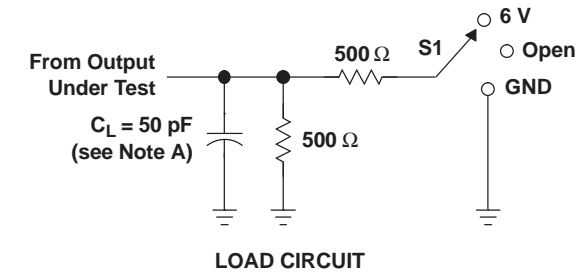
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

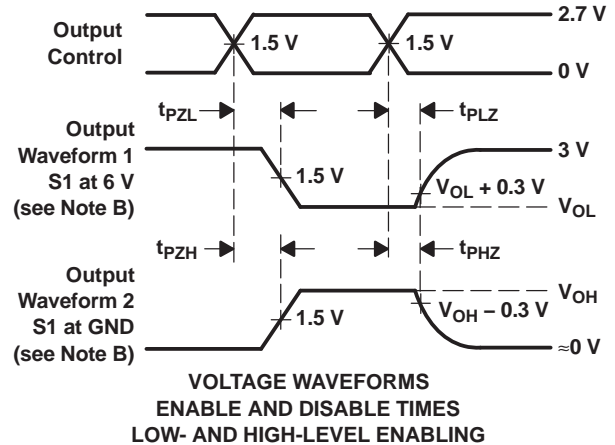
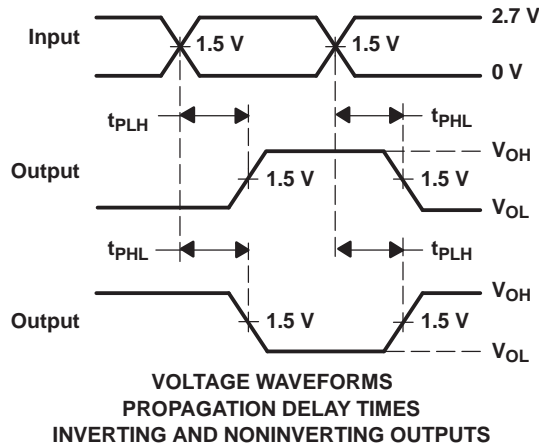
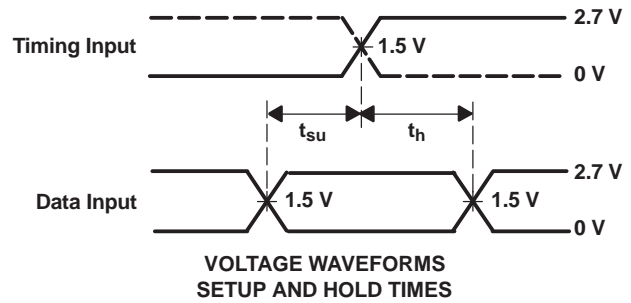
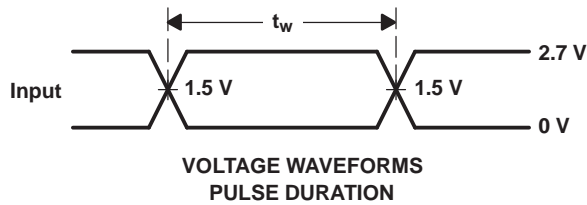
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.2	3.5	4		ns
t_{PHL}			1	2.7	3.5	4		
t_{PZH}	\overline{OE}	Y	1	2.6	4	4.9		ns
t_{PZL}			1.2	2.6	4.4	4.6		
t_{PHZ}	\overline{OE}	Y	2	3.4	4.5	5		ns
t_{PLZ}			2	3.2	4.2	4.2		
$t_{sk(LH)}$					0.5	0.5		ns
$t_{sk(HL)}$					0.5	0.5		

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVT32240GKER	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT32240GKER	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT32240GKER	LFBGA	GKE	96	1000	346.0	346.0	41.0

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

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