REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make corrections to waveforms. Update boilerplate. - CFS	00-06-12	Monica L. Poelking
B	Add device type 02. Add vendor CAGE F8859. Add section 1.5, radiation features. Correct t_{OSHL} and t_{OSLH} on waveforms in figure 5. Add table III, delta limits. Update the boilerplate to include radiation hardness assured requirements. - jak	04-03-30	Thomas M. Hess

REV																				
SHEET																				
REV	B	B	B																	
SHEET	15	16	17																	

REV STATUS OF SHEETS																
REV	B	B	B	B	B	B	B	B	B	B	B	B	A	B	B	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

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DRAWING APPROVAL DATE
93-07-23

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, TRIPLE 3-INPUT NAND GATE, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92182**

SHEET 1 OF 17

DSCC FORM 2233
APR 97

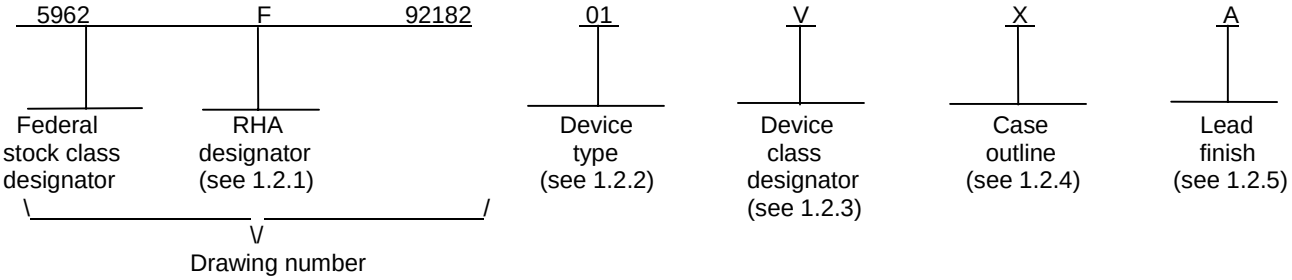
5962-E104-04

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels an+d are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACTQ10	Triple 3-input NAND gate, TTL compatible inputs
02	54ACT10	Triple 3-input NAND gate, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier
X	CDFP3-F14	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK}) (V_{IN} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output current (I_{OUT}) per output pin	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) per pin	±150 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds):	
Device type 01	+300°C
Device type 02	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	+0.8 V
Minimum high level input voltage (V_{IH})	+2.0 V
Case operating temperature range (T_C)	-55°C to +125°C
Input edge rate ($\Delta V/\Delta t$) maximum:	
(from V_{IN} = 0.8 V to 2.0 V, 2.0 V to 0.8 V)	125 mV/ns
Maximum high level output current (I_{OH})	-24.0 mA
Maximum low level output current (I_{OL})	+24.0 mA

1.5 Radiation features.

Device type 02:	
Total dose (dose rate = 50 – 300 rads (Si)/s)	300 krads (Si)
Single Event Latchup (SEL) or Single Event Upset (SEU)	≥ 93 MeV-cm^2/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA/JEDEC Standard No. 78 - IC Latch-Up Test

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.40		V
	V_{OH2}		All All	5.5 V	1, 2, 3	5.40		
	V_{OH3}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -24 mA	All All	4.5 V	1	3.86		
					2, 3	3.70		
	V_{OH4}		All All	5.5 V	1	4.86		
					2, 3	4.70		
	V_{OH5} 6/	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA	All All	4.5 V	1, 2, 3		0.10	V
	V_{OL2}		All All	5.5 V	1, 2, 3		0.10	
	V_{OL3}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 24 mA	All All	4.5 V	1		0.36	
					2, 3		0.50	
	V_{OL4}		All All	5.5 V	1		0.36	
					2, 3		0.50	
	V_{OL5} 6/	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 1 mA	All Q, V	GND	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -1 mA	All Q, V	Open	1	-0.4	-1.5	V
Input current high 3010	I_{IH}	For input under test, V_{IN} = V_{CC} For all other inputs, V_{IN} = V_{CC} or GND	All All	5.5 V	1		+0.1	µA
					2, 3		+1.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Input current low 3009	I_{IL}	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND	All All	5.5 V	1		-0.1	µA
					2, 3		-1.0	
Input capacitance 3012	C_{IN}	T_C = +25°C See 4.4.1c	All All	GND	4		10.0	pF
Power dissipation capacitance	C_{PD} 7/		All All	5.0 V	4		90.0	pF
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 8/	For input under test, $V_{IN} = V_{CC} - 2.1\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	01 All	5.5 V	1		1.0	mA
					2, 3		1.6	
			02 All	5.5 V	1, 2, 3		1.6	
Quiescent supply current output high 3005	I_{CCH}	For all inputs affecting output under test, $V_{IN} = V_{CC}$ or GND	All All	5.5 V	1		4.0	µA
					2, 3		80.0	
		M, D, P, L, R, F 9/	02 Q, V		1		50.0	
Quiescent supply current output low 3005	I_{CCL}	For all inputs affecting output under test, $V_{IN} = V_{CC}$ or GND	All All	5.5 V	1		4.0	µA
					2, 3		80.0	
		M, D, P, L, R, F 9/	02 Q, V		1		50.0	
Low level ground bounce noise	V_{OLP} 10/	T_C = +25°C See figure 4 See 4.4.1c	All All	5.0 V	4		1500	mV
Low level ground bounce noise	V_{OLV} 10/		All All	5.0 V	4		-1200	mV
High level V_{CC} bounce noise	V_{OHP} 10/		01 All	5.0 V	4		V_{OH} + 1000	mV
			02 All				V_{OH} + 1700	
High level V_{CC} bounce noise	V_{OHV} 10/		01 All	5.0 V	4		V_{OH} - 1000	mV
			02 All				V_{OH} - 1700	
Latch-up input/output over-voltage	I_{CC} (O/V1) 11/	$t_w \ge 100$ µs $t_{cool} \ge t_w$ 5 µs $\le t_r \le$ 5 ms 5 µs $\le t_f \le$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V V_{over} = 10.5 V	All Q, V	5.5 V	2		200	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Latch-up input/output positive over-current	I_{CC} (O/I1+) 11/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$	All Q, V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I_{CC} (O/I1-) 11/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$	All Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 11/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$	All Q, V	5.5 V	2		100	mA
Functional tests 3014	12/	$V_{IN} = 2.0\ V$ or $0.8\ V$ Verify output V_O See 4.4.1b	All	4.5 V	7, 8	L	H	
			All	5.5 V	7, 8	L	H	
Propagation delay time, data to output, An, Bn, Cn to On 3003	t_{PLH}, t_{PHL} 13/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 5	01 Q, V	4.5 V	9, 11	2.0	8.0	ns
					10	2.0	9.5	
			01 M		9	2.0	8.0	
					10, 11	2.0	9.5	
			02 All		9	2.0	9.0	
					10, 11	2.0	10.0	
Output skew	t_{OSHL}, t_{OSLH} 14/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 5	01 All	4.5 V	9, 10, 11		1.0	ns

1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table herein. Output terminals not designated shall be high level logic, low level logic, or open except for the I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing the I_{CC} and ΔI_{CC} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 02 meet all levels M, D, P, L, R, and F of irradiation; however, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements and any RHA level for any device, $T_A = +25\ °C$.

4/ The word "All" in the device type and device class column, means limits for all device types and classes.

TABLE I. Electrical performance characteristics – Continued.

5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

6/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

7/ Power dissipation capacitance (C_{PD}) determines the power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC}) f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the current consumption $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$. For both P_D and I_S, n is the number of device inputs at TTL levels; f is the frequency of the input signal; d is the duty cycle of the input signal; and C_L is the external output load capacitor.

8/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method; the maximum limits is equal to the number of inputs at a high TTL input level times 1.0 mA or 1.6 mA, as applicable; and the preferred method and limits are guaranteed.

9/ The maximum limit for this parameter at 100 krads (Si) is 4 µA.

10/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The device manufacturer shall determine the values of these decoupling capacitors. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

11/ See EIA/JEDEC STD. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ±5 percent.

12/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerance in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For output measurements, L < 2.5 V, H ≥ 2.5 V.

13/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guard-banding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

14/ This parameter shall be guaranteed, if not tested, to the limits specified in table I, herein. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either high-to-low (t_{OSHL}) or low-to-high (t_{OSLH}).

Device types	01, 02	
Case outlines	C, D, X	2
Terminal number	Terminal symbol	
1	A0	NC
2	B0	A0
3	A1	B0
4	B1	A1
5	$\overline{C1}$	NC
6	$\overline{O1}$	B1
7	GND	NC
8	$\overline{O2}$	$\overline{C1}$
9	C2	$\overline{O1}$
10	B2	GND
11	$\overline{A2}$	NC
12	$\overline{O0}$	$\overline{O2}$
13	C0	C2
14	V_{CC}	B2
15	---	NC
16	---	A2
17	---	$\overline{NC}$
18	---	$\overline{O0}$
19	---	C0
20	---	V_{CC}

NC = No connection

Pin description	
Terminal symbol	Description
$\overline{An}$, Bn, Cn (n = 0 to 2)	Data inputs
$\overline{On}$ (n = 0 to 2)	Outputs (inverting)

FIGURE 1. Terminal connections.

Device types 01, 02			
Inputs			Output
An	Bn	Cn	$\overline{On}$
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

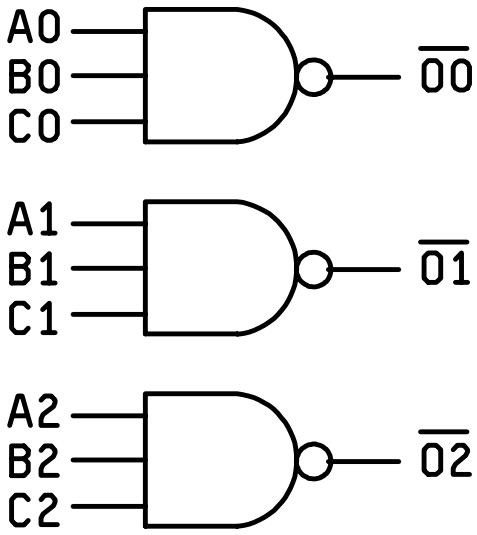
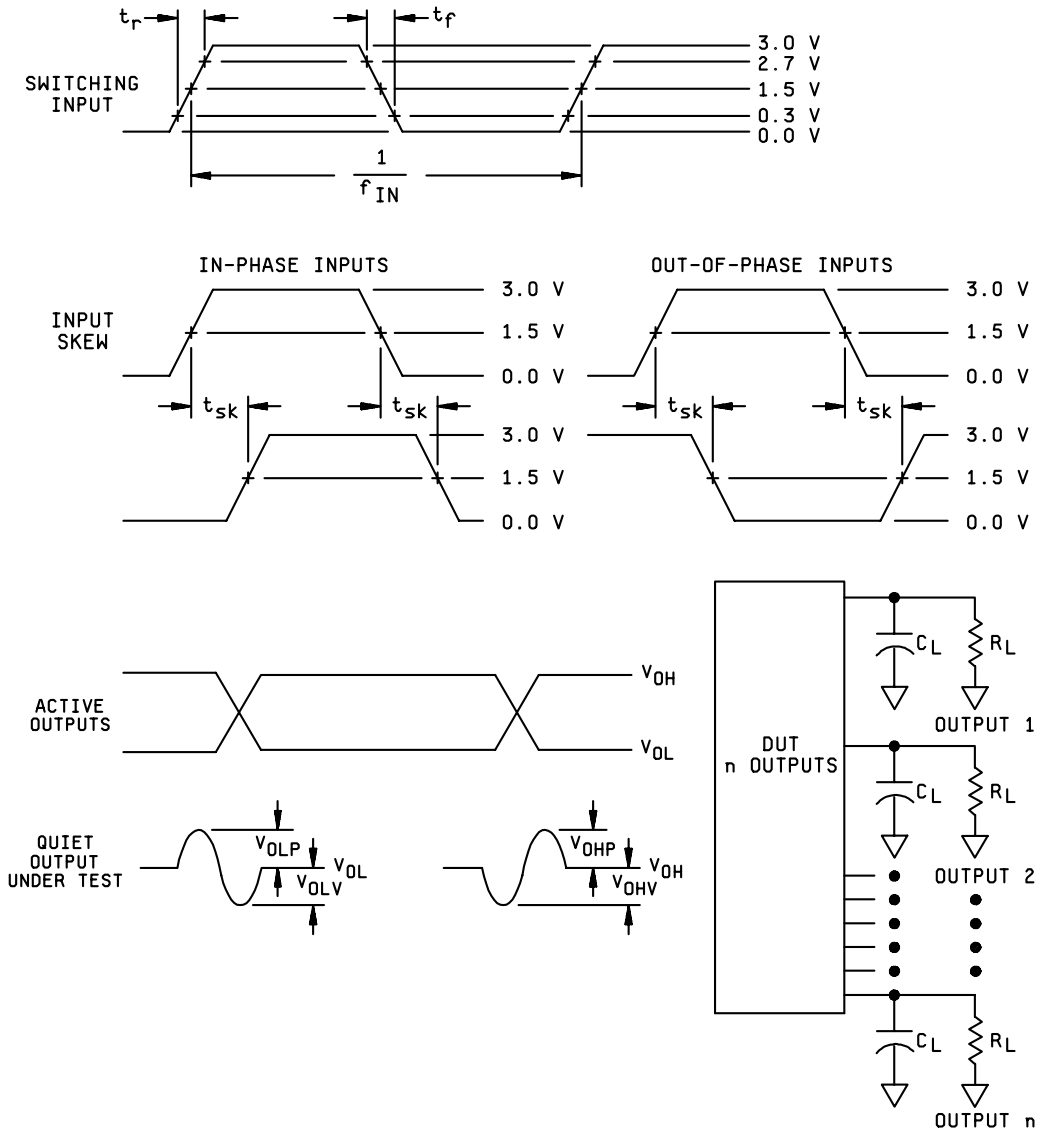


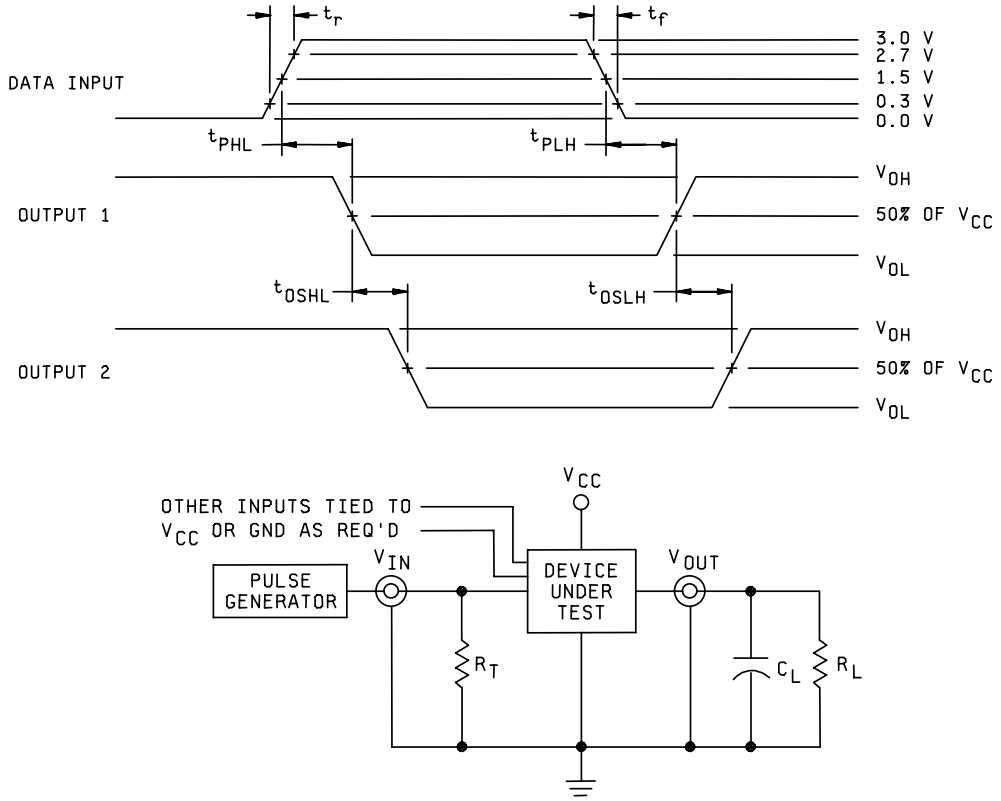
FIGURE 3. Logic diagram.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3.0 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching input signals (tsk): ≤ 250 ps.

FIGURE 4. Ground bounce waveforms and test circuit.



NOTES:

1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_T = 50Ω, R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7, and deltas.
3/ Delta limits, as specified in table III, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta limits
Supply current	I_{CC}	02	±150 nA
Supply current delta	ΔI_{CC}	02	±0.4 mA
Input current low level	I_{IL}	02	±20 nA
Input current high level	I_{IH}	02	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = 24 mA)	V_{OL}	02	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	02	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN
DATE: 04-03-30

Approved sources of supply for SMD 5962-92182 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9218201MCA	27014 01295	54ACTQ10DMQB SNJ54ACT10J
5962-9218201MDA	27014 01295	54ACTQ10FMQB SNJ54ACT10W
5962-9218201M2A	27014 01295	54ACTQ10LMQB SNJ54ACT10FK
5962-9218202QXA	F8859	54ACT10K02Q
5962-9218202QXC	F8859	54ACT10K01Q
5962-9218202VXA	F8859	54ACT10K02V
5962-9218202VXC	F8859	54ACT10K01V
5962F9218202QXA	F8859	RHFACT10K02Q
5962F9218202QXC	F8859	RHFACT10K01Q
5962F9218202VXA	F8859	RHFACT10K02V
5962F9218202VXC	F8859	RHFACT10K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - FRANCE