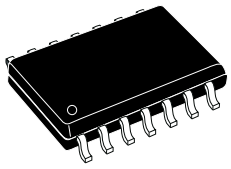
M41TC8025

Highly accurate, temperature-compensated serial real-time clock (RTC) with embedded crystal

Datasheet - production data



SO14
14-pin SOIC

Features

- Embedded high-stability 32 KHz DTCXO
- Accuracy: ±3.8 ppm max from 0 to 50°C
- Supply voltage: 1.6 to 5.5 V
- Current: 0.8 µA typical at 3.0 V
- 400 kHz I^2C interface
- Time-of-day alarm (with interrupt)
- Fixed-cycle timer interrupt function
- Time update interrupt function
- Programmable frequency output: 1 Hz, 1 KHz and 32 KHz
- Registers for seconds, minutes, hours, day-of-week, date (day of month), month and year with automatic leap year compensation
- Programmable temperature compensation intervals: 0.5 s, 2 s (default), 10 s, 30 s

Applications

- Power meters
- Industrial applications

Description

The M41TC8025 is a serial I^2C real-time clock (RTC) incorporating temperature compensation to maintain accurate timekeeping over the extended temperature range of -45 to +70 °C or the industrial temperature range of -40 to +85 °C. In addition to providing date and time (seconds, minutes, hours, day-of-week, date (day of month), month and year), the device also provides an alarm function, fixed-cycle timer, time update interrupt and programmable frequency outputs (1 Hz, 1 KHz and 32 KHz).

The M41TC8025 is provided in a 200-mil, 14-pin SOIC package.

Table 1. Device summary

Order code	Accuracy	Package
M41TC8025AMC6F	±5.0 ppm (-40 to 85 °C) ±3.8 ppm (0 to 50 °C)	SO14
M41TC8025CMC7F(1)	±5.0 ppm (-45 to 70°C) ±3.8 ppm (0 to 50 °C)	SO14

1. Contact local ST sales office for availability.

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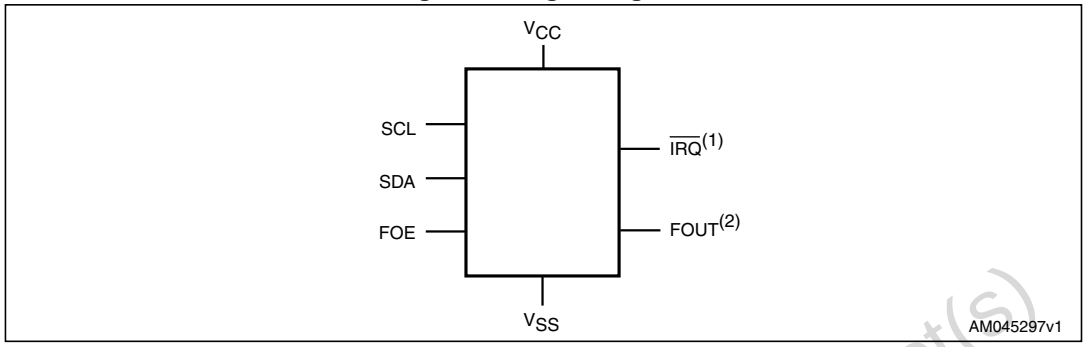
1 Device overview

Figure 1. Logic diagram



1. $\overline{IRQ}$ is an open-drain output
2. FOUT is a CMOS output

Figure 2. Pinout

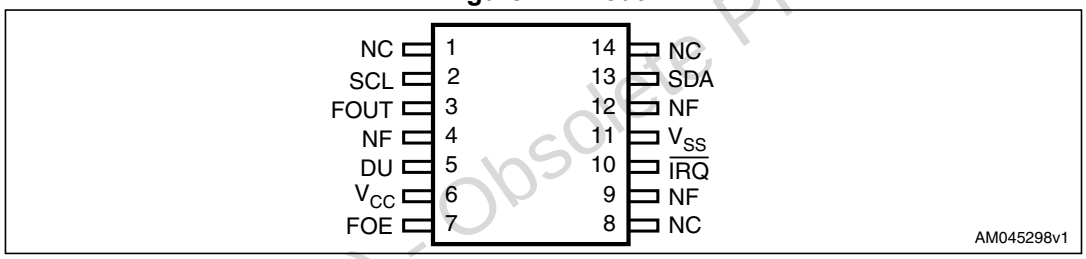


Table 2. Pin description

Pin	Name	Description
1	NC	No connect. The NC pin can be connected to V_{CC}, GND or left floating.
2	SCL	Serial clock input
3	FOUT	Programmable frequency output (CMOS). The FOUT pin is Hi-Z if FOE is low.
4	NF	No function. The NF pin can be connected to V_{CC}, GND or left floating.
5	DU	Do not use externally. The DU pin must be left floating.
6	V_{CC}	Power supply
7	FOE	Frequency output enable, controls the frequency output on FOUT pin
8	NC	No connect. The NC pin can be connected to V_{CC}, GND or left floating.
9	NF	No function. The NF pin can be connected to V_{CC}, GND or left floating.
10	$\overline{IRQ}$	Interrupt output (open drain)
11	V_{SS}	Ground supply
12	NF	No function. The NF pin can be connected to V_{CC}, GND or left floating.
13	SDA	Serial data input/output
14	NC	No connect. The NC pin can be connected to V_{CC}, GND or left floating.

Note: Be sure to connect a 0.1 µF to 1 µF bypass capacitor between V_{CC} and V_{SS}.

Figure 3. Block diagram

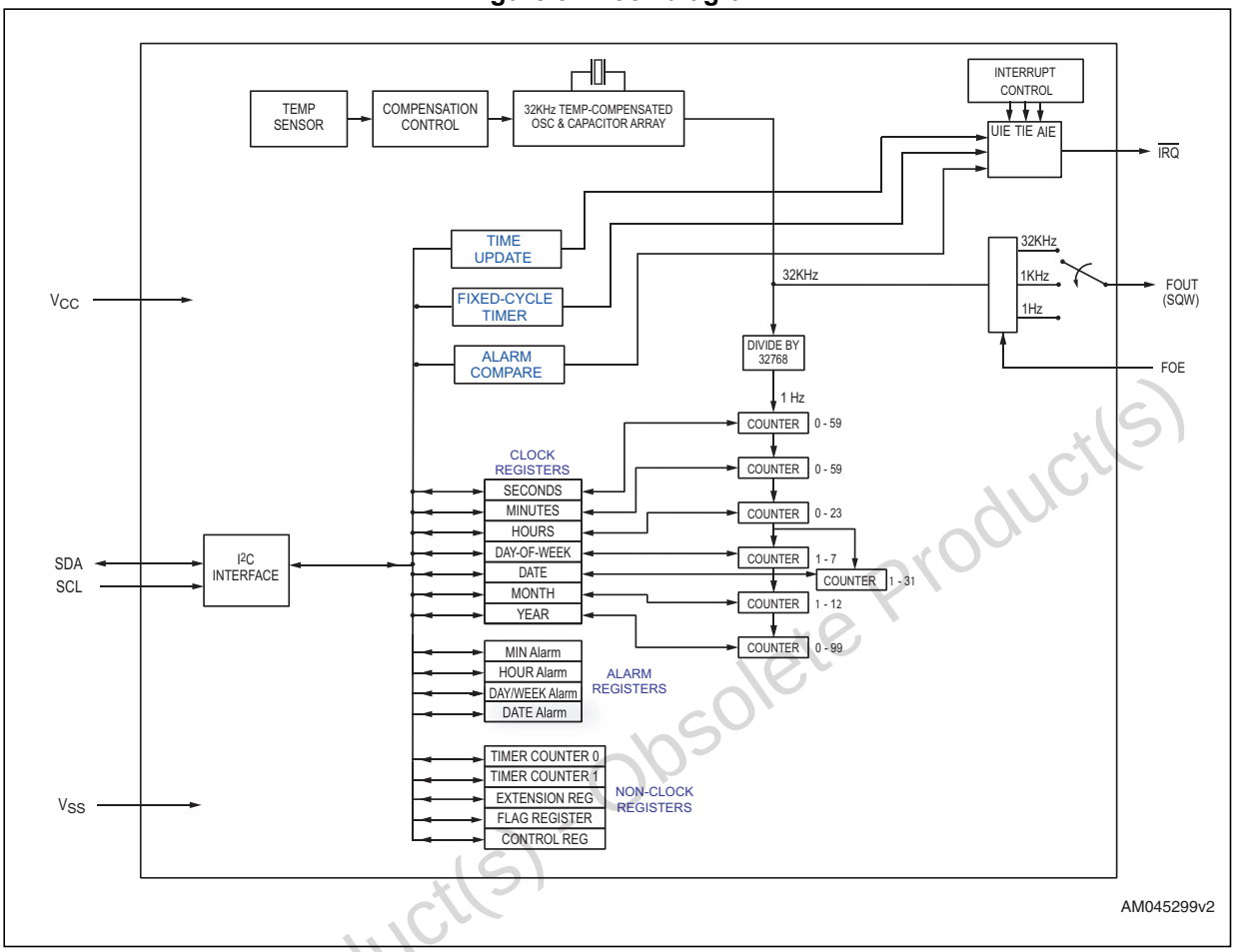
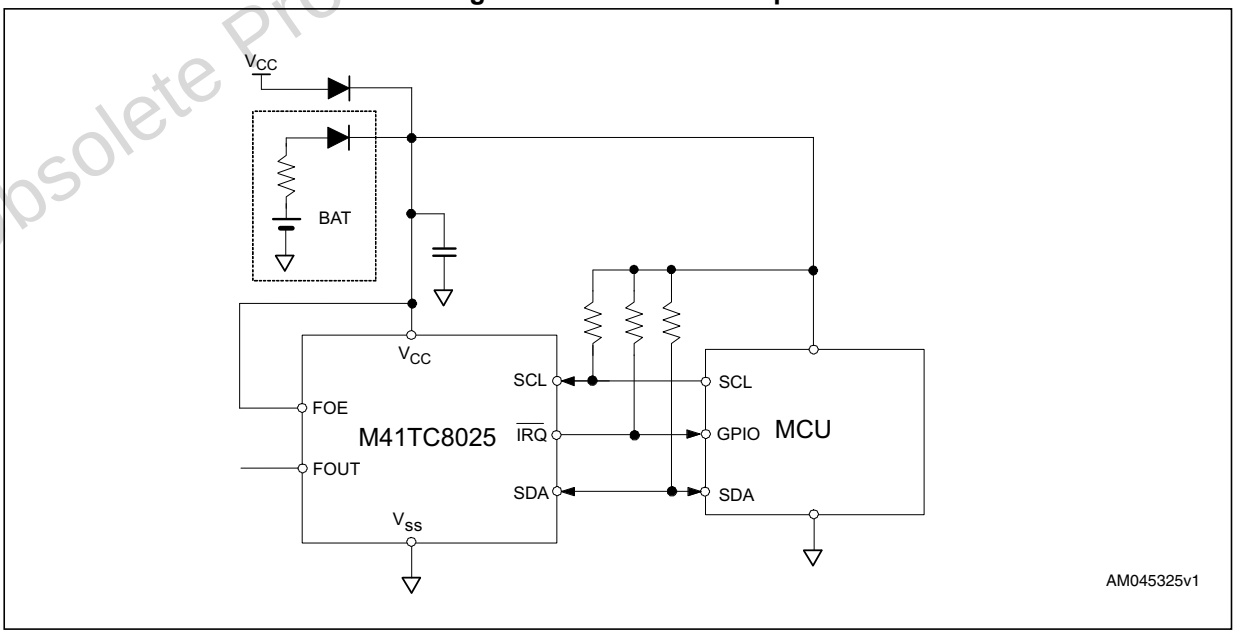


Figure 4. Hardware hookup



2 Operation

2.1 Overview of functions

2.1.1 User interface

The M41TC8025 RTC operates as a slave device on the serial I^2C bus. Access is obtained by implementing a START condition followed by the correct slave address (64h, see *Table 3 on page 11*). The 16-byte registers contained in the device can then be accessed.

2.1.2 Temperature-compensated clock and calendar

The M41TC8025 RTC provides the date and time (seconds, minutes, hours, day of week, date (day of month), month and year) while incorporating temperature compensation (sampling period user-programmable) to maintain accurate timekeeping over the extended temperature range of -45 to +70 °C or the industrial temperature range of -40 to +85 °C. Leap year is compensated automatically. Refer to *Section 2.4: Clock and calendar on page 15*.

2.1.3 Programmable clock output

The M41TC8025 RTC provides a programmable, accurate 1 Hz, 1,024 Hz (1 KHz) and 32,768 Hz (32 KHz) output on the FOUT pin. The FOUT pin is a CMOS output and is controlled by the FOE pin.

If the FOE pin is logic high, the FOUT output is enabled. If the FOE pin is logic low, the FOUT output is disabled and is Hi-Z. Refer to *Section 2.5: Programmable frequency output on FOUT pin on page 17* for a detailed description.

2.1.4 Fixed-cycle timer interrupt

The fixed-cycle timer interrupt function generates periodic interrupts at any fixed-cycle programmed between 244.14 µs and 4095 minutes.

When an interrupt is generated, the $\overline{IRQ}$ pin will be pulled low if enabled (bit TIE=1) and the flag bit (TF) will be set to 1 to indicate the interrupt occurrence. After the $\overline{IRQ}$ pin is pulled low, it will be automatically released (change to Hi-Z) after time t_{RTN} so that periodic interrupts can be generated even though the user does not clear the flag bit (no auto-clear of the flag bit). Refer to *Section 2.6: Fixed-cycle timer interrupt on page 18* for a detailed description.

2.1.5 Time update interrupt

The time update interrupt function generates periodic interrupts at one-second or one-minute cycles based on the internal clock timing update.

When a time update is generated, the $\overline{IRQ}$ pin will be pulled low if enabled (bit UIE=1) and the flag bit (UF) will be set to 1 to indicate the time update occurrence. After the $\overline{IRQ}$ pin is pulled low, it will be automatically released (change to Hi-Z) after time t_{RTN} so that periodic interrupts can be generated even if the user does not clear the flag bit (no auto-clear of the flag bit). Refer to *Section 2.7: Time update interrupt function on page 22* for a detailed description.

2.1.6 Alarm interrupt

The user can set the alarm interrupt condition in the alarm date, day, hours, and minutes registers. Once the current clock and calendar match the alarm condition, the alarm is activated so that the $\overline{IRQ}$ pin will be pulled low if enabled (bit AIE=1) and the flag bit (AF) will be set to 1 to indicate the alarm occurrence (no auto-clear of the $\overline{IRQ}$ pin nor the flag bit). Refer to *Section 2.8: Alarm interrupt function on page 25* for a detailed description.

2.2 Two-wire I^2C bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bidirectional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.2.1 Bus not busy

Both data and clock lines remain high.

2.2.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.2.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.2.4 Data valid

The state of the data line represents valid data when after a START condition; the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called "transmitter," the receiving device that gets the message is called "receiver." The device that controls the message is called "master." The devices that are controlled by the master are called "slaves."

2.2.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus transfer sequence

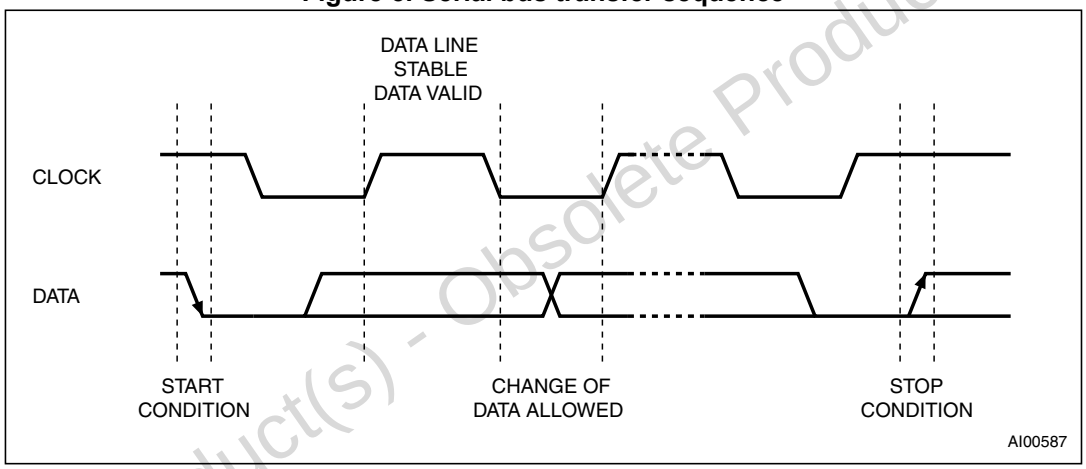
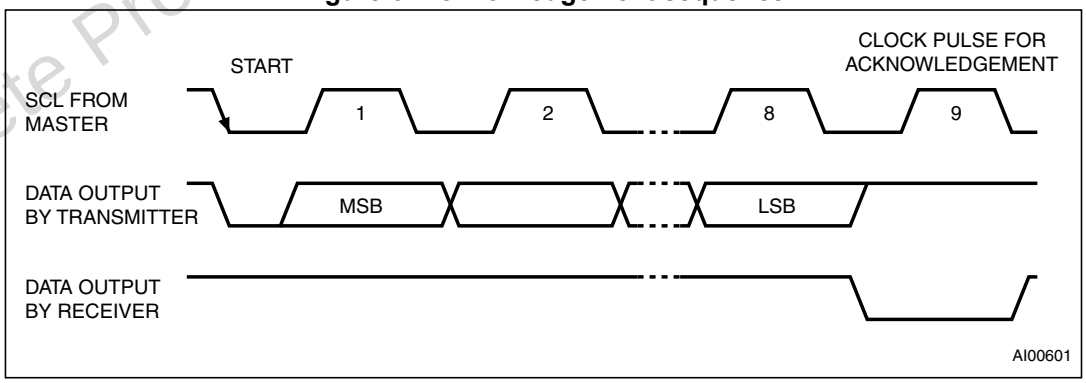


Figure 6. Acknowledgement sequence



2.2.6 READ mode

In this mode the master reads the M41TC8025 slave after setting the slave address (see *Table 3 on page 11*). Following the WRITE mode control bit (R/$\overline{W}$ = 0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$ = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41TC8025 slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to "An+2." (see *Figure 7 on page 12*).

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter. Once the address pointer reaches the register 0Fh, it will roll over to 00h automatically.

Note: The address pointer rolling over is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41TC8025 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 8 on page 12*).

Note: If an undefined register address is selected by the master, the M41TC8025 address pointer will not change. For a read command, the undefined register address will not be acknowledged and the first address that is read is the last one stored in the pointer (the M41TC8025 works in the alternate read mode). For a write command, the undefined register address will not be acknowledged and the address pointer remains unchanged.

Table 3. Slave address byte

Command	Slave address							R/$\overline{W}$
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read (65h)	0	1	1	0	0	1	0	1
Write (64h)	0	1	1	0	0	1	0	0
	MSB							LSB

Figure 7. READ mode sequence

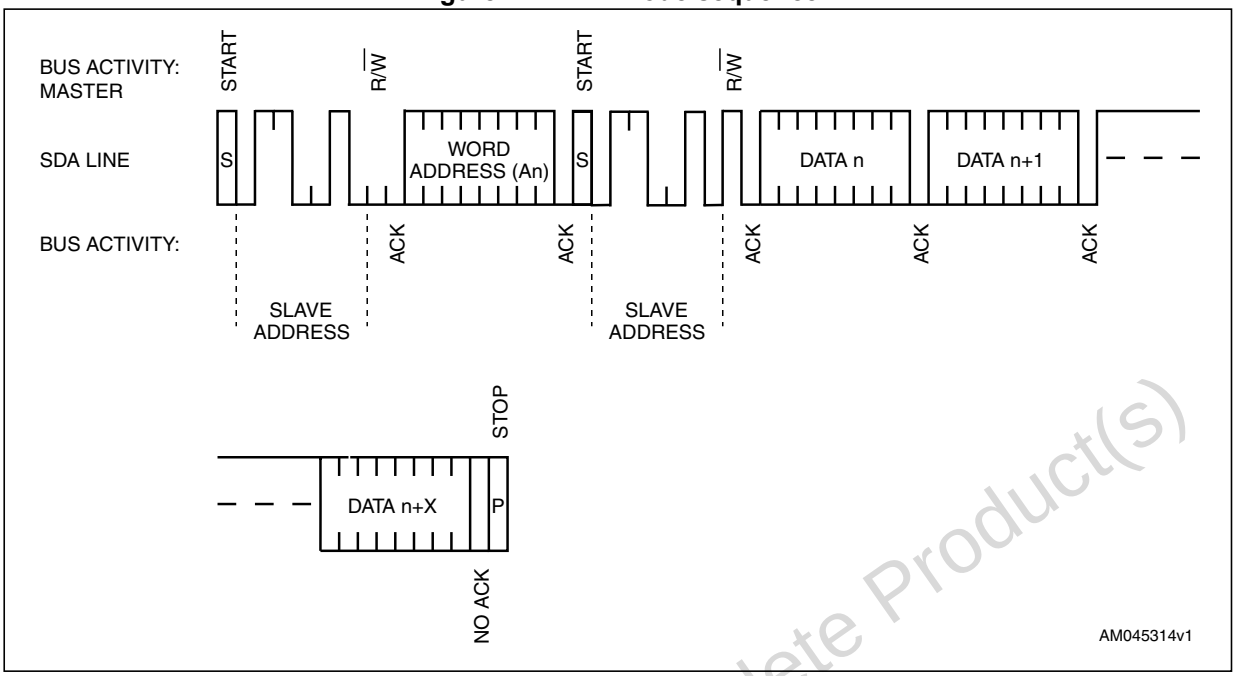
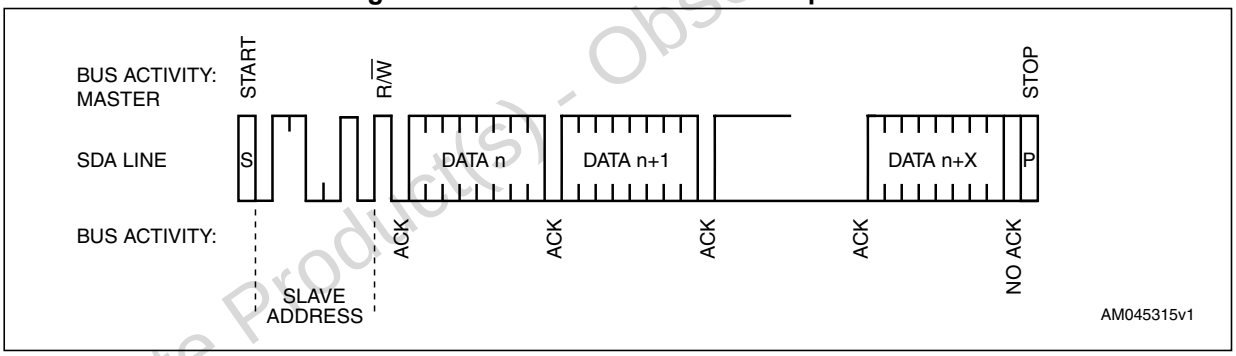


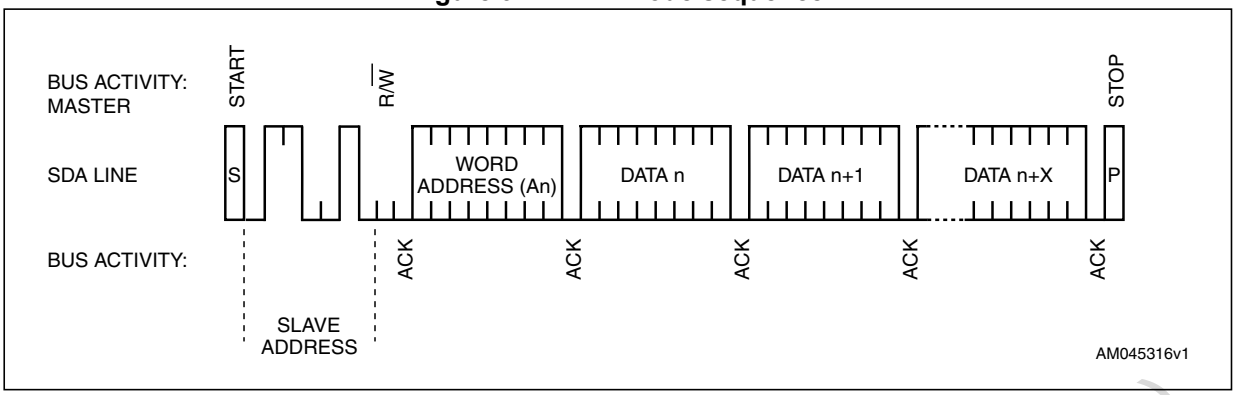
Figure 8. Alternative READ mode sequence



2.2.7 WRITE mode

In this mode the master transmitter transmits to the M41TC8025 slave receiver. Bus protocol is shown in *Figure 9 on page 13*. Following the START condition and slave address, a logic '0' ($R/\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address "An" will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41TC8025 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see *Table 3 on page 11*) and again after it has received the word address and each data byte.

Figure 9. WRITE mode sequence



2.2.8 I²C timeout function

The M41TC8025 device incorporates a timeout function for the I²C bus. When communicating with the M41TC8025 device, the series of operations from transmitting the START condition to transmitting the STOP condition should be kept within 0.95 seconds.

If the series of operations require more than 0.95 seconds, the I²C bus interface will be automatically reset to standby mode by this timeout function.

If timeout happens during a data byte transfer, the data byte being transferred (read or write) will not complete successfully. Data written into the device will not be acknowledged and the address pointer remains unchanged. If a read is in progress, the data bits after timeout will be read as 1 and the address pointer will remain unchanged.

2.3 Register description

The register map within the M41TC8025 and the default values after initial power-up are given in *Table 4 on page 14*.

Register 00h to 06h are used for the clock and calendar. Refer to *Section 2.4: Clock and calendar on page 15* for the detailed function and setting of the registers.

Register 07h is a RAM byte for the user.

Register 08h to 0Ah are alarm registers for the alarm interrupt. Refer to *Section 2.8: Alarm interrupt function on page 25* for the detailed function and setting of the registers.

Register 0Bh to 0Ch are timer registers for the fixed-cycle interrupt timer target value setting. Refer to *Section 2.6: Fixed-cycle timer interrupt on page 18* for the detailed function and setting of the registers.

Register 0Dh to 0Fh are status and control registers. The detailed function of each bit is described in each of the function sections.

Table 4. Register map and default values

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Seconds	0	40	20	10	8	4	2	1
01h	Minutes	0	40	20	10	8	4	2	1
02h	Hours	0	0	20	10	8	4	2	1
03h	Day-of-week	0	6	5	4	3	2	1	0
04h	Date (day of month)	0	0	20	10	8	4	2	1
05h	Month	0	0	0	10	8	4	2	1
06h	Year	80	40	20	10	8	4	2	1
07h	RAM	x	x	x	x	x	x	x	x
08h	Alarm minutes (default)	AM_M (1)	40	20	10	8	4	2	1
09h	Alarm hours (default)	AM_H (1)	x	20	10	8	4	2	1
0Ah	Alarm day (default)	AM_D (1)	6	5	4	3	2	1	0
	Alarm date (default)		x	20	10	8	4	2	1
0Bh	Timer counter 0	128	64	32	16	8	4	2	1
0Ch	Timer counter 1	x	x	x	x	2048	1024	512	256
0Dh	Extension register (default)	Test (0)	WADA (0)	USEL (0)	TE (0)	FSEL1 (0)	FSEL0 (0)	TSEL1 (0)	TSEL0 (0)
0Eh	Flag register (default)	0	0	UF (0)	TF (0)	AF (0)	0	VLF (1)	VDET (1)
0Fh	Control register (default)	CSEL1 (0)	CSEL0 (1)	UIE (0)	TIE (0)	AIE (0)	0	0	RESET (0)

Note: 1 After the initial power-up or when the VLF bit is read as "1", the user must initialize all the registers before using the RTC.

2 Date and time data should be configured in the correct format. Clock operations are not guaranteed if the data is incorrect.

3 Only "0" can be written to the Test, UF, TF, AF, VLF or VDET bits.

4 Any bit marked with "0" should be written as "0" after initialization and the value read from these bits are all "0".

5 Any bit marked with "x" is a RAM bit and the data written/read will not affect RTC function.

6 The test bit is only for testing by the manufacturer. The user must write 0 to TEST bit.

2.4 Clock and calendar

The M41TC8025 incorporates an accurate temperature-compensated real-time clock and calendar. The user can access at registers 00h to 06h.

2.4.1 Clock registers configuration

Table 5. Clock counters (00h to 02h)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Seconds	0	40	20	10	8	4	2	1
01h	Minutes	0	40	20	10	8	4	2	1
02h	Hours	0	0	20	10	8	4	2	1

The clock counters count seconds, minutes, and hours. The data is in BCD format. For example, the "seconds" register value "0101 1001" indicates 59 seconds.

The seconds and minutes counters count from "00" to "01", "02" and up to "59" and they roll over to "00" after that.

The hours counter counts from "00" to "01", "02" and up to "23" and it rolls over to "00" after that.

Note: Writing invalid time data may interfere with normal operation of the clock counter.

2.4.2 Calendar registers configuration

Table 6. Calendar counters (03h to 06h)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	Day-of-week	0	6	5	4	3	2	1	0
04h	Date (day of month)	0	0	20	10	8	4	2	1
05h	Month	0	0	0	10	8	4	2	1
06h	Year	80	40	20	10	8	4	2	1

In the day-of-week register, each bit (from bit 0 to bit 6) represents a different day of the week.

The day-of-week data values sequence is as follows: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc. The possible configuration in the Day-of-week register is in *Table 7* .

Table 7. Data for day-of-week

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Data [h]	Day-of-week
0	0	0	0	0	0	0	1	01h	Sunday
0	0	0	0	0	0	1	0	02h	Monday
0	0	0	0	0	1	0	0	04h	Tuesday
0	0	0	0	1	0	0	0	08h	Wednesday
0	0	0	1	0	0	0	0	10h	Thursday
0	0	1	0	0	0	0	0	20h	Friday
0	1	0	0	0	0	0	0	40h	Saturday

Note: Do not write more than one bit of "1" in the Day-of-week register.

Note: Writing invalid day-of-week data may interfere with normal operation of the calendar.

The data in the date (day of month), month and year registers are in BCD format. For example, the date register value "0011 0001" indicates 31st.

The date counter counts from "01" to "02", "03" and up to "31" and rolls over to "01" after that. The maximum date value varies according to the value in the month register which is show in *Table 8*.

Table 8. Data for date (day of month) register

Month value	Data for date (day of month) register
1, 3, 5, 7, 8, 10 or 12	01→02→…→31→01→02→…
4, 6, 9 or 11	01→02→…→30→01→02→…
February in normal year	01→02→…→28→01→02→…
February in leap year	01→02→…→29→01→02→…

Note: Leap year is whenever the year value is a multiple of four (such as 04, 08, 12…88, 92, or 96). Year 00 is not considered to be a leap year.

The month counter counts from "01" to "02", "03" and up to "12" and it rolls over to "01" after that. It represents: January, February… and December.

The year counter counts from "00" to "01", "02" and up to "99" and it rolls over to "00" after that. It may represent: year 2000, 2001… and 2099. Any year that is a multiple of four (04, 08, 12… 88, 92, 96, etc.) is automatically handled as a leap year. Year 00 is not considered to be a leap year.

2.4.3 Clock reset function

Table 9. Reset bit in control register 0Fh

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Control register	CSEL1	CSEL0	UIE	TIE	AIE	0	0	**RESET**

The RESET bit in the control register 0Fh is related to the clock counter operations.

If RESET=1, the internal clock divider below 4 KHz will be stopped and the RTC module's internal counter value will be cleared. The updating of seconds, minutes, hours, day-of-week, date (day of month), month and year registers will be stopped. As a result, the alarm function, the time update interrupt and part of the fixed-cycle interrupt (clock source <4 KHz) will be stopped.

If RESET=0, the clock divider below 4 KHz operates normally. All the updates of the clock and calendar and interrupts return to normal operation.

Once the RESET bit is set to 1, it will be automatically cleared to 0 upon a STOP condition, a RE-START condition or the 0.95 second I^2C timeout occurrence.

2.4.4 Temperature compensation

The M41TC8025 RTC incorporates a temperature sensor to monitor the device temperature and compensate the internal clock source so that accurate timekeeping over the extended temperature range of -45 to +70 °C or the industrial temperature range of -40 to +85 °C is maintained. The compensation period can be configured by the user to 0.5 s, 2 s, 10 s or 30 s. The related register bits (CSEL1 and CSEL0, highlighted in bold) are shown in *Table 10* and the detailed configuration is given in *Table 11*.

Table 10. Temperature compensation bits in control register 0Fh

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Control register	**CSEL1**	**CSEL0**	UIE	TIE	AIE	0	0	RESET

Table 11. Temperature compensation period configuration

CSEL1	CSEL0	Compensation period	Comment
0	0	0.5 s	
0	1	2 s	Default
1	0	10 s	
1	1	30 s	

2.5 Programmable frequency output on FOUT pin

The M41TC8025 RTC provides programmable accurate 1 Hz, 1,024 Hz (1 KHz) and 32,768 Hz (32 KHz) square wave output on the FOUT pin. The user can configure the output frequency through the FSEL1 and FSEL0 bits in the 0Dh register. The FOUT pin is a CMOS output and controlled by the FOE pin.

If the FOE pin is logic high, the FOUT output is enabled. If the FOE pin is logic low, the FOUT output is disabled and is Hi-Z.

Table 12. FOUT pin output frequency selection

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	Extension register	TEST	WADA	USEL	TE	**FSEL1**	**FSEL0**	TSEL1	TSEL0

The FSEL1 and FSEL0 bits in register 0Dh are for the user to select the output frequency on the FOUT pin. The frequency options are given in *Table 13*.

Table 13. FOUT frequency configuration

FSEL1	FSEL0	FOUT frequency	Comment
0	0	32,768 Hz	Default
0	1	1,024 Hz	
1	0	1 Hz	
1	1	32,768 Hz	

2.6 Fixed-cycle timer interrupt

The fixed-cycle timer interrupt function generates periodic interrupts at any fixed-cycle programmed between 244.14 µs and 4095 minutes.

When a fixed-cycle timer interrupt is generated, the $\overline{IRQ}$ pin will be pulled low if enabled (bit $\overline{TIE}$ = 1) and the flag bit (TF) will be set to 1 to indicate the interrupt occurrence. After the $\overline{IRQ}$ pin is pulled low, it will be automatically released (change to Hi-Z) after time t_{RTN} so that periodic interrupts can continue to be generated even if the user does not clear the flag bit.

The fixed-cycle timer interrupt function related registers are shown in *Table 14*.

Table 14. Fixed-cycle timer interrupt related register bits

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Timer counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0Ch	Timer counter 1	x	x	x	x	**2048**	**1024**	**512**	**256**
0Dh	Extension register	TEST	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
0Eh	Flag register	0	0	UF	**TF**	AF	0	VLF	VDET
0Fh	Control register	CSEL1	CSEL0	UIE	**TIE**	AIE	0	0	**RESET**

Note: All the fixed-cycle interrupt function related register bits are marked in bold.

2.6.1 Related registers

Register 0Bh and 0Ch are used to set the interrupt trigger value for the internal timer. It is in 12-bit binary format with a value of 1 (001h) to 4095 (FFFh).

The TE bit in register 0Dh is to start (TE=1) or stop and reset (TE=0) the internal timer. Once the timer is enabled, it will count from 000h towards the interrupt trigger value. Once the

timer value reaches the interrupt trigger value, a fixed-cycle interrupt will be triggered and the timer will automatically start to count from 000h towards the interrupt trigger value again.

The TF bit in register 0Eh is the fixed-cycle timer interrupt flag. Once the timer is enabled (TE=1) and the internal counter increment reaches the interrupt trigger value, the TF bit is set to 1 to indicate a fixed-cycle timer interrupt occurrence. Once TF=1, it will not be automatically cleared and relies on the user to reset to 0. Resetting the TF bit to 0 will release the $\overline{IRQ}$ pin from low to Hi-Z immediately, otherwise the $\overline{IRQ}$ pin is auto-released after time t_{RTN} specified in *Table 15*.

The TIE bit in register 0Fh is the interrupt enable bit. If the interrupt is enabled (TIE=1) and there is a fixed-cycle interrupt event, the $\overline{IRQ}$ pin will be pulled low. If the interrupt is disabled (TIE=0), even if there is a fixed-cycle interrupt event, the $\overline{IRQ}$ pin will remain unchanged and stay Hi-Z. The TF bit still can be set to 1, regardless of the status of the $\overline{IRQ}$ pin. Resetting the TIE bit to 0 while $\overline{IRQ}$ is low will immediately release the $\overline{IRQ}$ pin (change to Hi-Z).

The TSEL1 and TSEL0 bits in register 0Dh are used to select the internal timer counting source clock. *Table 15* shows the configuration.

Table 15. Timer source clock configuration

TSEL1	TSEL0	Clock source	Auto reset time (t_{RTN})	Effect of RESET bit
0	0	4096 Hz (once per 244.14 µs)	122 µs	Not affected
0	1	64 Hz (once per 15.625 ms)	7.8125 ms	Does not operate when RESET = 1
1	0	1 Hz (once per second)	7.8125 ms	
1	1	“minute” update (once per minute)	7.8125 ms	

Note: 1 The $\overline{IRQ}$ pin auto release time (t_{RTN}) varies according to the source clock selection.

2 When the source clock has been selected to "second update" or "minute update", the timing of both counting and interrupts is coordinated with the clock update timing.

3 When the RESET bit in control register 0Fh is 1, the clock divider <4 KHz is stopped. As a result, the fixed-cycle timer interrupt with source clocks of 64 Hz, 1 Hz and "minute" update will be stopped.

2.6.2 Fixed-cycle timer interrupt interval configuration

Table 16 gives examples of the possible periods for the fixed-cycle timer interrupt.

Table 16. Fixed-cycle timer interrupt configuration

Timer counter setting	Source clock			
	4096 Hz TSEL1,0 = 0,0	64 Hz TSEL1,0 = 0,1	"Second" update 1 Hz TSEL1,0 = 1,0	"Minute" update TSEL1,0 = 1,1
0	-	-	-	-
1	244.14 µs	15.625 ms	1 s	1 min
2	488.28 µs	31.25 ms	2 s	2 min
...	...	...	...	...
41	10.01 ms	640.63 ms	41 s	41 min
205	50.049 ms	3.203 s	205 s	205 min
410	100.1 ms	6.406 s	410 s	410 min
2048	500 ms	32 s	2048 s	2048 min
...	...	...	...	...
4095	0.9998 s	63.984 s	4095 s	4095 min

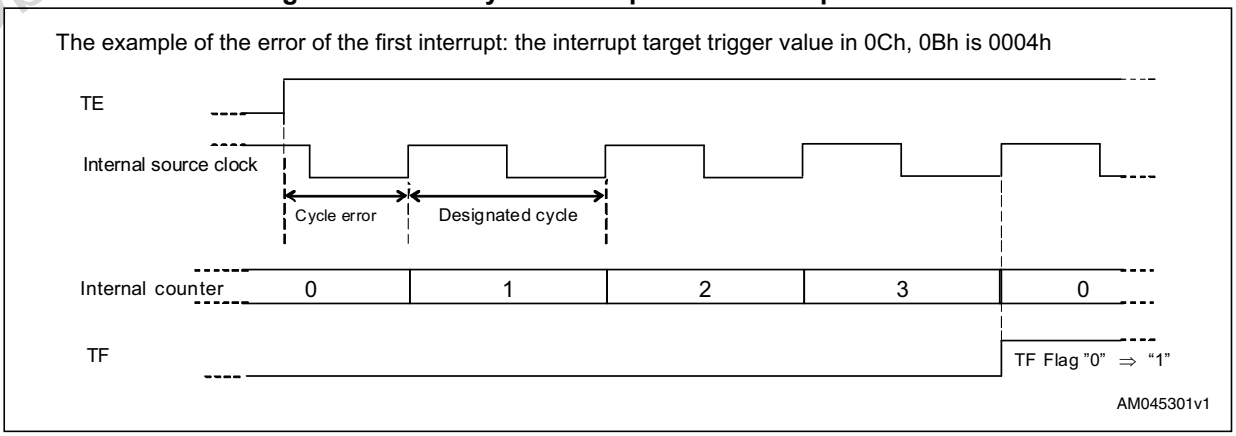
2.6.3 Time error in fixed-cycle timer interrupt

Before configuring the fixed-cycle timer interrupt conditions, for example, setting the values in register 0Bh and 0Ch or selecting the source clock, it is recommended to write "0" to both the TE and TIE bits to prevent hardware interrupts during the configuration period.

When the TE bit is set from 0 to 1, the first interrupt may not be generated correctly. The maximum time error could be as much as the source clock period as illustrated below in *Figure 10*.

In a similar way, if the user sets the RESET bit to 1, the fraction of the internal clock chain below 4 kHz will be cleared. This can also result in an error in the first interrupt once the RESET bit is cleared. This timing error does not affect the 4 kHz clock source fixed-cycle interrupt.

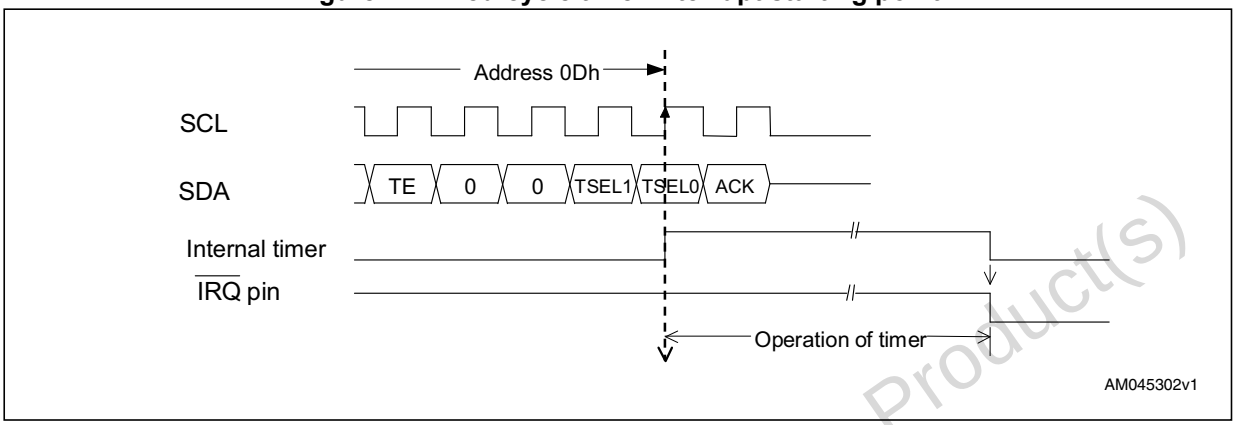
Figure 10. Fixed-cycle interrupt - first interrupt time error



2.6.4 Starting the fixed-cycle timer interrupt

The fixed-cycle timer interrupt internal counter value starts at the rising edge of the SCL signal that occurs when the TE value is changed from "0" to "1" (after the LSB is transferred). Refer to *Figure 11* for a detailed illustration.

Figure 11. Fixed-cycle timer interrupt starting point



2.6.5 Stopping the fixed-cycle timer interrupt

When the RESET bit in control register 0Fh is 1, the clock divider <4 KHz is stopped. As a result, the fixed-cycle timer interrupt with source clocks of 64 Hz, 1 Hz and "minute" update will be stopped. The RESET bit will not affect the fixed-cycle timer interrupt with the source clock of 4,096 Hz.

2.6.6 Example operation of the fixed-cycle timer interrupt

The fixed-cycle timer interrupt example is given in *Figure 12*. The fixed-cycle timer interrupt timing sequence is given in *Figure 13*.

Figure 12. Example of fixed-cycle timer interrupt

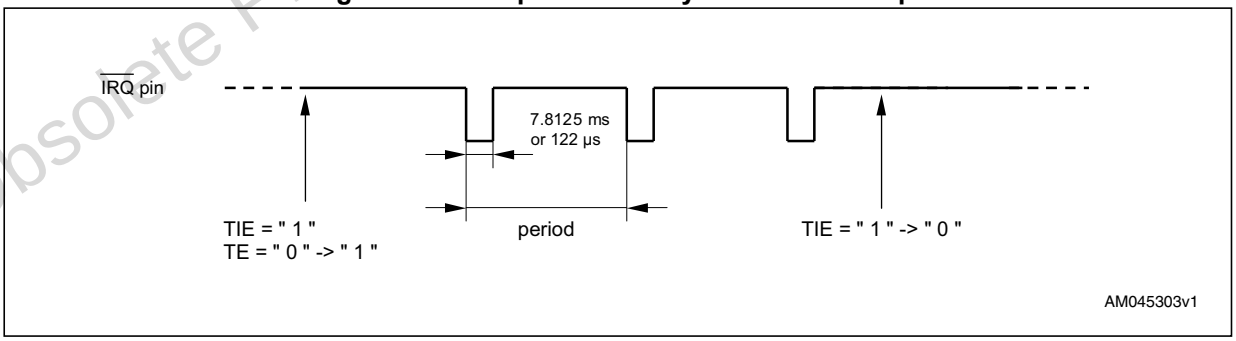
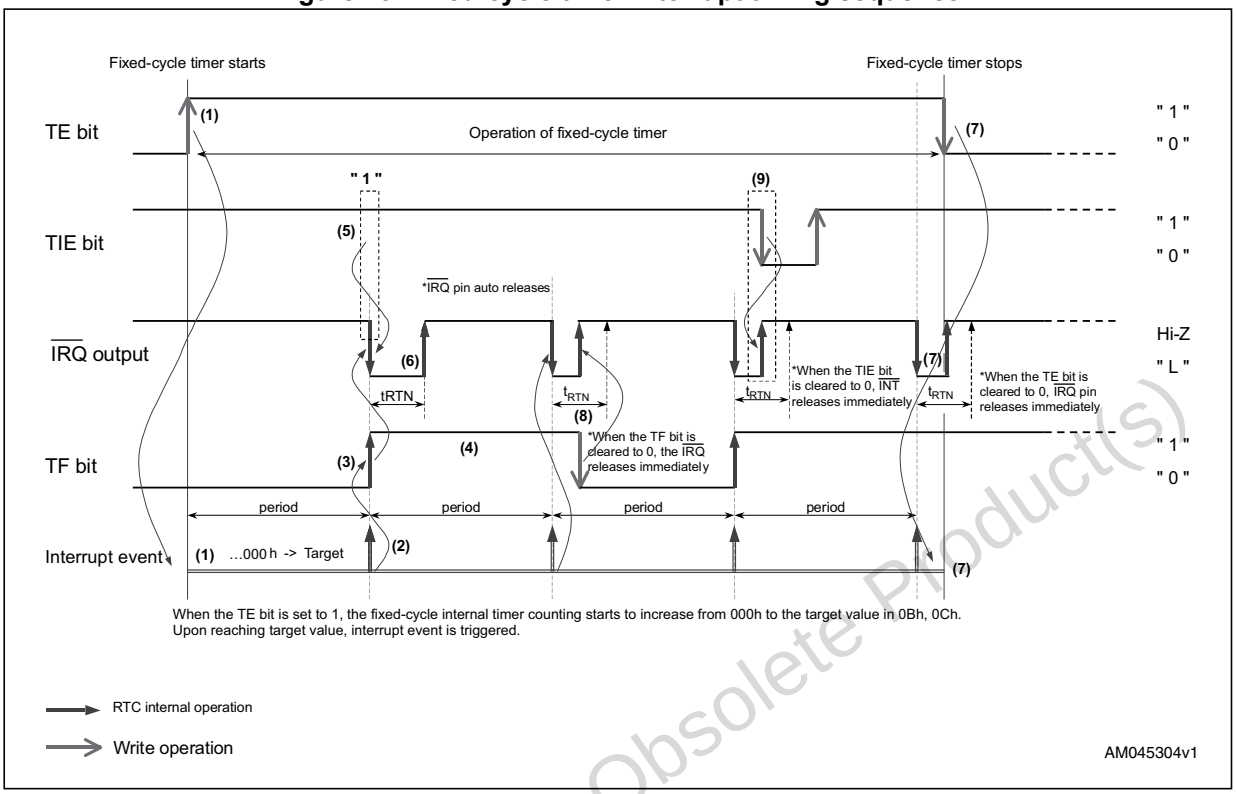


Figure 13. Fixed-cycle timer interrupt timing sequence



1. When the TE bit is set to 1, the fixed-cycle internal timer starts incrementing from 000h towards the target value set in register 0Bh and 0Ch.
2. When the internal timer value reaches the target value, an interrupt event occurs. After the interrupt event, the internal timer automatically counts starting from 000h towards the target value again.
3. When a fixed-cycle timer interrupt event occurs, the TF bit is set to 1.
4. Once the TF bit is set to 1, it remains until it is reset to 0 by the user.
5. If TIE=1 when a fixed-cycle timer interrupt occurs, the $\overline{IRQ}$ pin output is driven low. If TIE=0 when a fixed-cycle timer interrupt event occurs, the $\overline{IRQ}$ pin output remains Hi-Z.
6. Output from the $\overline{IRQ}$ pin remains low during the t_{RTN} period following each event, after which it is automatically released to Hi-Z. The $\overline{IRQ}$ pin is again driven low when the next interrupt occurs.
7. When the TE bit is reset to 0, the fixed-cycle timer function is stopped and the $\overline{IRQ}$ pin is released to Hi-Z immediately.
8. If the $\overline{IRQ}$ pin is low, the $\overline{IRQ}$ pin status is released to Hi-Z immediately when the TF bit value changes from 1 to 0.
9. If the $\overline{IRQ}$ pin is low, the $\overline{IRQ}$ pin status is released to Hi-Z immediately when the TIE bit value changes from 1 to 0.

2.7 Time update interrupt function

The time update interrupt function generates periodic interrupts at one-second or one-minute intervals according to the timing of the internal clock.

When a time update is generated, the $\overline{IRQ}$ pin will be pulled low if enabled (bit UIE=1) and the flag bit (UF) will be set to 1 to indicate the time update occurrence. After the $\overline{IRQ}$ pin is pulled low, it will be automatically released (change to Hi-Z) after time t_{RTN} so that periodic interrupts can be generated even if the user does not clear the flag bit.

The time update interrupt function related registers are given in *Table 17*.

Table 17. Time update interrupt related register bits

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	Extension register	TEST	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0Eh	Flag register	0	0	**UF**	TF	AF	0	VLF	VDET
0Fh	Control register	CSEL1	CSEL0	**UIE**	TIE	AIE	0	0	**RESET**

Note: All the timer update interrupt function related register bits are marked in bold.

2.7.1 Related registers

The USEL bit in register 0Dh is for the selection of either one-second or one-minute update generating the interrupts. If USEL=0 (default value), one-second update interrupt is selected. If USEL=1, one-minute update interrupt is selected.

The UF bit in register 0Eh is the time update interrupt flag. Once the time gets updated (one-second or one-minute selected by USEL bit), the UF bit is set to 1 to indicate a time update occurrence. Once UF=1, it will not be auto-cleared and relies on the user to reset it to 0. Resetting the UF bit to 0 will release the $\overline{IRQ}$ pin from low to Hi-Z immediately, otherwise the $\overline{IRQ}$ pin is auto-released after t_{RTN} time specified in *Table 18*.

The UIE bit in register 0Fh is the interrupt enable bit. If the interrupt is enabled (UIE=1) and there is a time update event, the $\overline{IRQ}$ pin will be pulled low. If the interrupt is disabled (UIE=0), even when there is a time update event, the $\overline{IRQ}$ pin will remain Hi-Z. The UF bit still can be set to 1 regardless of the status of the $\overline{IRQ}$ pin. Resetting the UIE bit to 0 while $\overline{IRQ}$ is low will immediately release the $\overline{IRQ}$ pin (change to Hi-Z).

Table 18. Time update interrupt cycle selection

USEL	Time update interrupt cycle	Auto reset time (t_{RTN})	Effect of RESET bit
0	One-second update (once per second)	500 ms	Does not operate when RESET = 1
1	One-minute update (once per minute)	7.8125 ms	

Note: 1 The $\overline{IRQ}$ pin auto-release time (t_{RTN}) varies according to the selection of the interrupt.

2 When the source clock has been set to "second update" or "minute update", the timing of both counting and interrupts is coordinated with the clock update timing.

3 Since RESET=1 will stop the clock chain below 4,096 Hz, both the one-second update and one-minute update will be stopped.

2.7.2 Starting the time update interrupt

Once the M41TC8025 is powered on, the time update interrupt is turned on. According to the selection of the USEL bit (one-second or one-minute update), the UF bit will be set once there is a time update. The $\overline{IRQ}$ pin will be pulled low if it is enabled (bit UIE=1).

2.7.3 Stopping the time update interrupt

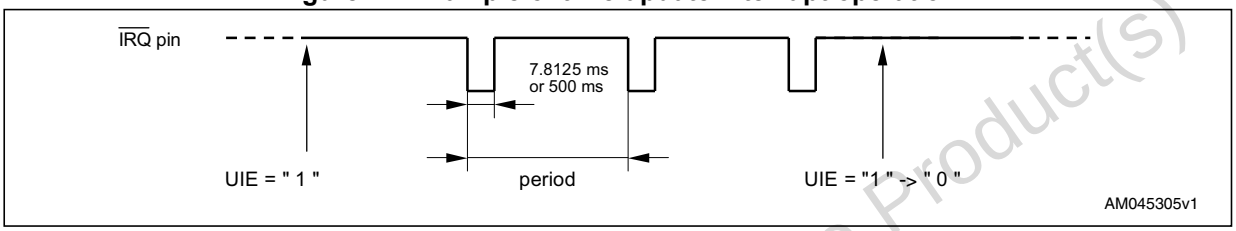
Although the time update interrupt function cannot be fully stopped, if UIE=0, the time update interrupt can be prevented.

Since RESET=1 will stop the clock divider below 4,096 Hz, both the one-second update and one-minute update interrupts will be stopped.

2.7.4 Example operation of the time update interrupt

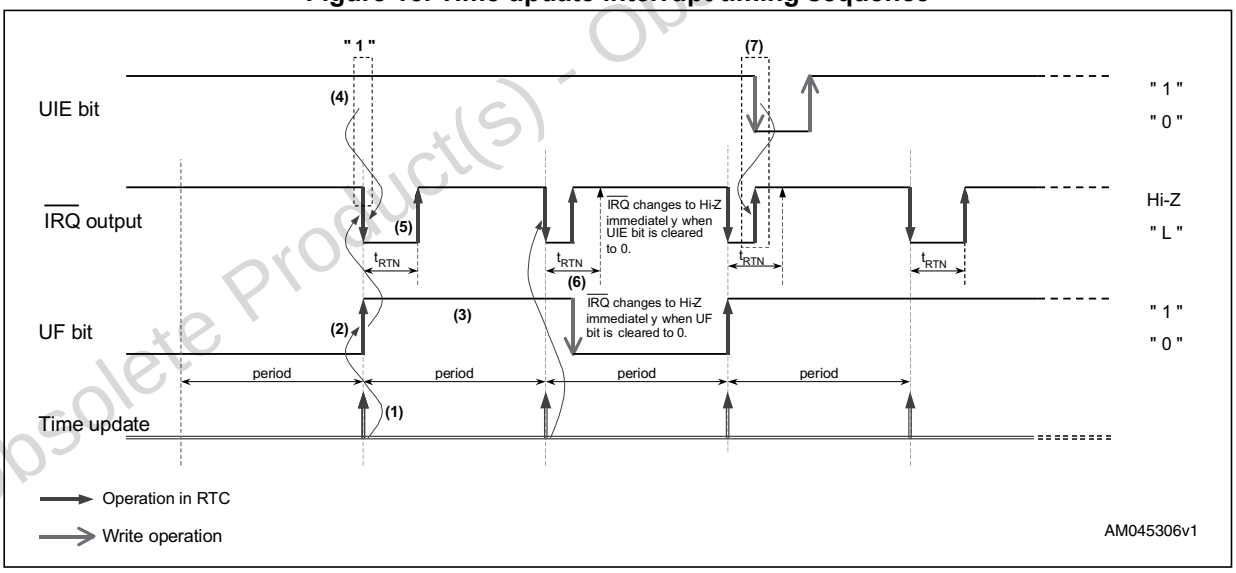
The time update interrupt example is given in *Figure 14*. The time update interrupt timing sequence is given in *Figure 15*.

Figure 14. Example of time update interrupt operation



Note: One-second update auto release time is 500 ms while one-minute auto release time is 7.8125 ms.

Figure 15. Time update interrupt timing sequence



1. The time update event occurs when the internal clock's value matches either the second update or the minute update (selected by USEL bit).
2. When the time update occurs, the UF bit is set to 1.
3. Once UF=1, it remains until the user clears it to 0.
4. When the time update interrupt occurs, the $\overline{IRQ}$ pin output is driven low if UIE=1. If UIE=0 when a time update occurs, the $\overline{IRQ}$ pin remains Hi-Z.
5. Each time an interrupt occurs, the $\overline{IRQ}$ pin output is driven low only up to time t_{RTN} (fixed as 500 ms for the second update and 7. 8125 ms for the minute update) after which it is automatically released to Hi-Z. The $\overline{IRQ}$ pin output is driven low again when the next interrupt event occurs.
6. When the $\overline{IRQ}$ pin is low, it will be released to Hi-Z immediately when the UF bit is reset to 0.
7. When the $\overline{IRQ}$ pin is low, it will be released to Hi-Z immediately when the UIE bit is set to 0.

2.8 Alarm interrupt function

The alarm interrupt function generates an alarm at the condition set in the alarm registers in 08h to 0Ah. Once the current clock and calendar match the alarm condition, the alarm function is activated. The flag bit (AF) will be set to 1 to indicate the alarm event and the $\overline{IRQ}$ pin will be pulled low if enabled (bit AIE=1). There is no auto clear of either the $\overline{IRQ}$ pin or the flag bit.

The alarm interrupt function related registers are given in *Table 19*.

Table 19. Alarm interrupt related register bits

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Minutes	**0**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
02h	Hours	**0**	**0**	**20**	**10**	**8**	**4**	**2**	**1**
03h	Day-of-week	**0**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
04h	Date (day of month)	**0**	**0**	**20**	**10**	**8**	**4**	**2**	**1**
08h	Alarm minutes	**AM_M**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
09h	Alarm hours	**AM_H**	x	**20**	**10**	**8**	**4**	**2**	**1**
0Ah	Alarm day	**AM_D**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Alarm date		x	**20**	**10**	**8**	**4**	**2**	**1**
0Dh	Extension register	TEST	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0Eh	Flag register	0	0	UF	TF	**AF**	0	VLF	VDET
0Fh	Control register	CSEL1	CSEL0	UIE	TIE	**AIE**	0	0	**RESET**

Note: All the alarm interrupt function related register bits are marked in bold.

2.8.1 Related registers

Registers from 01h to 04h are the current clock and calendar registers and are described in detail in *Section 2.4: Clock and calendar*.

Registers from 08h to 0Ah are the alarm condition setting for minutes, hours and day/date. The MSB of each register is the alarm masking bit AM_M, AM_H and AM_D. If AM_x=0, the alarm occurs when the alarm register setting matches the corresponding current clock and calendar register values. If AM_x=1, this alarm register value will not be compared with the corresponding clock and calendar value.

Register 0Ah is defined for day-of-week or date (day of month). It can be selected by WADA (Week-alarm/Day-alarm) bit in register 0Dh. If WADA=0, day-of-week is selected. If WADA=1, date (day of month) is selected.

The possible values of the alarm minutes register in 08h are in BCD format of "00", "01", "02" and up to "59".

The possible values of the alarm hours register in 09h are in BCD format of "00", "01", "02" and up to "23".

In the alarm day-of-week register in 0Ah, one bit represents one day from bit 0 to bit 6, which is the same definition as the calendar Day-of-week register 03h. The only difference

is that in register 03h, only one bit should be set since that bit represents one day in a week in the calendar while in register 0Ah, multiple bits can be set to represent the alarm for more than one day in a week.

In the alarm date register in 0Ah, possible values are given in BCD format of "00", "01", "02", and up to "31".

The AF bit in register 0Eh is the alarm flag. Once the alarm event occurs, the AF bit is set to 1. Once AF=1, it will not be auto-cleared and relies on the user to reset to 0. Resetting the AF bit to 0 will release the $\overline{IRQ}$ pin from low to Hi-Z immediately.

The AIE bit in register 0Fh is the alarm enable bit. If the alarm is enabled (AIE=1) and there is an alarm event, the $\overline{IRQ}$ pin will be pulled low. If the alarm is disabled (AIE=0), even if there is an alarm event, the $\overline{IRQ}$ pin will remain Hi-Z. Setting the AIE bit to 0 while the $\overline{IRQ}$ pin is low will immediately release the $\overline{IRQ}$ pin from low to Hi-Z.

Since RESET=1 will stop the clock chain below 4,096 Hz, the alarm interrupt will be stopped.

2.8.2 Alarm interrupt example

Table 20 below gives the example of the alarm settings when "Day-of-week" has been selected (WADA=0).

Table 20. Day-of-week alarm settings

	Register 0Ah								Reg. 09h	Reg. 08h	Alarm description
	Day-of-week alarm								Hour alarm	Minute alarm	
	Bit 7 AM_D	Bit 6 S	Bit 5 F	Bit 4 T	Bit 3 W	Bit 2 T	Bit 1 M	Bit 0 S			
Day-of-week is selected (WADA=0)	0	0	1	1	1	1	1	0	08h	80h~FFh	Monday through Friday at 8:00 am
	0	1	0	0	0	0	0	1	80h~FFh	38h	Every Saturday and Sunday at 38 minutes each hour. Hour value is not compared.
	0	1	1	1	1	1	1	1	18h	18h	Every day at 6:18 pm
	1	x	x	x	x	x	x	x			
	1	x	x	x	x	x	x	x	80h~FFh	80h~FFh	Alarm at every minute

Note: 1 x means don't care.

2 If all the AM_M, AM_H and AM_D bits in register 08h, 09h and 0Ah are set to 1, that means all the day-of-week, hours and minutes registers do not compare and the alarm will be generated every minute.

Table 21 gives the example of the alarm settings when "Date (day of month)" has been specified (WADA=1).

Table 21. Date alarm settings

	Register 0Ah								Reg. 09h	Reg. 08h	Alarm description
	Date (day-of-month) alarm								Hour	Minute	
	Bit 7 AM_D	Bit 6 0	Bit 5 20	Bit 4 10	Bit 3 08	Bit 2 04	Bit 1 02	Bit 0 S01			
Date (day-of-month) is selected (WADA=1)	0	0	0	0	1	0	0	0	18h	80h~ FFh	The 8th of each month at 6:00 pm, the minute value is not compared
	0	0	0	1	1	0	0	0	80h~ FFh	28h	The 18th of each month at 28 minutes each hour, the hour value is not compared
	1	x	x	x	x	x	x	x	18h	18h	Every day at 6:18 pm
	1	x	x	x	x	x	x	x	80h~ FFh	80h~ FFh	Alarm at every minute

Note: 1 x means don't care.

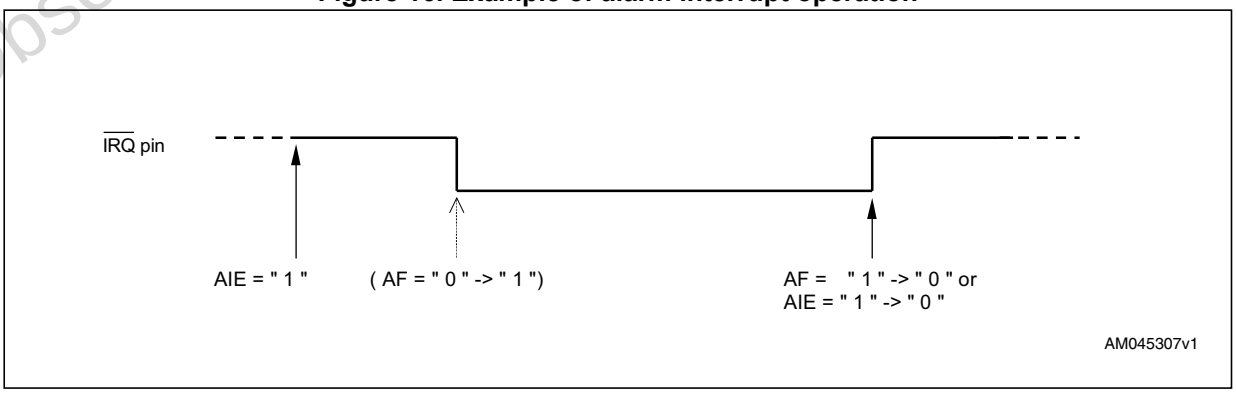
2 If all the AM_M, AM_H and AM_D bits in register 08h, 09h and 0Ah are set to 1, that means all the day-of-month, hours and minutes registers do not compare and the alarm will be generated every minute.

The alarm event only happens when the current clock and calendar counts match the alarm condition. Even if the current date/time is set as the alarm condition, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur the next time, not immediately).

2.8.3 Example operation of the alarm interrupt

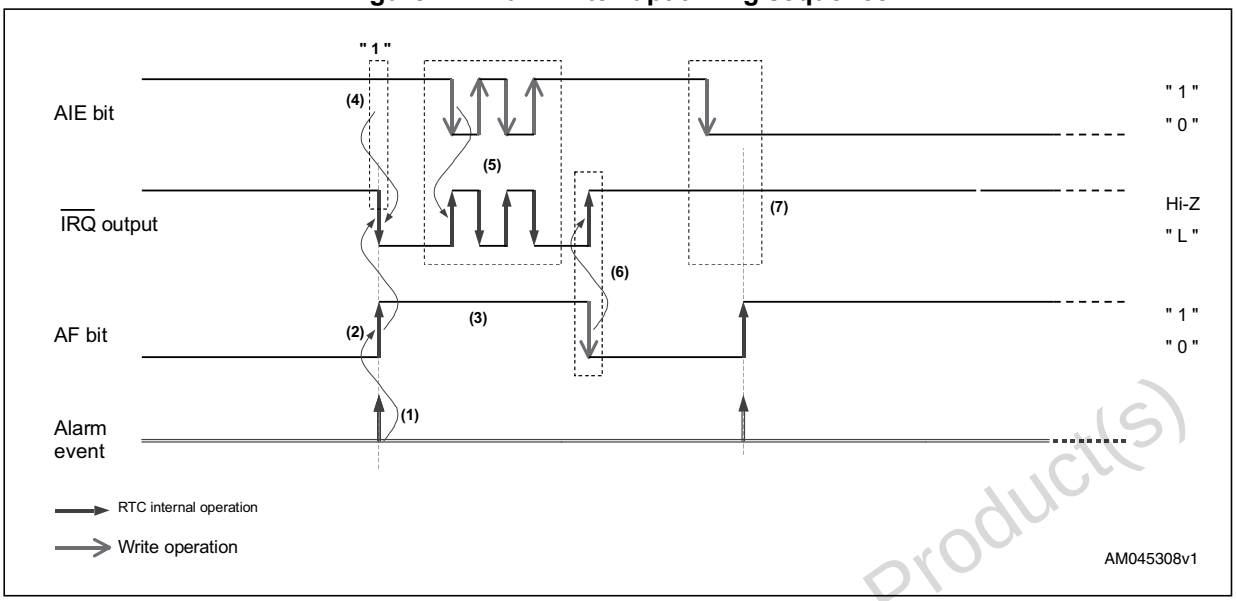
The alarm interrupt example is given in *Figure 16*. The alarm interrupt timing sequence is given in *Figure 17*.

Figure 16. Example of alarm interrupt operation



Note: There is no auto-clear of the IRQ pin.

Figure 17. Alarm interrupt timing sequence



1. The alarm condition of alarm hours, minutes, date or day is set in advance along with the WADA bit. The alarm event only happens when the current clock and calendar counts to match the alarm condition. Even if the current date/time is set as the alarm condition, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur the next time, not immediately).
2. When an alarm event occurs, the AF bit is set to 1.
3. When the AF=1, it remains until it is reset to 0 by the user.
4. If AIE=1 when an alarm event occurs, the $\overline{IRQ}$ pin output is driven low and the status is then held until it is released to Hi-Z by the AF bit reset to 0 or the AIE bit set to 0.
5. If the AIE is set to 0 while the $\overline{IRQ}$ pin is low, the $\overline{IRQ}$ pin is released to Hi-Z immediately.
6. If the AF bit is reset to 0 while the $\overline{IRQ}$ pin is low, the $\overline{IRQ}$ pin is released to Hi-Z immediately.
7. If AIE=0 when an alarm event occurs, the $\overline{IRQ}$ pin status remains Hi-Z.

2.9 Relationship between the three interrupts

The $\overline{IRQ}$ pin is a shared output pin for the above three types of interrupts. It outputs the logic OR'ed result of these interrupts.

When an interrupt has occurred and the $\overline{IRQ}$ pin is pulled low, the status of the UF, TF and AF flags will indicate which interrupt(s) has(have) occurred.

If the user sets RESET to 1 when $\overline{IRQ}$ is low, the $\overline{IRQ}$ pin releases to Hi-Z immediately.

2.10 Low-voltage detection

The M41TC8025 has two register bits in 0Eh to indicate the voltage low levels as highlighted in *Table 22*.

Table 22. Battery voltage low related register bits

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OEh	Flag register	0	0	UF	TF	AF	0	**VLF**	**VDET**

The VLF (Voltage Low Flag) bit indicates a low voltage occurrence. At initial power-up, the VLF bit is set to 1 and the user needs to reset it to 0 in the startup routine. The VLF bit is automatically set and can only be reset to 0 by the user.

During operation, if VLF=1, all the register data is not guaranteed to be correct and the RTC needs initialization.

The VDET (Voltage Detection Flag) bit indicates the status of temperature compensation. At initial power-up, the VDET bit is set to 1 and the user needs to reset it to 0 in the startup routine.

During operation, if VDET=1, although the timekeeping is still functional, the temperature compensation stops and the timing accuracy is not guaranteed. The VDET bit is automatically set and can only be reset to 0 by the user.

VLF and VDET detection occurs during the temperature compensation period (*Section 2.4.4: Temperature compensation on page 17*). The worst case delay is 30 seconds for these bits to be set to 1 (longest temperature compensation period).

2.11 Application

2.11.1 Battery backup and recovery

Figure 18 gives an example of the battery backup for the M41TC8025. The diode in the battery block is only required when using a lithium battery. The battery backup sequence and AC characteristics are given in *Figure 19* and *Table 23*.

Figure 18. Battery backup connection

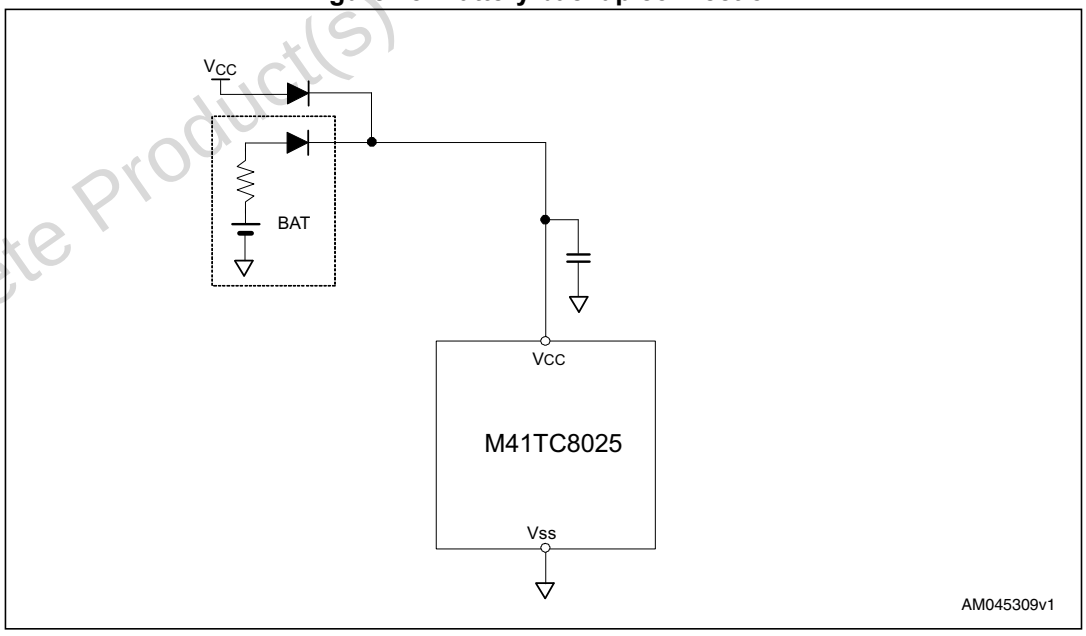


Figure 19. Battery backup sequence

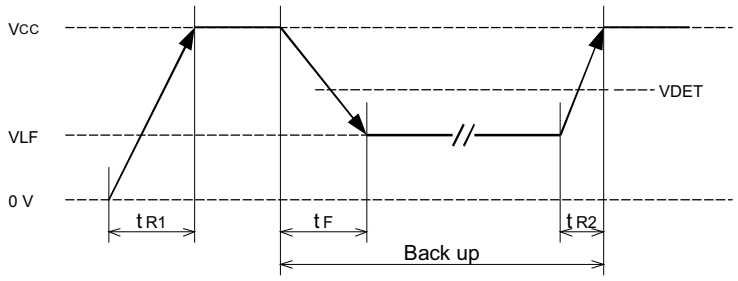


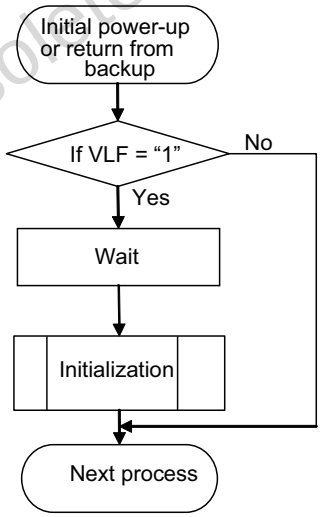
Table 23. Battery backup time AC characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply detection voltage 1	V_{DET}	-			2.2	V
Power supply detection voltage 2	V_{LF}	-			1.6	V
Power supply drop time	t_F	-	2			µs/V
Initial power-up time	t_{R1}	-			10	ms/V
Clock maintenance power-up time	t_{R2}	1.6 V to $V_{CC} \leq 3.6$ V	5			µs/V
		1.6 V to $V_{CC} \geq 3.6$ V	15			µs/V

2.11.2 Application flowcharts

The flowcharts in *Figure 20* and *Figure 21* give the user an example of the initial power-up routine and the initialization procedure of the M41TC8025. The user can modify them based on the real application.

Figure 20. Initial power-up routine



After initial power-up or return from the battery backup, VLF should be checked first.

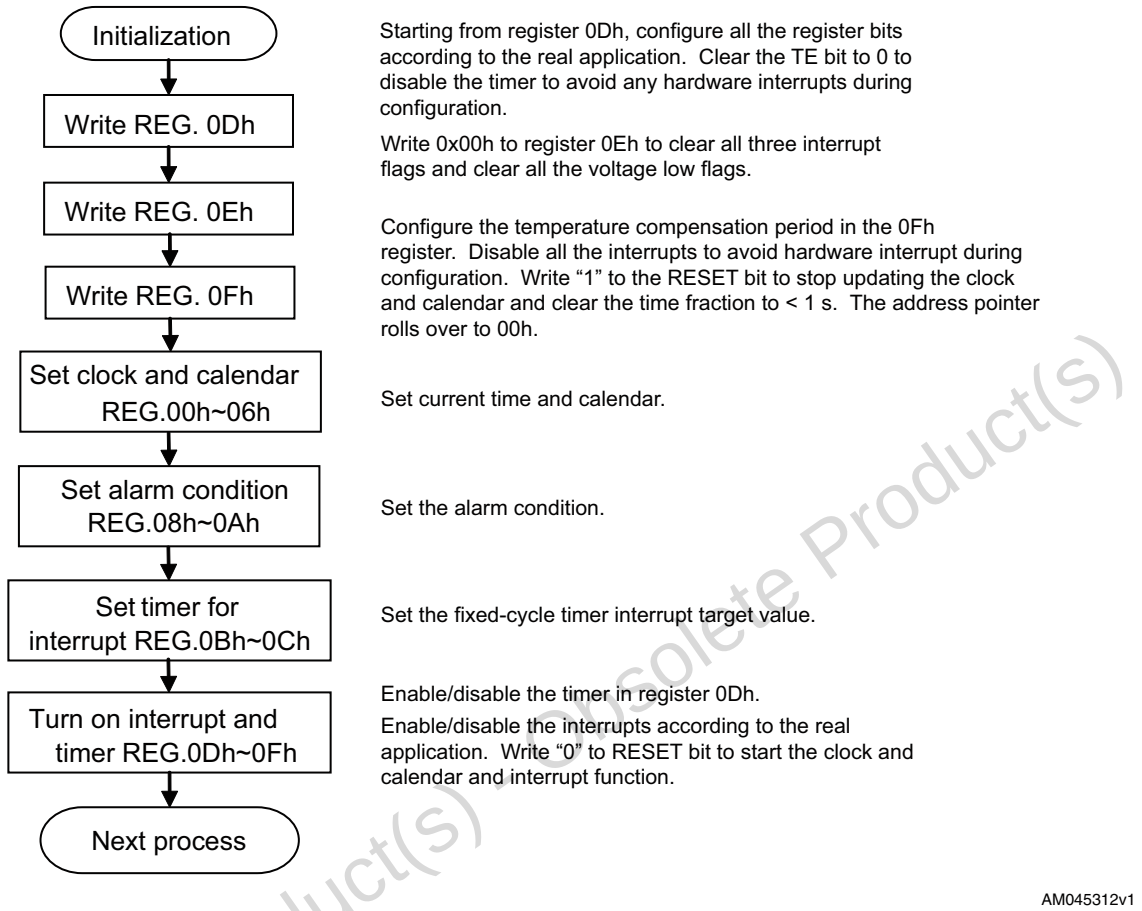
At initial power-up, VLF is set to “1” by default.

If M41TC8025 is returned to Vcc from battery backup and VLF = 1, an abnormal event occurred during the backup and all the register data is not guaranteed. The user needs to initialize the RTC as in the flowchart shown in Figure 21.

The wait time is to ensure that the oscillator is stable.
The typical oscillator startup time is 1 s at 25°C and 3 V supply voltage.

AM045311v1

Figure 21. Initial power-up routine



It is recommended that the user simply include all the initialization process in one I^2C command, ensuring that all the commands from the START condition to the STOP condition are kept within 0.95 s to avoid triggering timeout function. With a single command, the user doesn't need to write "0" to the RESET bit since the STOP condition will automatically set RESET to 0.

3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 24. Absolute maximum ratings

Symbol	Parameter	Value(1)	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	-55 to +125	°C
V_{CC}	Supply voltage	-0.3 to 7.0	V
T_{SLD}(2)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input voltage on FOE pin	-0.3 to V_{CC} +0.3	V
	Input voltage on SCL and SDA pins	-0.3 to 7.0	
	Output voltage on FOUT pin	-0.3 to V_{CC} +0.3	
	Output voltage on SDA and $\overline{IRQ}$ pins	-0.3 to 7.0	
θ_{JA}	Thermal resistance (junction to ambient)	75	°C/W

1. Data based on characterization results, not tested in production.
2. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

4 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 25: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 25. Operating and AC measurement conditions

Parameter	Value	Unit
Clock operating and timekeeping V_{CC} supply voltage	1.6 to 5.5	V
I^2C interface operating V_{CC} supply voltage	1.8 to 5.5	V
Temperature compensation V_{CC} supply voltage	2.2 to 5.5	V
Ambient operating temperature (T_A)	-45 to +85	°C

Table 26. Frequency characteristics

Parameter	Condition	Value	Unit
Accuracy	T_A = -40 to +85 °C; V_{CC} = 3.0 V (version A) T_A = -45 to 70 °C; V_{CC} = 3.0 V (version C)	±5.0	ppm
	T_A = 0 to +50 °C; V_{CC} = 3.0 V	±3.8	ppm
Frequency/voltage characteristics	T_A = 25 °C; V_{CC} = 2.2 to 5.5 V	±1.0	ppm/V
Aging	T_A = 25 °C; V_{CC} = 3.0 V, the first year	±3.0	ppm/year
Oscillator startup	T_A = -40 to +85 °C; V_{CC} = 2.2 to 5.5 V	3.0 (max)	s

Table 27. DC and AC characteristics

Parameter	Symbol	Condition[1][2]		Min	Typ	Max	Unit
Operating voltage	V_{CC1}	Clock operating and timekeeping		1.6		5.5	V
	V_{CC2}	I^2C interface operating		1.8		5.5	V
	V_{CC3}	Temperature compensation		2.2		5.5	V
Supply current	I_{CC1}	f_{SCL} = 0 Hz, $\overline{IRQ}$ = V_{CC} FOE = V_{SS}, FOUT = output OFF (Hi-Z) Temperature compensation interval = 2.0 seconds	5 V		1.2	3.4	µA
	I_{CC2}		3 V		0.8	2.8	µA
	I_{CC3}	f_{SCL} = 0 Hz, $\overline{IRQ}$ = V_{CC} FOE = V_{CC}, FOUT = 32 KHz, C_L = 0 pF Temperature compensation interval = 2.0 seconds	5 V		3.0	7.5	µA
	I_{CC4}		3 V		2.0	5.0	µA
	I_{CC5}	f_{SCL} = 0 Hz, $\overline{IRQ}$ = V_{CC} FOE = V_{CC}, FOUT = 32 KHz, C_L = 30 pF Temperature compensation interval = 2.0 seconds	5 V		8.0	20.0	µA
	I_{CC6}		3 V		5.0	12.0	µA
Temperature compensation time	t_C				0.977		ms
Input voltage logic high	V_{IH}	FOE		0.7*V_{CC}		V_{CC} + 0.3	V
		SCL and SDA		0.7*V_{CC}		5.5	
Input voltage logic low	V_{IL}	FOE, SCL and SDA		V_{SS} – 0.3		0.3*V_{CC}	V
Output voltage logic high	V_{OH1}	FOUT	V_{CC} = 5 V, I_{OH} = -1 mA	4.5		5.0	V
	V_{OH2}		V_{CC} = 3 V, I_{OH} = -1 mA	2.2		3.0	V
	V_{OH3}		V_{CC} = 3 V, I_{OH} = -100 µA	2.9		3.0	V

Table 27. DC and AC characteristics (continued)

Parameter	Symbol	Condition[1][2]		Min	Typ	Max	Unit
Output voltage logic low	V_{OL1}	FOUT	V_{CC} = 5 V, I_{OL} = 1 mA	V_{SS}		V_{SS} + 0.5	V
	V_{OL2}		V_{CC} = 3 V, I_{OL} = 1 mA	V_{SS}		V_{SS} + 0.8	V
	V_{OL3}		V_{CC} = 3 V, I_{OL} = 100 µA	V_{SS}		V_{SS} + 0.1	V
	V_{OL4}	$\overline{IRQ}$	V_{CC} = 5 V, I_{OL} = 1 mA	V_{SS}		V_{SS} + 0.25	V
	V_{OL5}		V_{CC} = 3 V, I_{OL} = 1 mA	V_{SS}		V_{SS} + 0.4	V
	V_{OL6}	SDA	$V_{CC} \geq$ 2 V, I_{OL} = 3 mA	V_{SS}		V_{SS} + 0.4	V
Input leakage current	I_{LI}	SDA, SCL, FOE pin $V_{IN} = V_{CC}$ or V_{SS}				±0.5	µA
Output leakage current	I_{LO}	$\overline{IRQ}$, SDA, FOUT pin $V_{IN} = V_{CC}$ or V_{SS}				±0.5	µA

1. Valid for ambient operating temperature: T_A = -40 to +85 °C or T_A = -45 to +70 °C; V_{CC} = 1.8 V to 5.5 V (except where noted).
2. Typical values are at V_{CC} = 3.0 V and T_A = 25 °C (except where noted).

Figure 22. Temperature compensation

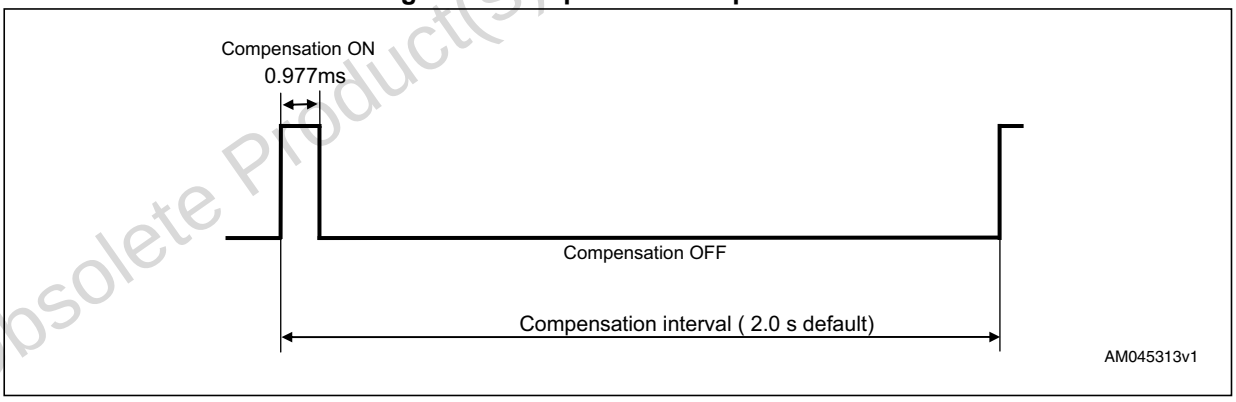
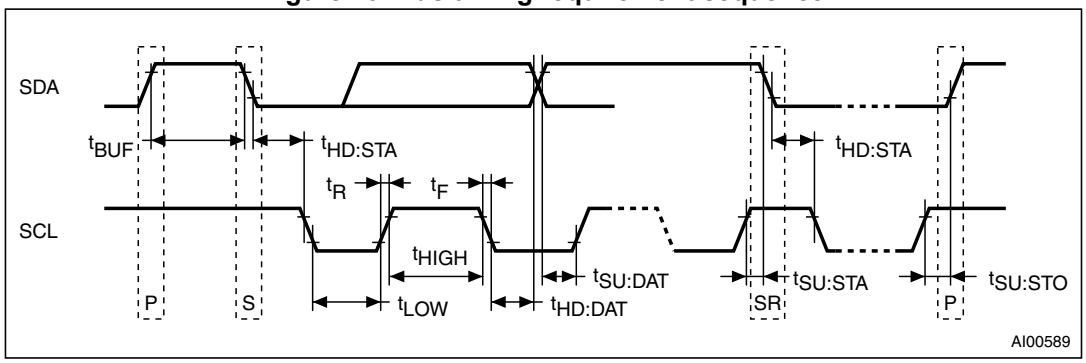


Figure 23. Bus timing requirement sequence



Note: When accessing this device, all communication from transmitting the START condition to transmitting the STOP condition should be completed within 0.95 seconds. If such communication requires 0.95 seconds or longer, the I^2C bus interface is reset by the internal bus timeout function. Refer to the detailed description in Section 2.2.8: I^2C timeout function on page 13.

Table 28. AC characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$(2)	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

1. Valid for ambient operating temperature: T_A = -40 to 85 °C or T_A = -45 to 70 °C; V_{CC} = 1.8 to 5.5 V (except where noted).
2. $t_{SU:DAT}$ = 100 ns (min) for $V_{CC} \geq$ 2.2 V.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 24. SO14 - 14-lead small outline 200-mil package mechanical drawing

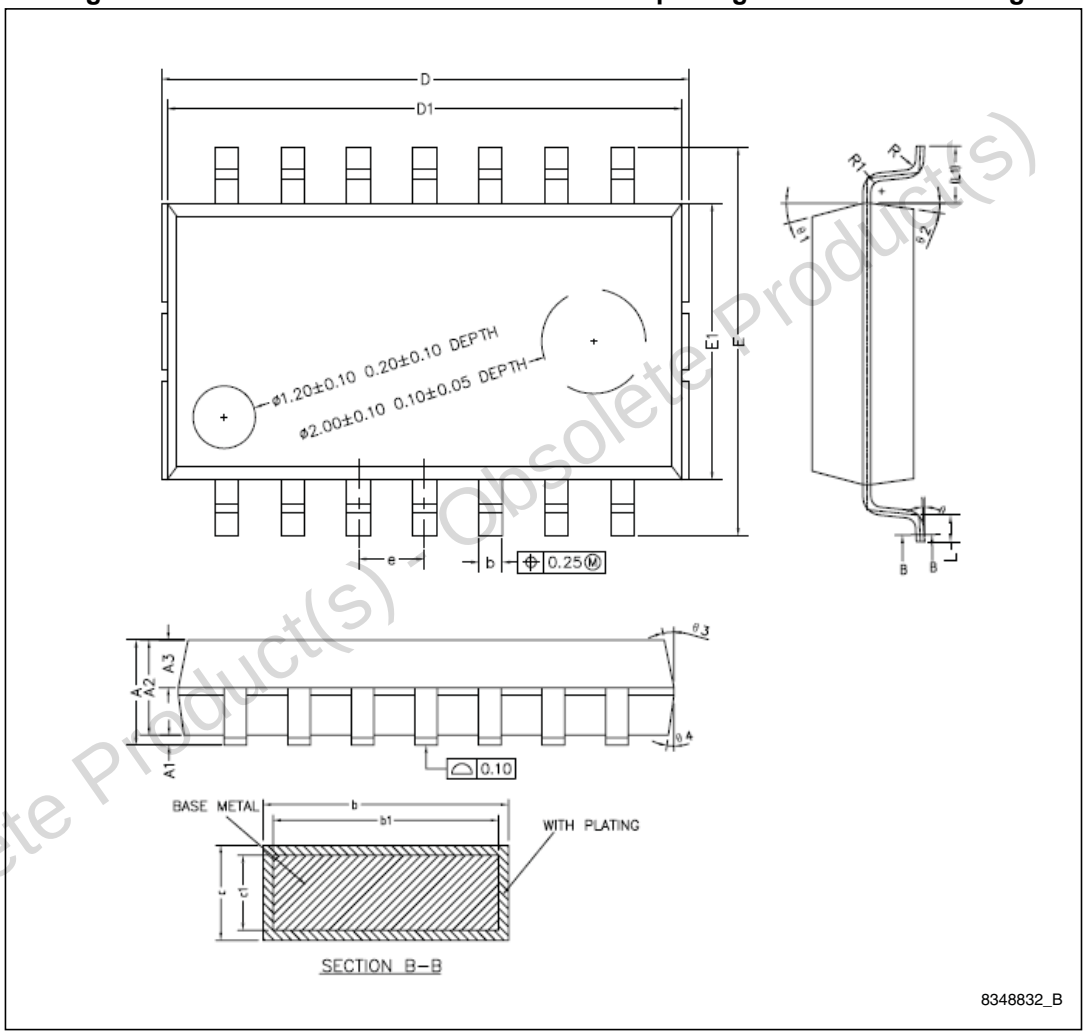


Table 29. SO14 - 14-lead small outline 200-mil package mechanical data

Symbol	mm			in		
	Min	Typ	Max	Min	Typ	Max
A	-	-	2.25	-	-	0.089
A1	0.15	0.20	0.25	0.006	0.008	0.010
A2	1.80	1.90	2.00	0.071	0.075	0.079
A3	0.85	0.95	1.05	0.033	0.037	0.041
b	0.41	-	0.54	0.016	-	0.021
b1	0.40	0.45	0.50	0.016	0.018	0.020
c	0.14	-	0.21	0.006	-	0.008
c1	0.13	0.15	0.17	0.005	0.006	0.007
D1	9.80	9.90	10.00	0.386	0.390	0.394
D(1)	10.05	10.15	10.25	0.396	0.400	0.404
E	7.30	7.45	7.60	0.287	0.293	0.299
E1	5.20	5.30	5.40	0.205	0.209	0.213
e	1.27			0.050		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	1.07 ref.			0.042 ref.		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
θ1	0°	-	8°	0°	-	8°
θ2	13°	15°	17°	13°	15°	17°
θ3	6°	8°	10°	6°	8°	10°
θ4	9.5°	11.5°	13.5°	9.5°	11.5°	13.5°
θ5	6°	8°	10°	6°	8°	10°

1. Dimension “D” includes mold flash.

6 Part numbering

Table 30. Ordering information scheme

Example: M41TC 8025 A MC 6 F

Device family

M41TC

Device type

8025

Accuracy

A = ±5.0 ppm (-40 to 85 °C), ±3.8 ppm (0 to 50 °C)

C = ±5.0 ppm (-45 to 70 °C), ±3.8 ppm (0 to 50 °C)(1)

Package

MC = SO14

Temperature range

6 = –40 °C to 85 °C

7 = –45 °C to 70 °C(1)

Shipping method

F = ECOPACK® package, tape & reel

1. Contact local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Revision history

Table 31. Document revision history

Date	Revision	Changes
05-Mar-2012	1	Initial release.
29-Aug-2012	2	Datasheet status promoted to preliminary data; updated *Table 2: Pin description*; textual update in *Section 2.8.1: Related registers*; removed section concerning package marking.
21-Sep-2012	3	Modified title of document; updated *Figure 3: Block diagram*; minor textual updates in *Section 3: Maximum ratings*; updated footnote *2* of *Table 28: AC characteristics*.
20-May-2013	4	Datasheet status promoted to production data Shortened text of certain *Features* Added order code (M41TC8025CMC7F) with corresponding temperature ranges (updated *Description*, *Table 1*, *25*, *26*, and *30*, *Section 2.1.2*, *Section 2.4*, footnote *1* of *Table 27* and footnote *1* of *Table 28*) Textual update of package description (*Figure 24*, *Table 29*)

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