

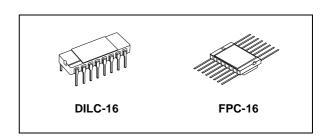
RAD-HARD 3 TO 8 LINE DECODER/LATCH (INVERTING)

- HIGH SPEED:
 - t_{PD} =18ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION: $I_{CC} = 2\mu A \text{ (MAX.)}$ at $T_A = 25^{\circ}\text{C}$
- HIGH NOISE IMMUNITY: V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE: |I_{OH}| = I_{OL} = 4mA (MIN)
- BALANCED PROPAGATION DELAYS: t_{PLH} ≅ t_{PHL}
- WIDE OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 137
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9205-013

DESCRIPTION

The M54HC137 is an high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated with silicon gate $\rm C^2MOS$ technology.

This device is a 3 to 8 line decoder with latches on the three address inputs. When GL goes from low



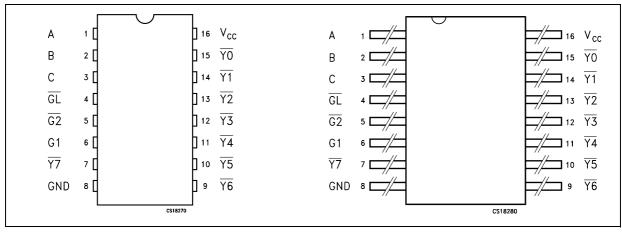
ORDER CODES

PACKAGE	FM	ЕМ
DILC	M54HC137D	M54HC137D1
FPC	M54HC137K	M54HC137K1

to high, the addresses present at the select inputs (A, B, and C) is stored in the latches. As long as GL remains high no address changes will be recognized. Output enable pins G1 and G2, control the state of the outputs independently of the select or latch-enable inputs. All the outputs are high unless G1 is high and G2 is low. The 54HC137 is ideally suited for the implementation of glitch-free decoders in stored-address application in bus oriented systems.

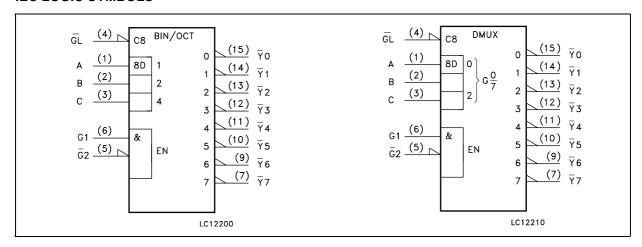
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

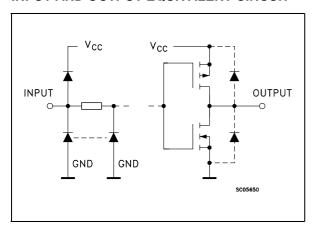


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IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



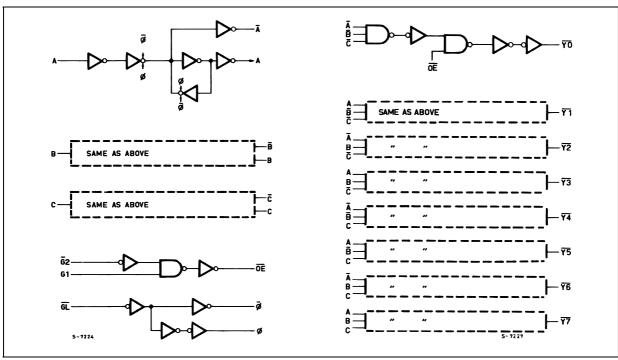
PIN DESCRIPTION

PIN N°	SYMBOL	NAME AND FUNCTION
1, 2, 3	A to C	Data Inputs
4	GL	Latch Enable Input (Active LOW)
5	G2	Data Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
9, 10, 11, 12, 13, 14, 15, 7	Y0 to Y7	Multiplexer Outputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

		INP	UTS			OUTPUTS							
ı	ENABLE			SELECT	-								
GL	G1	G2	С	В	Α	Y0	<u>Y1</u>	Y2	<u>Y3</u>	<u>Y4</u>	Y5	<u>Y6</u>	<u>Y7</u>
Х	Х	Н	X	X	Х	Н	Н	Н	Н	Н	Н	Н	Н
Х	L	Х	X	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
L	Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
L	Н	Ĺ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
Н	Н	L	Х	Х	Х	O	utputs co	rrespond	ding to st	ored add	dress L: a	all others	Н

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
VI	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
Vo	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
Io	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	300	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V _{CC}	Supply Voltage		2 to 6	V
VI	Input Voltage		0 to V _{CC}	V
Vo	Output Voltage		0 to V _{CC}	V
T _{op}	Operating Temperature		-55 to 125	°C
	Input Rise and Fall Time	V _{CC} = 2.0V	0 to 1000	ns
t_r , t_f		V _{CC} = 4.5V	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

		1	est Condition	Value							
Symbol	Parameter	v _{cc}		Т	T _A = 25°C		-40 to 85°C		-55 to 125°C		Unit
		(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input	2.0		1.5			1.5		1.5		
	Voltage	4.5		3.15			3.15		3.15		V
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input	2.0				0.5		0.5		0.5	
	Voltage	4.5				1.35		1.35		1.35	V
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		
	Voltage	4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		V
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	
	Voltage	4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	μΑ
I _{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			2		20		40	μΑ

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ns}$)

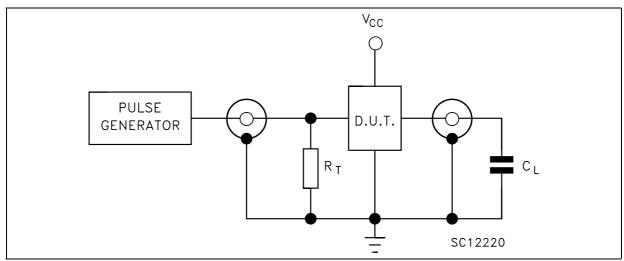
		Т	est Condition	Value							
Symbol	Parameter	v _{cc}		T _A = 25°C			-40 to	85°C	-55 to 125°C		Unit
		(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition	2.0			30	75		95		110	
	Time	4.5			8	15		19		22	ns
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay	2.0			45	115		145		175	
	Time (G1 - Yn)	4.5			14	23		29		35	ns
		6.0			12	20		25		30	
t _{PLH} t _{PHL}	Propagation Delay	2.0			50	115		145		175	
Time (G2 - Yn)	4.5			15	23		29		35	ns	
		6.0			13	20		25		30	
t _{PLH} t _{PHL}	Propagation Delay	2.0			70	170		215		250	
	Time (GL - Yn)	4.5			22	34		43		50	ns
		6.0			19	29		37		43	'
t _{PLH} t _{PHL}	Propagation Delay	2.0			70	165		205		110	
	Time (A, B, C - Y)	4.5			21	33		41		22	ns
		6.0			18	28		35		19	
t _{W(H)}	Minimum Pulse	2.0			12	50		65		75	
t _{W(L)}	Width (GL)	4.5			3	10		13		15	ns
		6.0			3	9		11		13	
t _s	Minimum Set-up_	2.0			8	50		60		75	
	Time (A, B, C - GL)	4.5			2	10		12		15	ns
		6.0			2	9		10		13	
t _h	Minimum Hold	2.0				5		5		5	
••	Time (A, B, C - GL)	4.5				5		5		5	ns
		6.0				5		5		5	

CAPACITIVE CHARACTERISTICS

		7	est Condition	Value							
Symbol	Symbol Parameter		V _{CC}		T _A = 25°C			-40 to 85°C		-55 to 125°C	
		(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
C _{IN}	Input Capacitance	5.0			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			55						pF

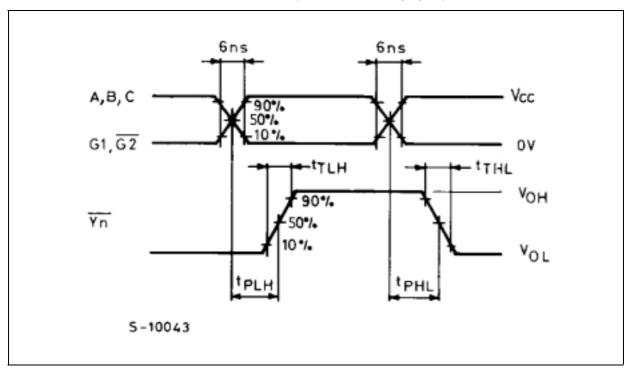
¹⁾ C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} x V_{CC} x f_{IN} + I_{CC}

TEST CIRCUIT

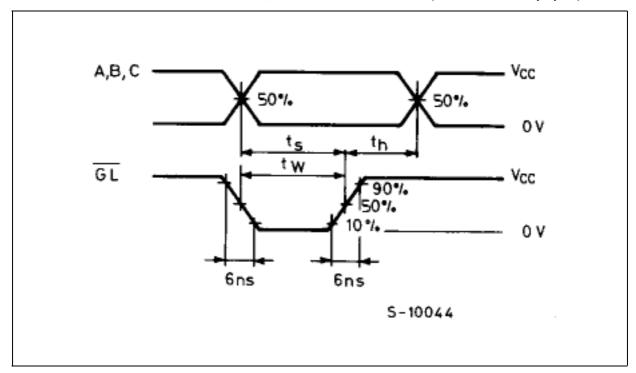


 C_L = 50pF or equivalent (includes jig and probe capacitance) R_T = Z_{OUT} of pulse generator (typically 50 Ω)

WAVEFORM 1: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)

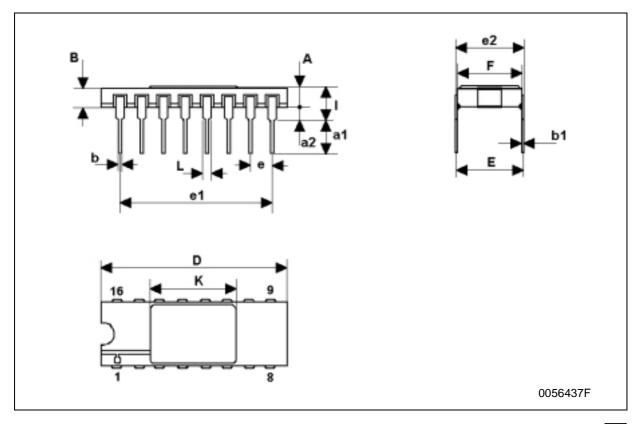


WAVEFORM 2: MINIMUM PULSE WIDTH, SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



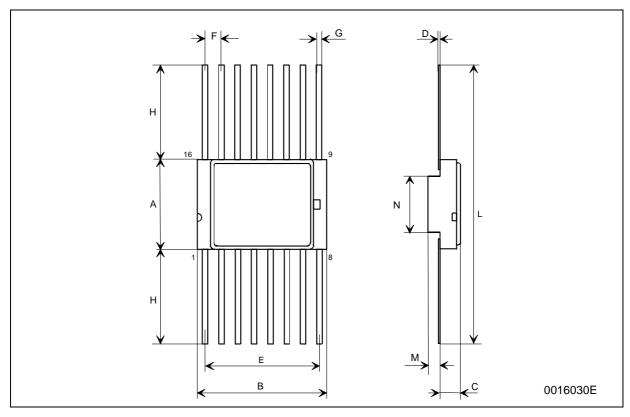
DILC-16 MECHANICAL DATA

DIM		mm.		inch					
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.			
Α	2.1		2.71	0.083		0.107			
a1	3.00		3.70	0.118		0.146			
a2	0.63	0.88	1.14	0.025	0.035	0.045			
В	1.82		2.39	0.072		0.094			
b	0.40	0.45	0.50	0.016	0.018	0.020			
b1	0.20	0.254	0.30	0.008	0.010	0.012			
D	20.06	20.32	20.58	0.790	0.800	0.810			
е	7.36	7.62	7.87	0.290	0.300	0.310			
e1		2.54			0.100				
e2	17.65	17.78	17.90	0.695	0.700	0.705			
еЗ	7.62	7.87	8.12	0.300	0.310	0.320			
F	7.29	7.49	7.70	0.287	0.295	0.303			
I			3.83			0.151			
K	10.90		12.1	0.429		0.476			
L	1.14		1.5	0.045		0.059			



FPC-16 MECHANICAL DATA

DIM		mm.		inch				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.		
А	6.75	6.91	7.06	0.266	0.272	0.278		
В	9.76	9.94	10.14	0.384	0.392	0.399		
С	1.49		1.95	0.059		0.077		
D	0.102	0.127	0.152	0.004	0.005	0.006		
Е	8.76	8.89	9.01	0.345	0.350	0.355		
F		1.27			0.050			
G	0.38	0.43	0.48	0.015	0.017	0.019		
Н	6.0			0.237				
L	18.75		22.0	0.738		0.867		
М	0.33	0.38	0.43	0.013	0.015	0.017		
N		4.31			0.170			



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