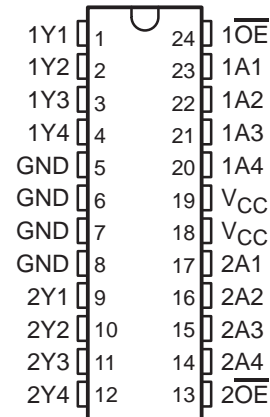


74AC11244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS171B – MARCH 1987 – REVISED SEPTEMBER 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) 1-μm Process
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic DIPs (NT)

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



description

The 74AC11244 is an octal buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as two 4-bit buffers or one 8-bit buffer, with active-low output-enable (\overline{OE}) inputs.

When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The 74AC11244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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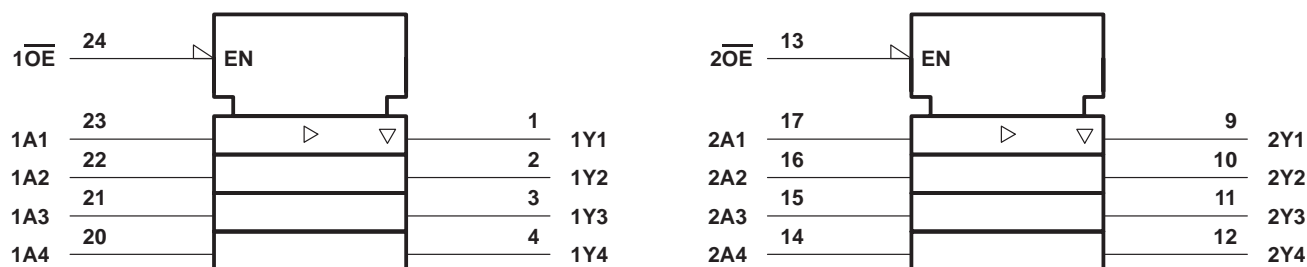
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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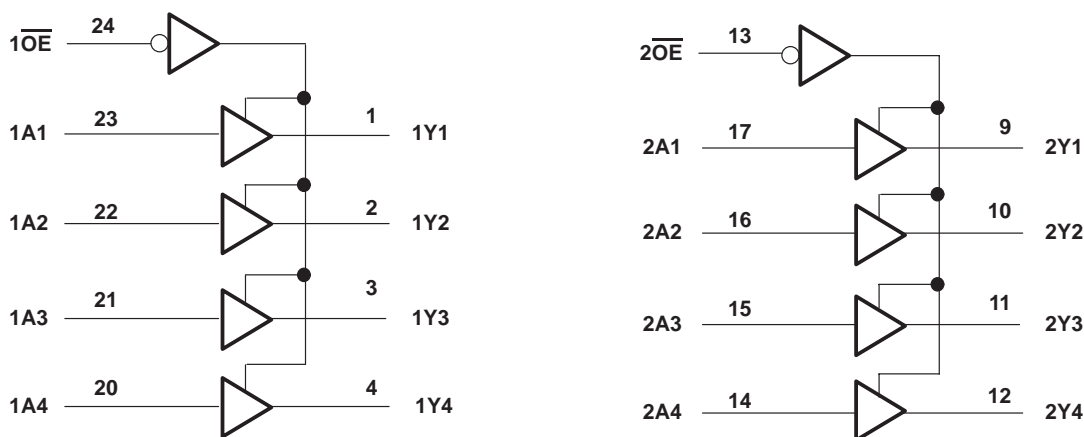
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

74AC11244
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS171B – MARCH 1987 – REVISED SEPTEMBER 1998

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 5.5 V	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V
		V _{CC} = 4.5 V		1.35	
		V _{CC} = 5.5 V		1.65	
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V		–4	mA
		V _{CC} = 4.5 V		–24	
		V _{CC} = 5.5 V		–24	
I _{OL}	Low-level output current	V _{CC} = 3 V		12	mA
		V _{CC} = 4.5 V		24	
		V _{CC} = 5.5 V		24	
Δt/Δv	Input transition rise or fall rate	0		10	ns/V
T _A	Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = –50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
	I _{OL} = –24 mA	5.5 V	4.94			4.8		
	I _{OH} = –75 mA†	5.5 V				3.85		
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.44	
	I _{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I _{OL} = 75 mA†	5.5 V					1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	μA
C _i	V _I = V _{CC} or GND	5 V		4				pF
C _O	V _O = V _{CC} or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.5	7.1	9.3	1.5	10.2	ns
t_{PHL}			1.5	6.3	8.6	1.5	9.5	
t_{PZH}	\overline{OE}	Y	1.5	8	10.7	1.5	11.8	ns
t_{PZL}			1.5	7.9	10.6	1.5	11.9	
t_{PHZ}	\overline{OE}	Y	1.5	5.9	7.9	1.5	8.3	ns
t_{PLZ}			1.5	7.2	9.4	1.5	9.9	

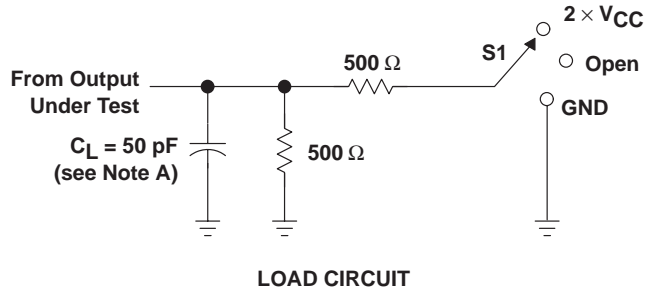
switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.5	4.9	6.7	1.5	7.3	ns
t_{PHL}			1.5	4.5	6.4	1.5	6.9	
t_{PZH}	\overline{OE}	Y	1.5	5.4	7.7	1.5	8.5	ns
t_{PZL}			1.5	5.4	7.6	1.5	8.5	
t_{PHZ}	\overline{OE}	Y	1.5	5.2	7	1.5	7.3	ns
t_{PLZ}			1.5	5.8	7.8	1.5	8.2	

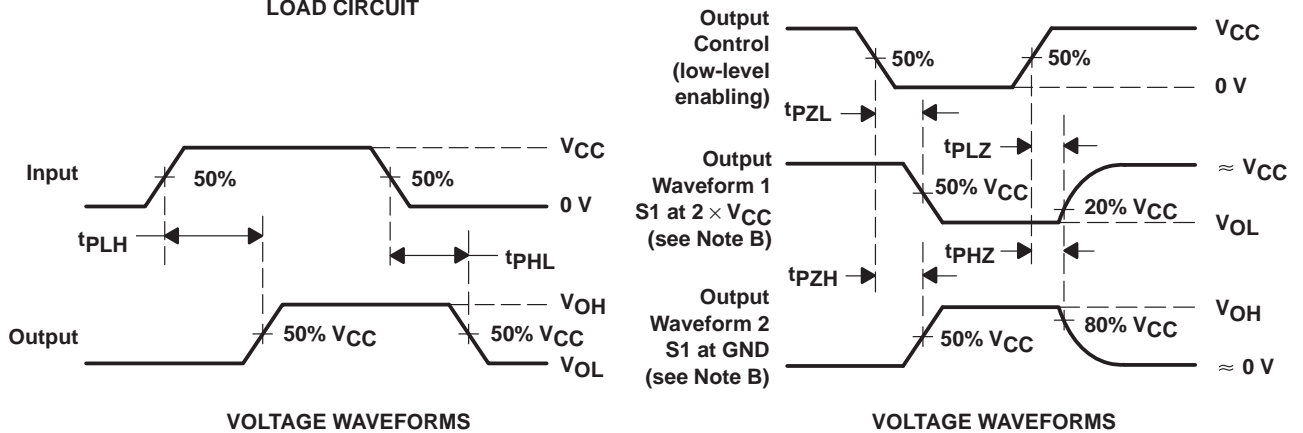
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	27	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AC11244DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
74AC11244DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
74AC11244NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
74AC11244PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244PWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
74AC11244PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC11244PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC11244DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
74AC11244DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
74AC11244PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

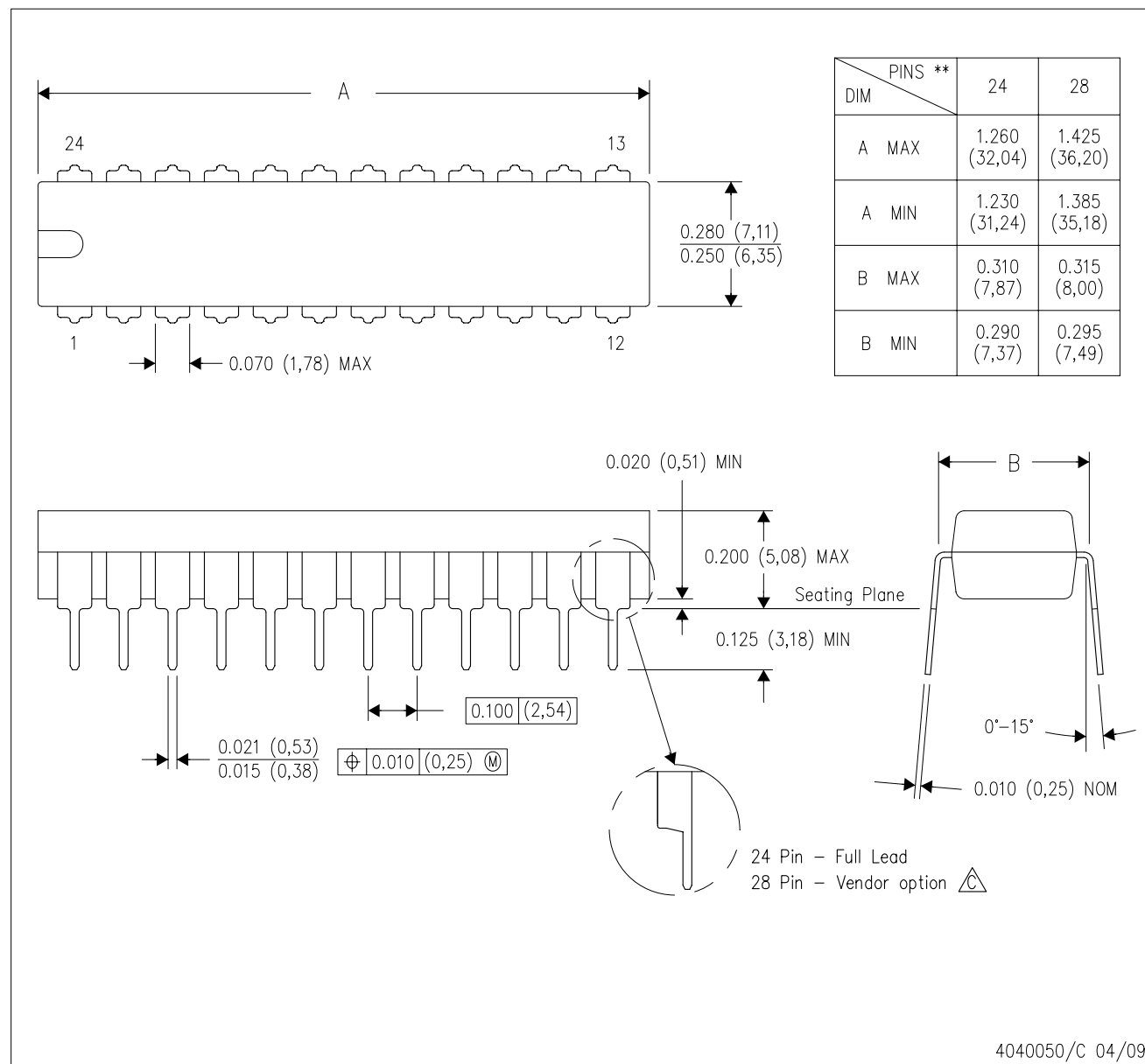
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC11244DBR	SSOP	DB	24	2000	346.0	346.0	33.0
74AC11244DWR	SOIC	DW	24	2000	346.0	346.0	41.0
74AC11244PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

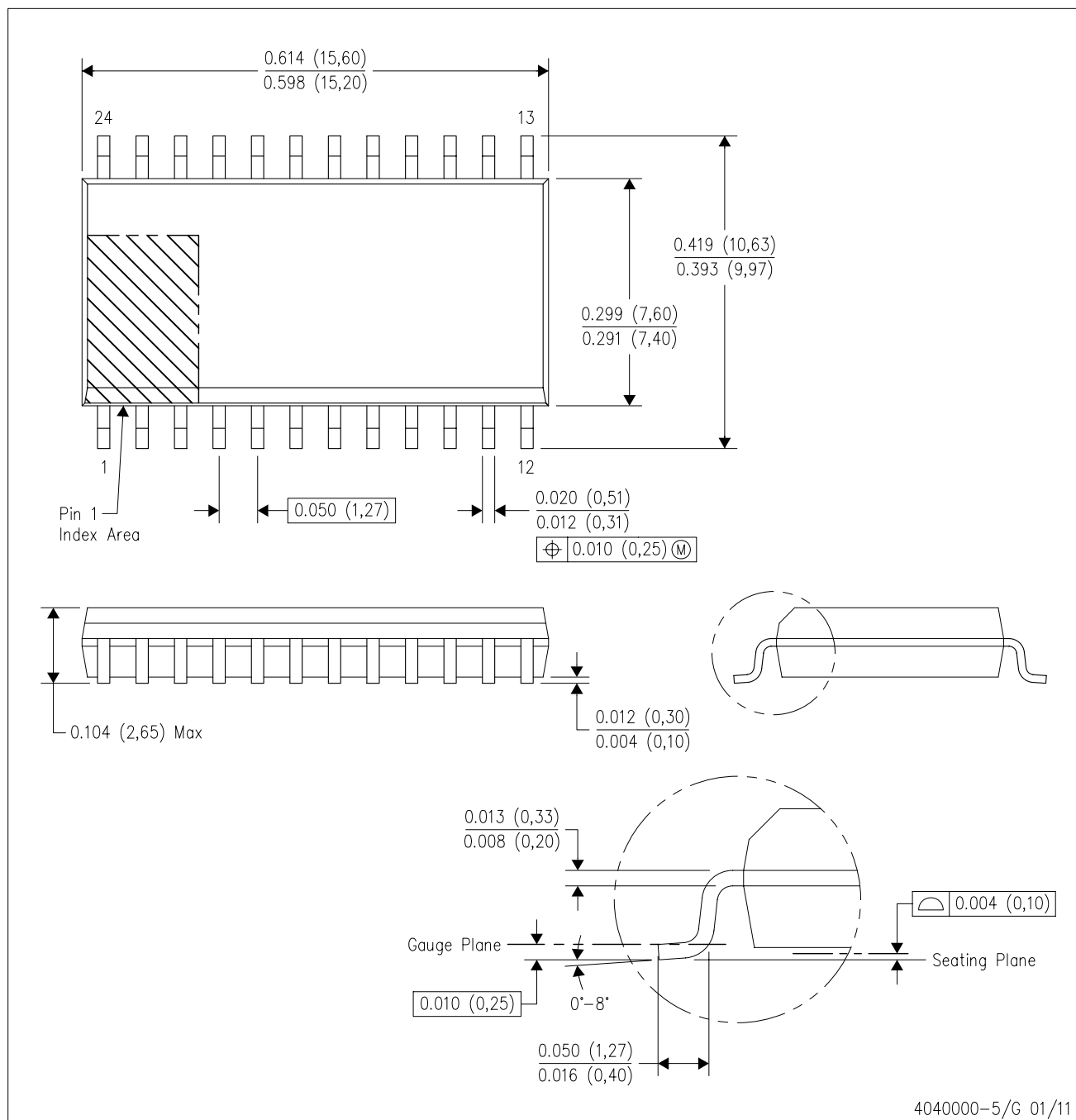
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - $\triangle C$ The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

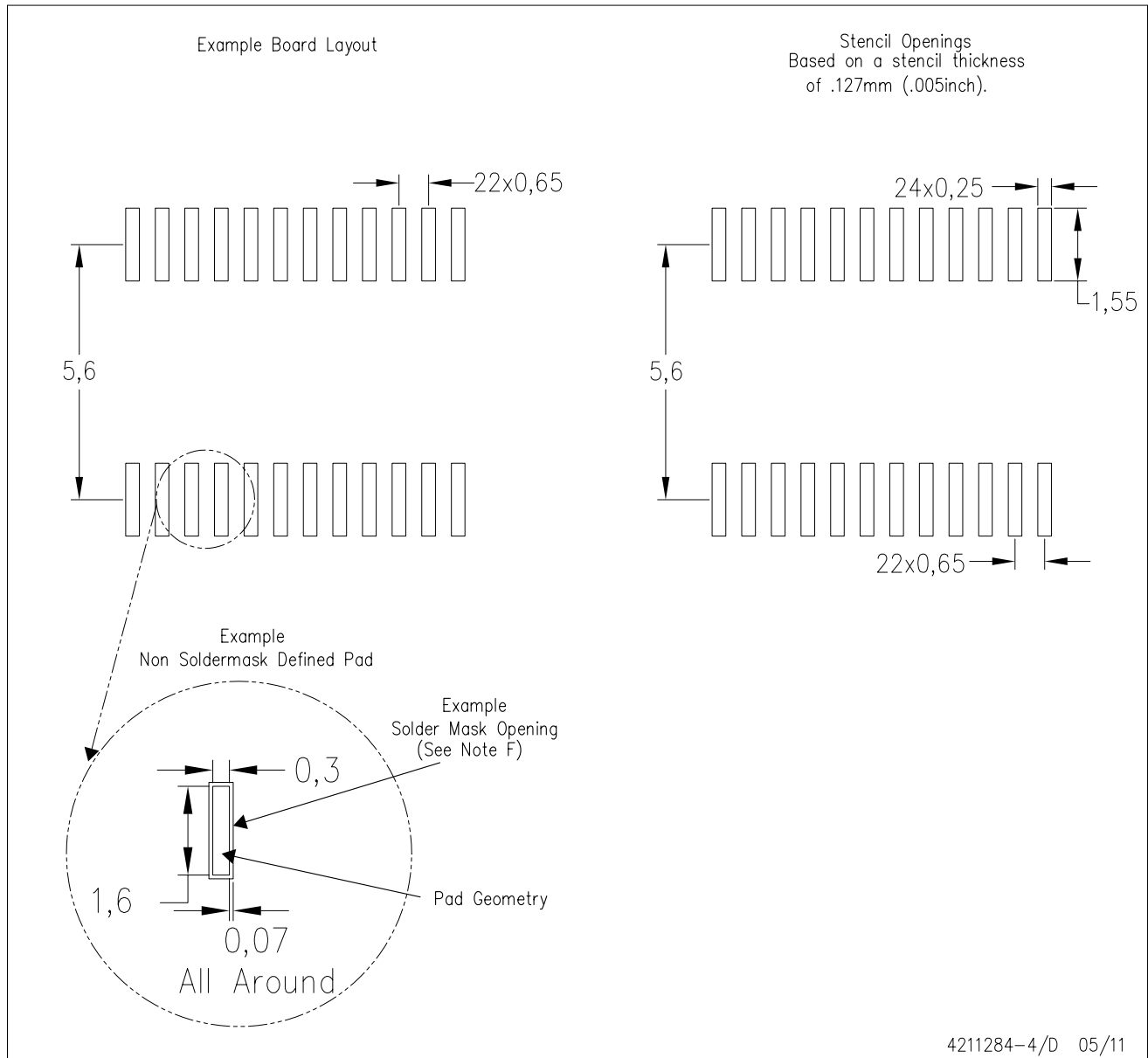
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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