SCAS235A - MARCH 1990 - REVISED APRIL 1996

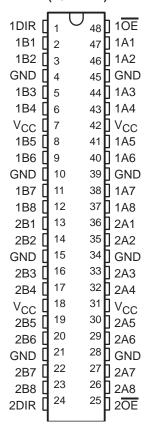
- **Members of the Texas Instruments** Widebus™ Family
- 3-State Outputs Drive Bus Lines or Buffer **Memory Address Registers**
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configuration **Minimizes High-Speed Switching Noise**
- **EPIC** ™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- **Package Options Include Plastic Thin** Shrink Small-Outline (DGG) Package, 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin **Spacings**

description

The 'AC16245 are 16-bit bus transceivers organized as dual-octal noninverting 3-state transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The output-enable input (OE) can be used to disable the devices so that the buses are effectively isolated.

54AC16245...WD PACKAGE 74AC16245 . . . DGG OR DL PACKAGE (TOP VIEW)



The 74AC16245 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	TROL UTS	OPERATION
OE	DIR	
L	L	B data to A bus
L	Н	A data to bus
Н	Χ	Isolation



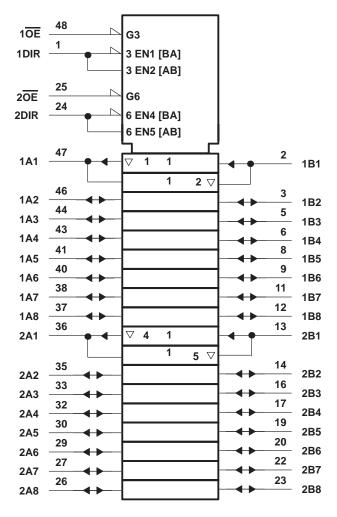
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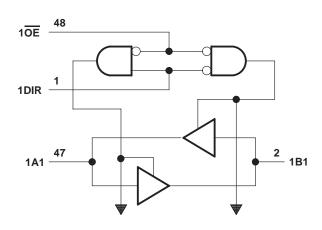
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Transceivers

2DIR 24
2DIR 24
2A1 36
2B1

To Seven Other Transceivers



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±400 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2):	DGG package 0.85 W
	DL package
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			54	AC1624	5	74	AC1624	5	LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 4)		3	5	5.5	3	5	5.5	V
		VCC = 3 V	2.1			2.1			
٧ _{IH}	'IH High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15			3.15			V
		$V_{CC} = 5.5 \text{ V}$	3.85			3.85			
		VCC = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 5.5 V		JE.	1.65			1.65	
٧ _I	Input voltage		0	R	Vcc	0		Vcc	V
٧o	Output voltage		0	5	Vcc	0		Vcc	V
		VCC = 3 V	0		-4			-4	
loh	High-level output current	V _{CC} = 4.5 V	Q		-24			-24	mA
		V _{CC} = 5.5 V			-24			-24	
		VCC = 3 V			12			12	
I _{OL}	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTES: 3. All unused pins (input and I/O) must be held high or low to prevent them from floating.

4. All V_{CC} and GND pins must be connected to the proper voltage power supply.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	T,	Δ = 25°C		54AC	16245	74AC1	6245	LINUT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
Voн	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		V
	I _{OH} = -24 mA	4.5 V	3.94			3.8		3.8		
	IOH = -24 IIIA	5.5 V	4.94			4.8		4.8		
	I _{OH} = -75 mA [†]	5.5 V				3.85	EV	3.85		
		3 V			0.1		0.1		0.1	
	I _{OL} = 50 μA	4.5 V			0.1	4	0.1		0.1	
		5.5 V			0.1	(0)	0.1		0.1	
VOL	I _{OL} = 12 mA	3 V			0.36	Pag	0.44		0.44	V
	I _{OL} = 24 mA	4.5 V			0.36	40	0.44		0.44]
	IOL = 24 IIIA	5.5 V			0.36	,	0.44		0.44	
	I _{OL} = 75 mA [†]	5.5 V					1.65		1.65	
lį	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μΑ
loz	V _I = V _{CC} or GND	5.5 V			±0.5		±5		±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μΑ
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	$V_I = V_{CC}$ or GND	5 V		16						ÞΓ

T Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (see Figure 1)

PARAMETER	FROM	то	T,	ղ = 25°C	;	54AC1	6245	74AC1	16245	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
^t PLH	A or B	B or A	2.5	7.6	10.4	2.5	11.9	2.5	11.9	no
t _{PHL}	AUID	BULA	3.1	9	12.3	3.1	13.5	3.1	13.5	ns
^t PZH	ŌĒ	A or P	2.8	8.6	11.8	2.8	13.2	2.8	13.2	no
t _{PZL}	OE	A or B	3.9	12	16.2	3.9	18	3.9	18	ns
^t PHZ	ŌĒ	A or P	5.3	8.4	10.4	5.3	11.2	5.3	11.2	no
t _{PLZ}	OE .	A or B	4.4	7.7	9.7	4.4	10.3	4.4	10.3	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (see Figure 1)

PARAMETER	FROM	ТО	T,	λ = 25°C	;	54AC1	6245	74AC1	16245	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
t _{PLH}	A or B	B or A	2	4.6	6.9	2	7.9	2	7.9	ns	
t _{PHL}	AOIB	BULA	2.5	5.2	7.9	2.5	8.9	2.5	8.9	1115	
^t PZH	ŌĒ	A or B	2.3	4.9	7.5	2.3	8.6	2.3	8.6	no	
tPZL	OE	AUIB	3	6.2	9.5	3	10.7	3	10.7	ns	
^t PHZ	ŌĒ	A or B	5	7.2	9.1	5	9.8	5	9.8	ne	
t _{PLZ}	OE .	AUIB	4.2	6.2	8.1	4.2	8.7	4.2	8.7	ns	

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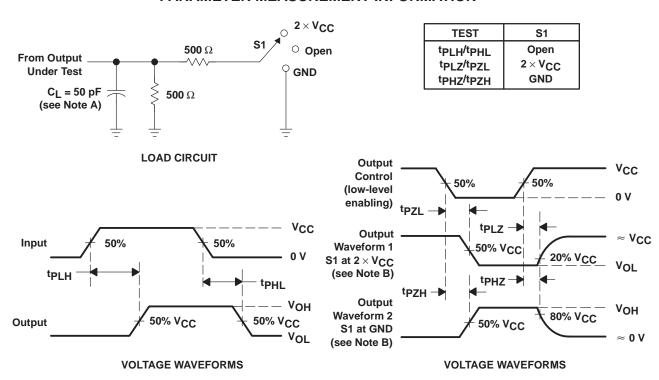


[‡] For I/O ports, the parameter IOZ includes the input leakage current.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
<u> </u>	Dower dissination conscitance nor lately	Outputs enabled	C: F0 %	43	pF
Cbq	Power dissipation capacitance per latch	Outputs disabled	$C_L = 50 \text{ pF}, f = 1 \text{ MHz}$	8	pr

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50~\Omega$, $t_f = 3~ns$, $t_f = 3~ns$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AC16245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16245DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

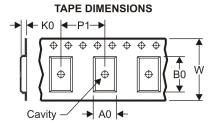
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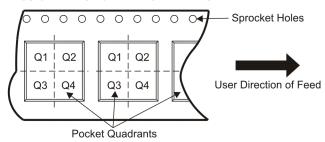
TAPE AND REEL INFORMATION





_		
	A0	Dimension designed to accommodate the component width
Γ	B0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC16245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC16245DLR	SSOP	DL	48	1000	346.0	346.0	49.0

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