

FEATURES

- Member of the Texas Instruments Widebus™ Family
- DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCB} Voltage
- If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.4-V to 3.6-V Power-Supply Range
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCB164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCB164245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCB} .

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CCB} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Tape and reel	74AVCB164245GRDR	WB4245
	FBGA – ZRD (Pb-Free)	Tape and reel	74AVCB164245ZRDR	
	TSSOP – DGG	Tape and reel	SN74AVCB164245GR	AVCB164245
	TVSOP – DGV	Tape and reel	SN74AVCB164245VR	WB4245
	VFBGA – GQL	Tape and reel	SN74AVCB164245KR	
	VFBGA – ZQL (Pb-Free)	Tape and reel	74AVCB164245ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

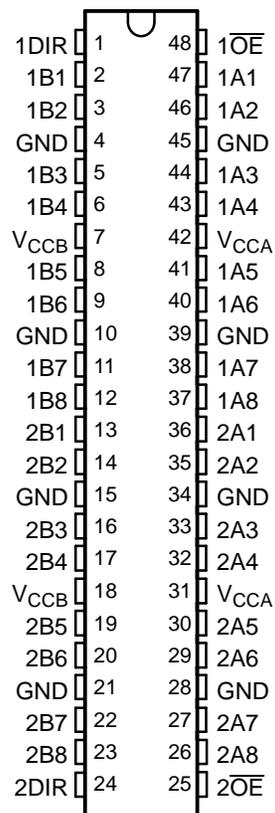
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SN74AVCB164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

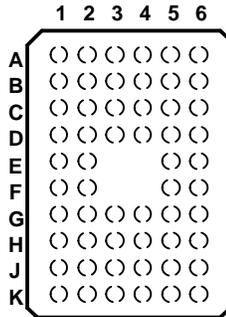
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TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE
(TOP VIEW)



**GQL OR ZQL PACKAGE
(TOP VIEW)**

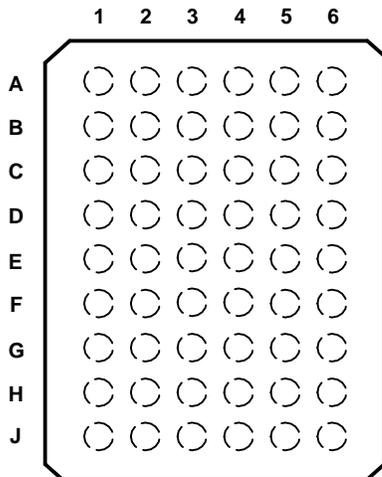


**TERMINAL ASSIGNMENTS
(56-Ball GQL/ZQL Package)⁽¹⁾**

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1 \overline{OE}
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V _{CCB}	V _{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V _{CCB}	V _{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2 \overline{OE}

(1) NC - No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS
(54-Ball GRD/ZRD Package)⁽¹⁾**

	1	2	3	4	5	6
A	1B1	NC	1DIR	1 \overline{OE}	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V _{CCB}	V _{CCA}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V _{CCB}	V _{CCA}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2 \overline{OE}	NC	2A8

(1) NC - No internal connection

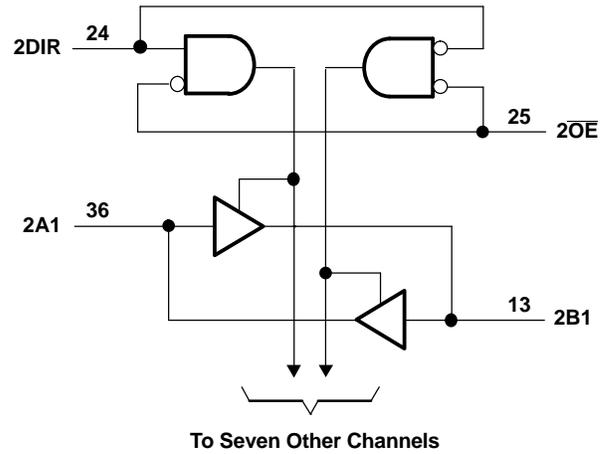
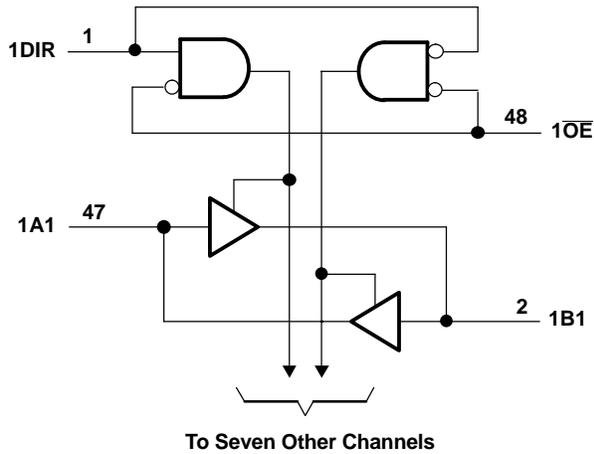
**FUNCTION TABLE
(EACH 8-BIT SECTION)**

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V_{CCA} V_{CCB}	Supply voltage range	-0.5	4.6	V	
V_I	Input voltage range ⁽²⁾	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA	
I_{OK}	Output clamp current	$V_O < 0$	-50	mA	
I_O	Continuous output current		50	mA	
		Continuous current through V_{CCA} , V_{CCB} , or GND	100		
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W	
		DGV package	58		
		GQL/ZQL package	28		
		GRD/ZRD package	36		
T_{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾

over operating free-air temperature range (unless otherwise noted)

		V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.4	3.6	V
V_{CCB}	Supply voltage			1.4	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		$V_{CCI} \times 0.65$	V
			1.95 V to 2.7 V		1.7	
			2.7 V to 3.6 V		2	
V_{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V		$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V		0.7	
			2.7 V to 3.6 V		0.8	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V		$V_{CCB} \times 0.65$	V
			1.95 V to 2.7 V		1.7	
			2.7 V to 3.6 V		2	
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V		$V_{CCB} \times 0.35$	V
			1.95 V to 2.7 V		0.7	
			2.7 V to 3.6 V		0.8	
V_I	Input voltage			0	3.6	V
V_O	Output voltage	Active state		0	V_{CCO}	V
		3-state		0	3.6	
I_{OH}	High-level output current		1.4 V to 1.6 V		–2	mA
			1.65 V to 1.95 V		–4	
			2.3 V to 2.7 V		–8	
			3 V to 3.6 V		–12	
I_{OL}	Low-level output current		1.4 V to 1.6 V		2	mA
			1.65 V to 1.95 V		4	
			2.3 V to 2.7 V		8	
			3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.

(2) V_{CCO} is the V_{CC} associated with the data output port.

(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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16-BIT DUAL-SUPPLY BUS TRANSCEIVER
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Electrical Characteristics⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	MIN	TYP ⁽³⁾	MAX	UNIT
V _{OH}		I _{OH} = –100 μA	V _I = V _{IH}	1.4 V to 3.6 V	1.4 V to 3.6 V	V _{CCO} – 0.2			V
		I _{OH} = –2 mA	V _I = V _{IH}	1.4 V	1.4 V	1.05			
		I _{OH} = –4 mA	V _I = V _{IH}	1.65 V	1.65 V	1.2			
		I _{OH} = –8 mA	V _I = V _{IH}	2.3 V	2.3 V	1.75			
		I _{OH} = –12 mA	V _I = V _{IH}	3 V	3 V	2.3			
V _{OL}		I _{OH} = 100 μA	V _I = V _{IL}	1.4 V to 3.6 V	1.4 V to 3.6 V	0.2			V
		I _{OH} = 2 mA	V _I = V _{IL}	1.4 V	1.4 V	0.35			
		I _{OH} = 4 mA	V _I = V _{IL}	1.65 V	1.65 V	0.45			
		I _{OH} = 8 mA	V _I = V _{IL}	2.3 V	2.3 V	0.55			
		I _{OH} = 12 mA	V _I = V _{IL}	3 V	3 V	0.7			
I _I	Control inputs	V _I = V _{CCB} or GND		1.4 V to 3.6 V	3.6 V	±2.5			μA
I _{off}	A port	V _I or V _O = 0 to 3.6 V		0 V	0 to 3.6 V	±10			μA
	B port			0 to 3.6 V	0 V	±10			
I _{OZ} ⁽⁴⁾	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V	±12.5			μA
	B port		$\overline{OE} = \text{don't care}$	0 V	3.6 V	±12.5			
	A port		$\overline{OE} = \text{don't care}$	3.6 V	0 V	±12.5			
I _{CCA}	V _I = V _{CCI} or GND, I _O = 0			1.6 V	1.6 V	20			μA
				1.95 V	1.95 V	20			
				2.7 V	2.7 V	30			
				0 V	3.6 V	–40			
				3.6 V	0 V	40			
				3.6 V	3.6 V	40			
I _{CCB}	V _I = V _{CCI} or GND, I _O = 0			1.6 V	1.6 V	20			μA
				1.95 V	1.95 V	20			
				2.7 V	2.7 V	30			
				0 V	3.6 V	40			
				3.6 V	0 V	–40			
				3.6 V	3.6 V	40			
C _i	Control inputs	V _I = 3.3 V or GND		3.3 V	3.3 V	4			pF
C _{io}	A or B ports	V _O = 3.3 V or GND		3.3 V	3.3 V	5			pF

- (1) V_{CCO} is the V_{CC} associated with the output port.
- (2) V_{CCI} is the V_{CC} associated with the input port.
- (3) All typical values are at T_A = 25°C.
- (4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t_{en}	\overline{OE}	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
		B	2.1	9	2.9	9.8	3.2	10	3	9.8	
t_{dis}	\overline{OE}	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
		B	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t_{en}	\overline{OE}	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t_{dis}	\overline{OE}	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
		B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	\overline{OE}	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
t_{dis}	\overline{OE}	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
		B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	\overline{OE}	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
		B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t_{dis}	\overline{OE}	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
		B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

Operating Characteristics

V_{CCA} and $V_{CCB} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	14	pF
		Outputs disabled	7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled	20	
		Outputs disabled	7	
C_{pdB} (V_{CCB})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	20	pF
		Outputs disabled	7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled	14	
		Outputs disabled	7	

Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

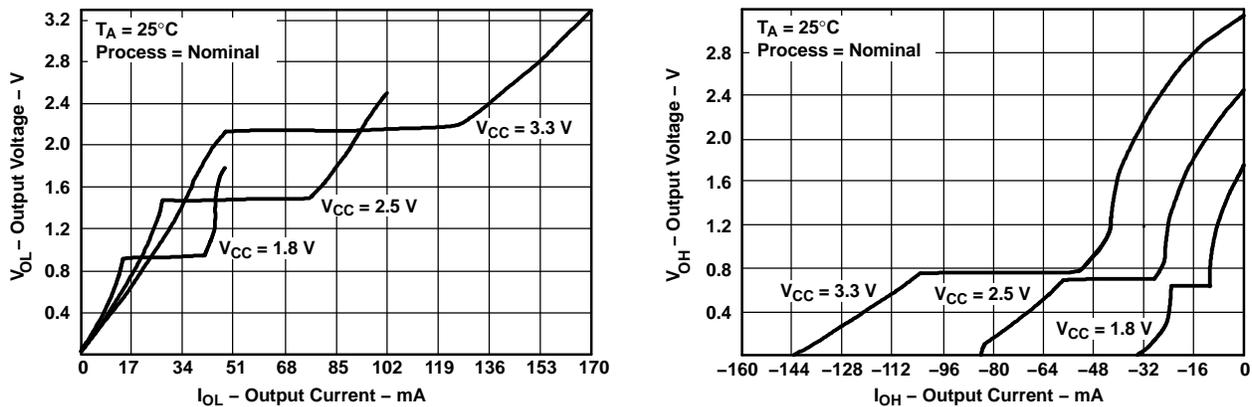
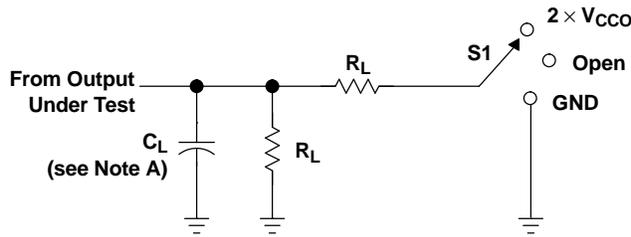


Figure 1. Typical Output Voltage vs Output Current

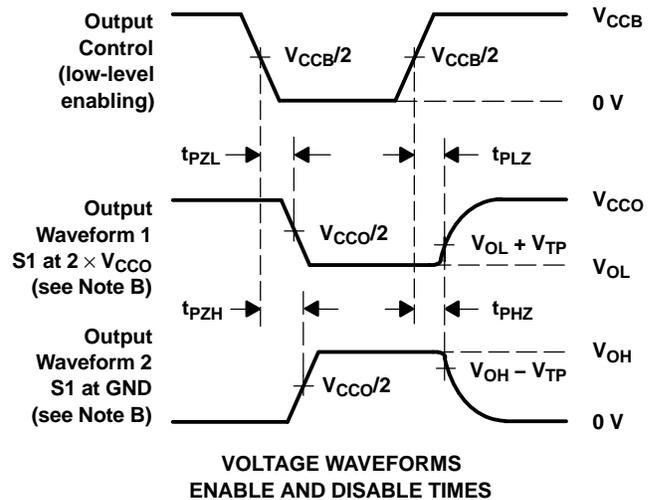
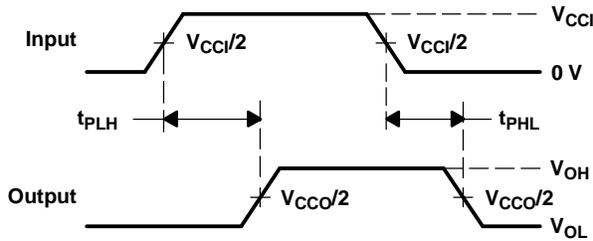
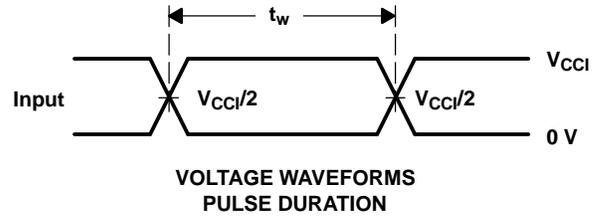
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

V _{CCO}	C _L	R _L	V _{TP}
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	30 pF	500 Ω	0.3 V

TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	2 × V _{CCO}
t _{PHZ} /t _{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 H. V_{CCi} is the V_{CC} associated with the input port.
 I. V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AVCB164245GRDR	ACTIVE	BGA MI CROSTAR JUNIOR	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
74AVCB164245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVCB164245GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVCB164245VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVCB164245VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVCB164245ZQLR	ACTIVE	BGA MI CROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
74AVCB164245ZRDR	ACTIVE	BGA MI CROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74AVCB164245DGG	PREVIEW	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVCB164245GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVCB164245KR	NRND	BGA MI CROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74AVCB164245VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

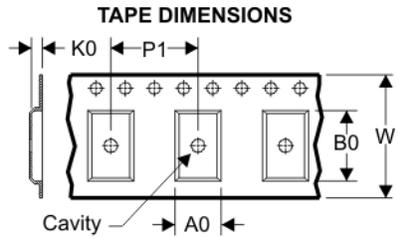
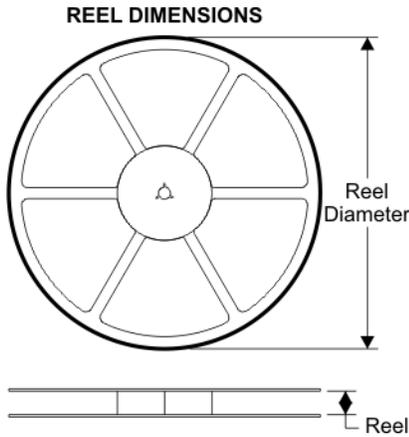
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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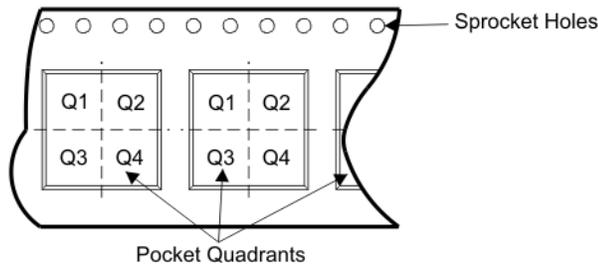
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TAPE AND REEL BOX INFORMATION



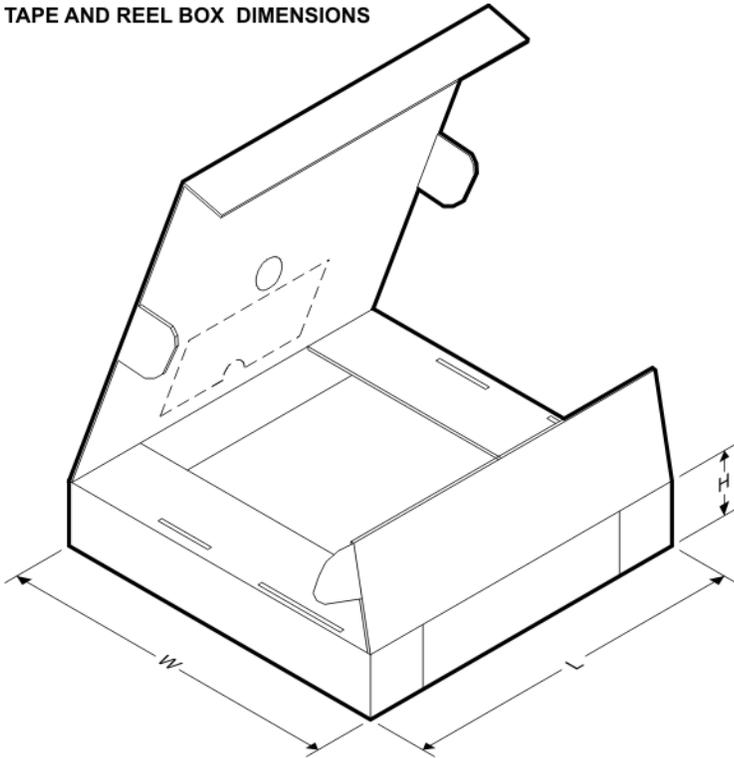
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCB164245GRDR	GRD	54	SITE 32	330	16	5.8	8.3	1.55	8	16	Q1
74AVCB164245ZQLR	ZQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
74AVCB164245ZQLR	ZQL	56	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
74AVCB164245ZRDR	ZRD	54	SITE 32	330	16	5.8	8.3	1.55	8	16	Q1
SN74AVCB164245GR	DGG	48	SITE 41	330	24	8.6	15.8	1.8	12	24	Q1
SN74AVCB164245KR	GQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74AVCB164245KR	GQL	56	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
SN74AVCB164245VR	DGV	48	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1

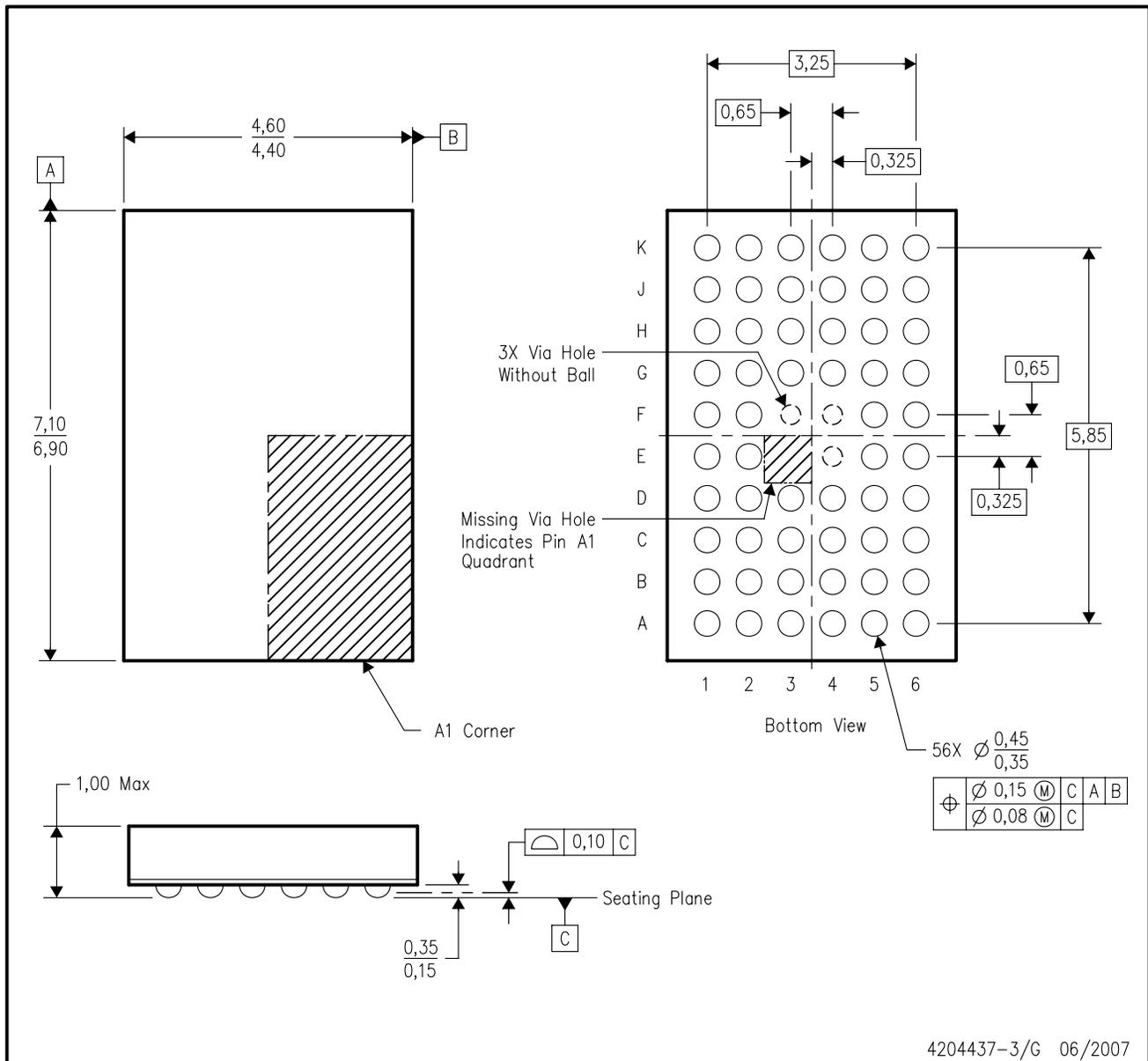
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
74AVCB164245GRDR	GRD	54	SITE 32	346.0	346.0	33.0
74AVCB164245ZQLR	ZQL	56	SITE 32	346.0	346.0	33.0
74AVCB164245ZQLR	ZQL	56	SITE 60	342.9	345.9	28.58
74AVCB164245ZRDR	ZRD	54	SITE 32	346.0	346.0	33.0
SN74AVCB164245GR	DGG	48	SITE 41	346.0	346.0	41.0
SN74AVCB164245KR	GQL	56	SITE 32	346.0	346.0	33.0
SN74AVCB164245KR	GQL	56	SITE 60	342.9	345.9	28.58
SN74AVCB164245VR	DGV	48	SITE 41	346.0	346.0	41.0

ZQL (R-PBGA-N56)

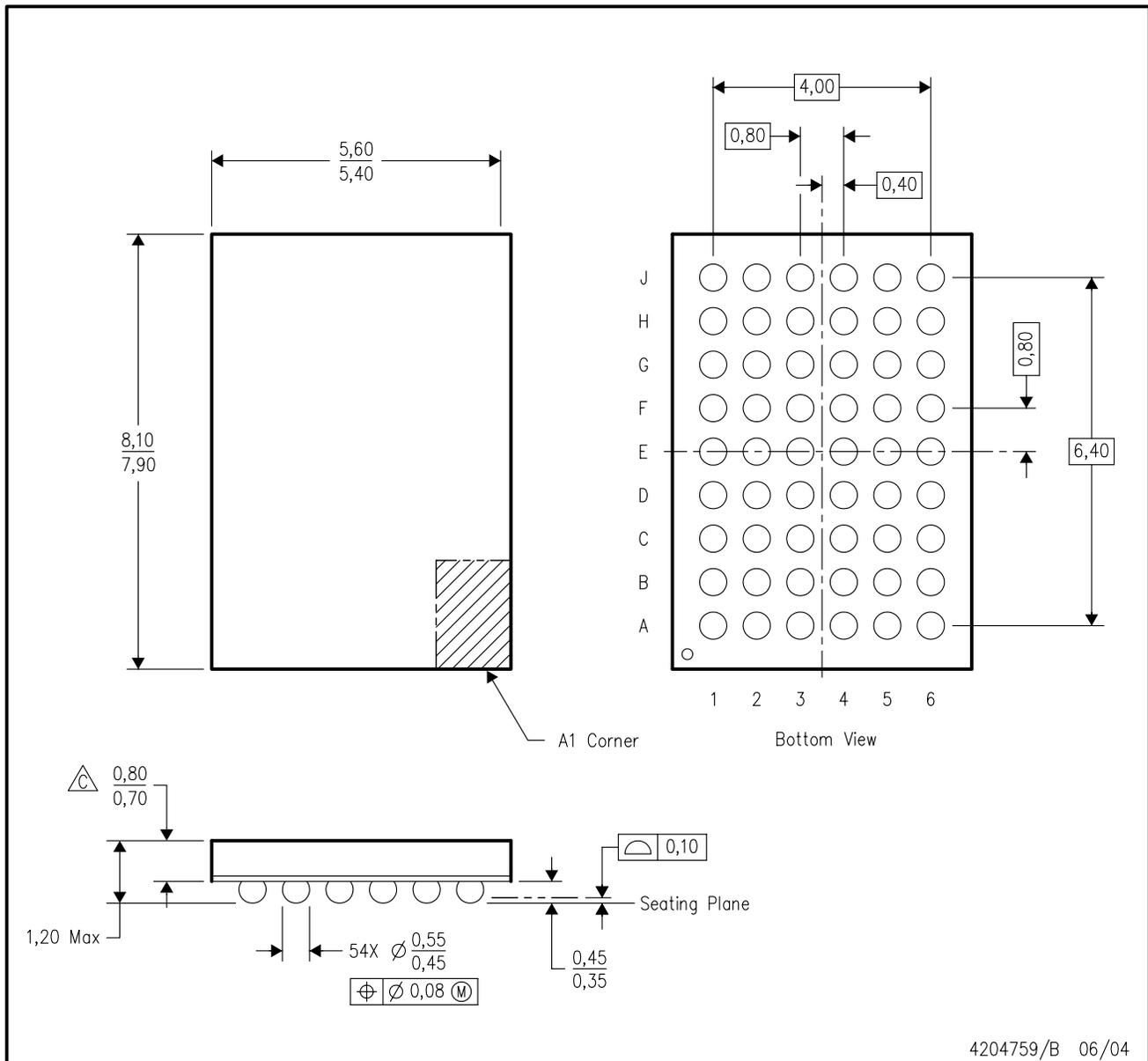
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GRD (R-PBGA-N54)

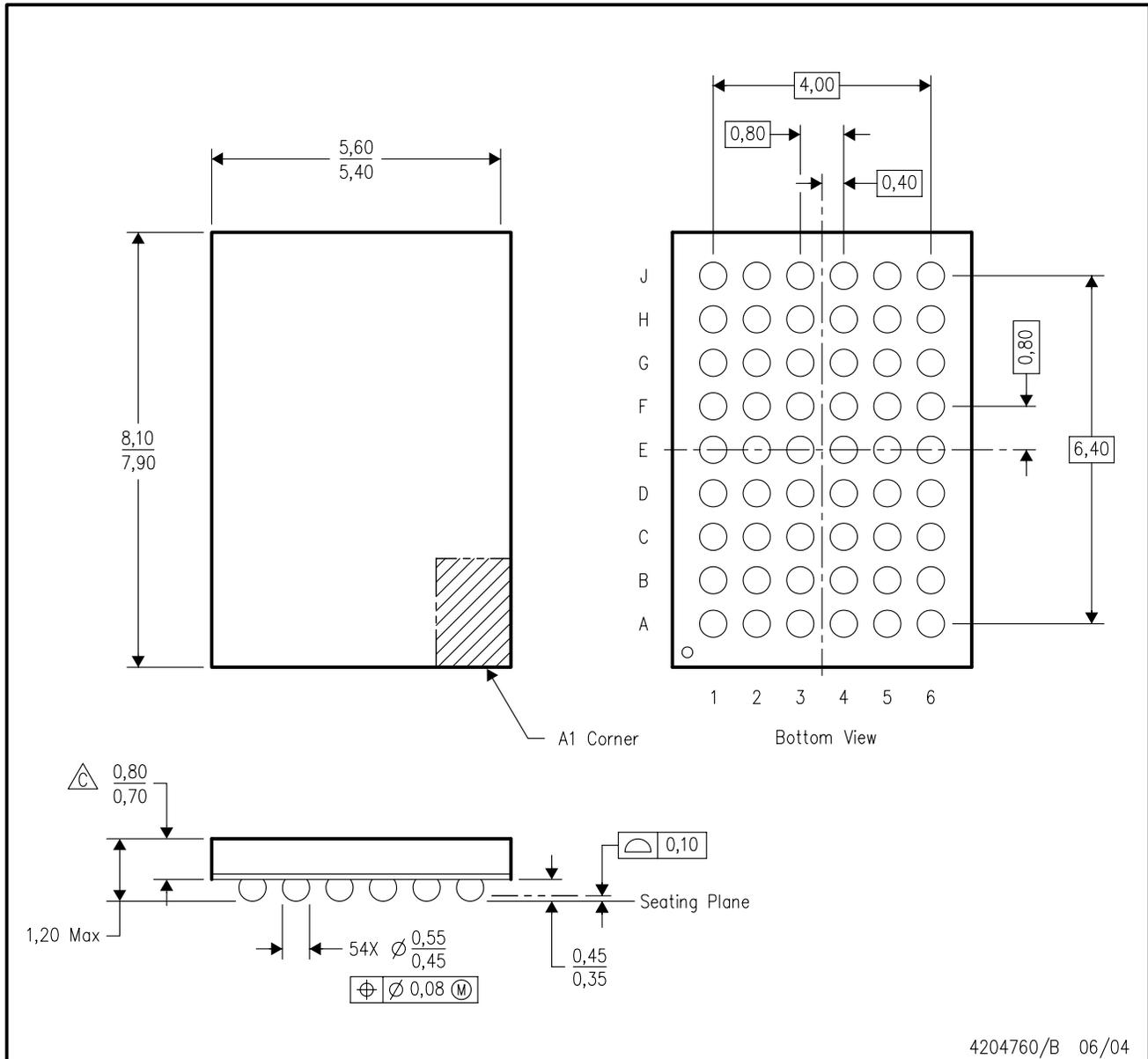
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DD.
 - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY

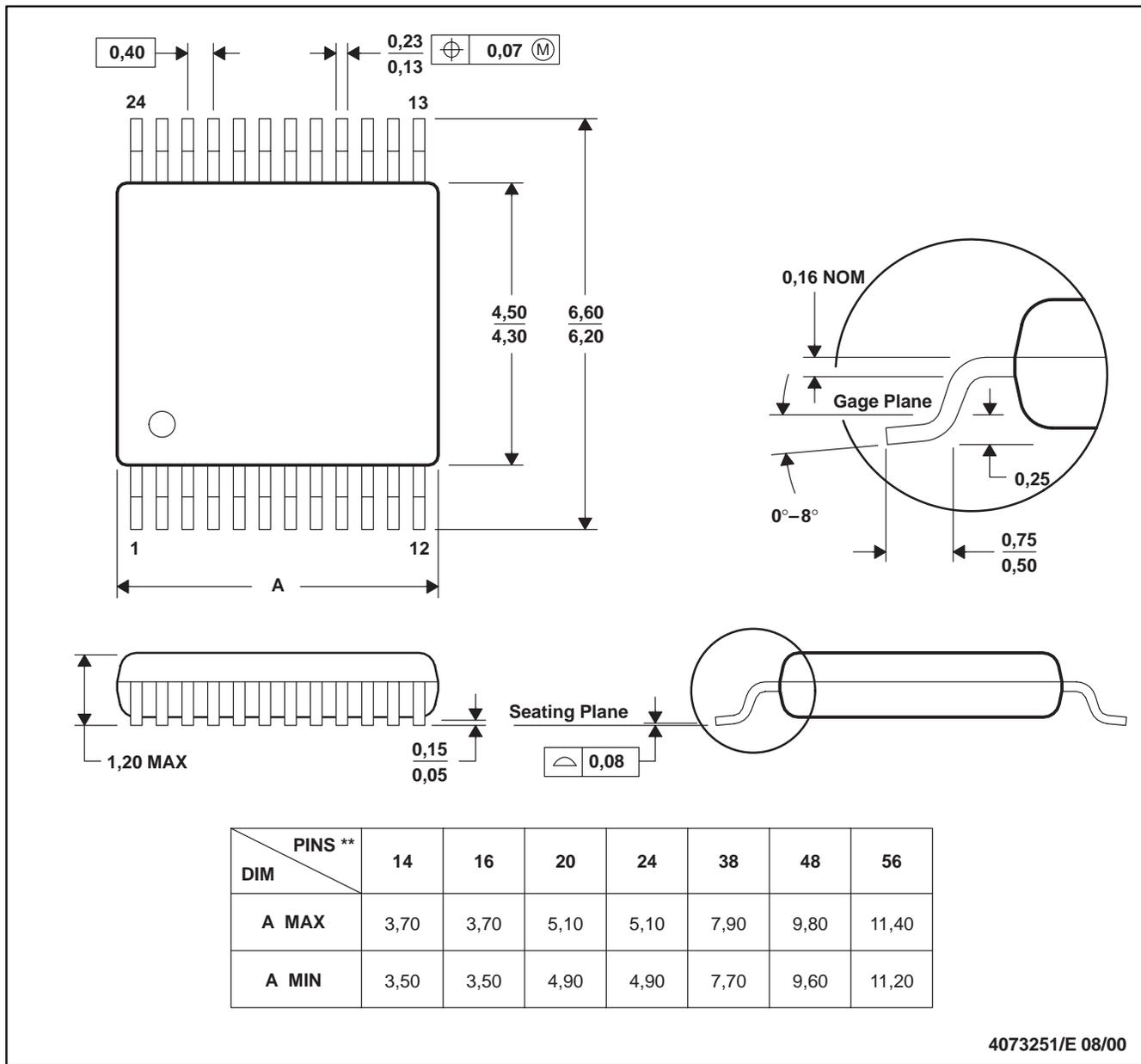


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

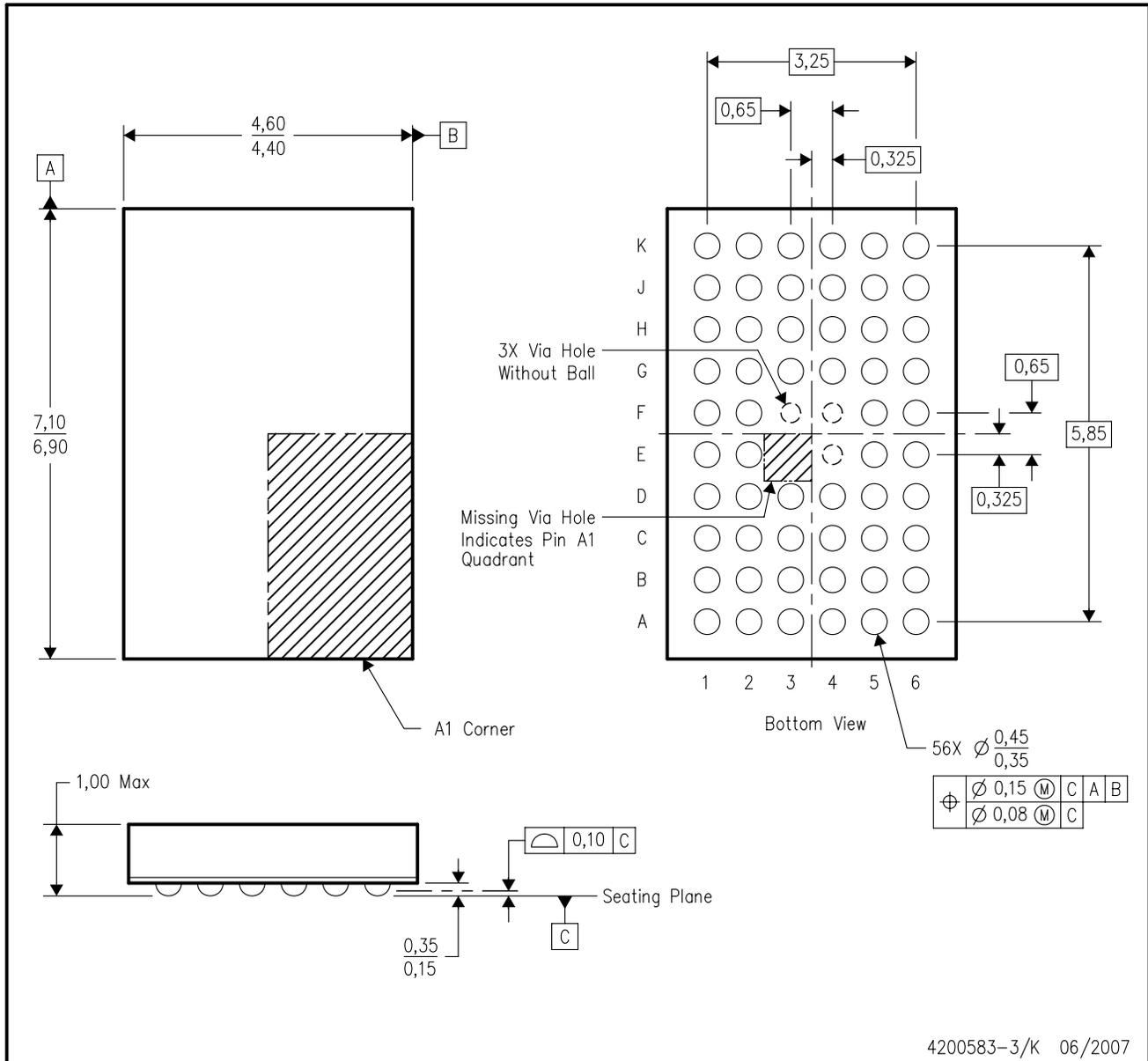


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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

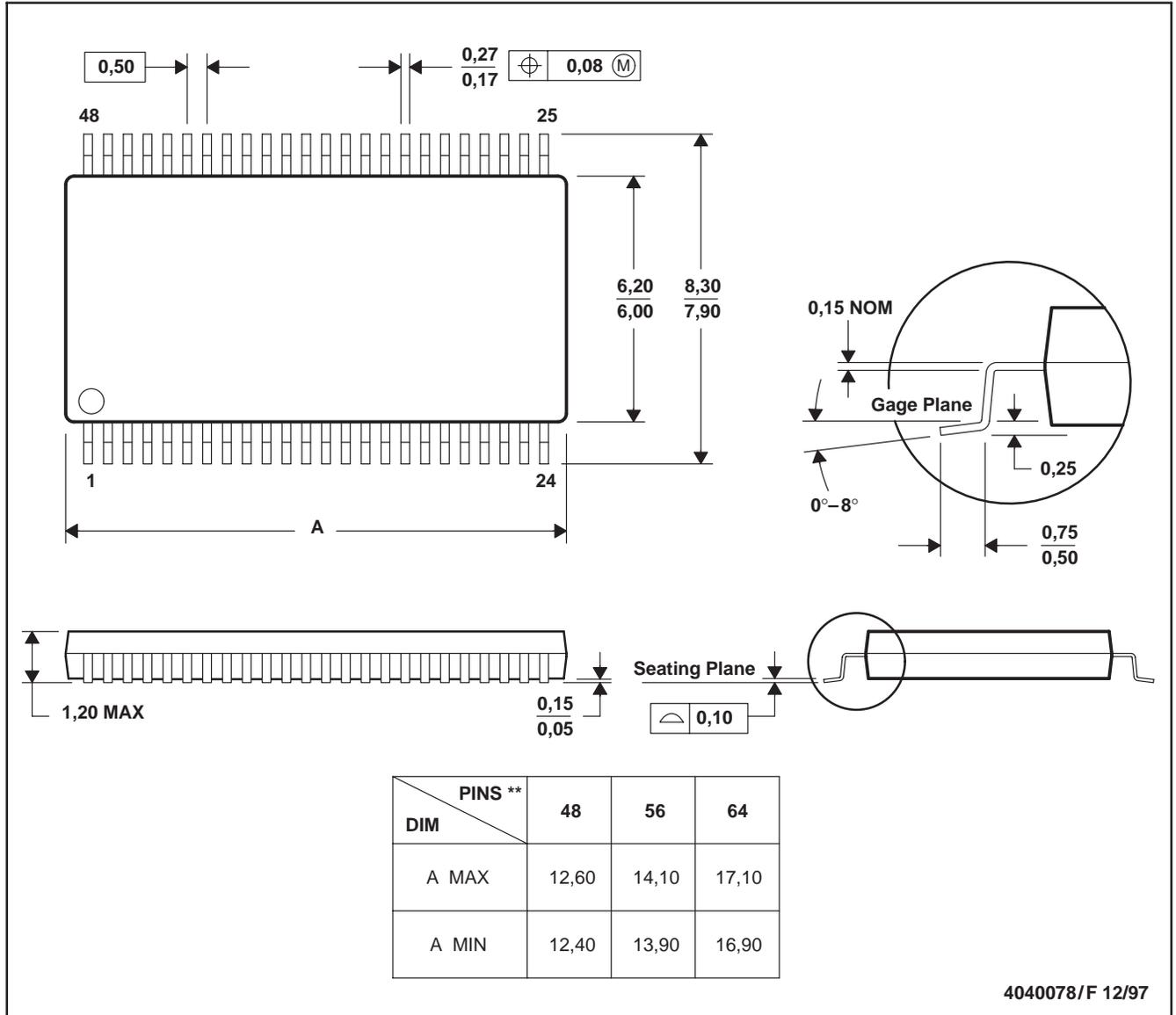


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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