- **Member of the Texas Instruments Widebus+™ Family**
- **DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of**
  - **±24 mA at 3-V V_{CC}**
  - **±15 mA at 2.3-V V_{CC}**
  - **±9 mA at 1.65-V V_{CC}**
  - **±6 mA at 1.4-V V_{CC}**
- **Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCB} Voltage**
- **If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **Inputs/Outputs Can Tolerate Up to 4.6 V, Which Allows Mixed-Voltage-Mode Data Communications**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

description/ordering information

This 32-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCB324245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCB324245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are supplied by V_{CCB}.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CCB} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

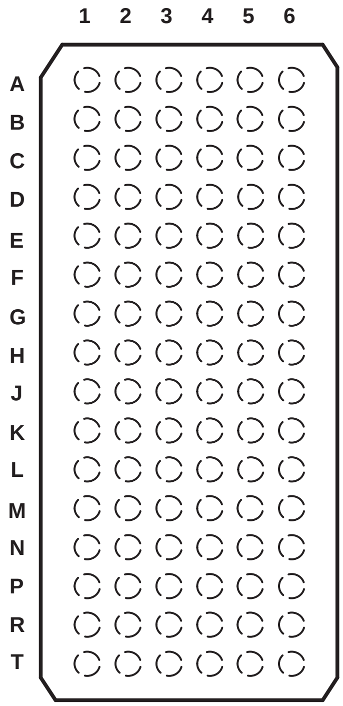
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA − GKE	Tape and reel	SN74AVCB324245KR	WD4245
	LFBGA − ZKE (Pb-free)		74AVCB324245ZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GKE OR ZKE PACKAGE
(TOP VIEW)



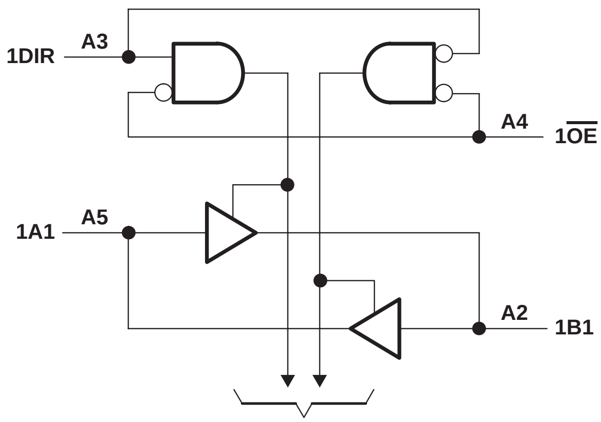
terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	1DIR	$1\overline{OE}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CCB}	V_{CCA}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CCB}	V_{CCA}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	$2\overline{OE}$	2A8	2A7
J	3B2	3B1	3DIR	$3\overline{OE}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CCB}	V_{CCA}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CCB}	V_{CCA}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	$4\overline{OE}$	4A8	4A7

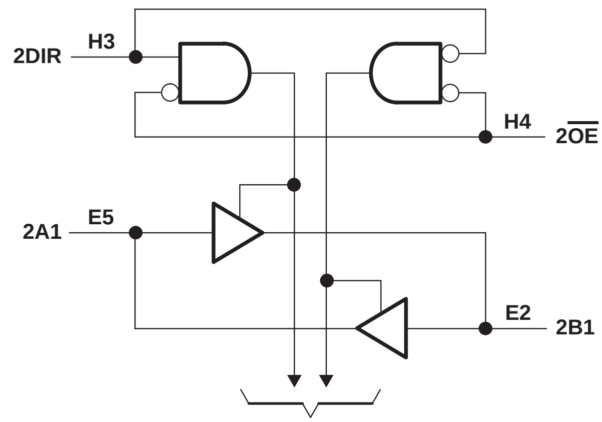
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

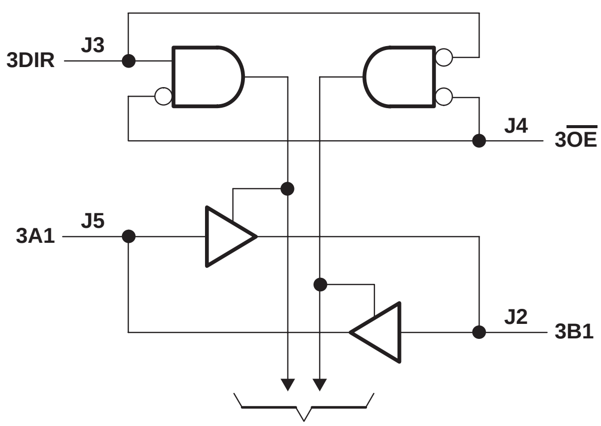
logic diagram (positive logic)



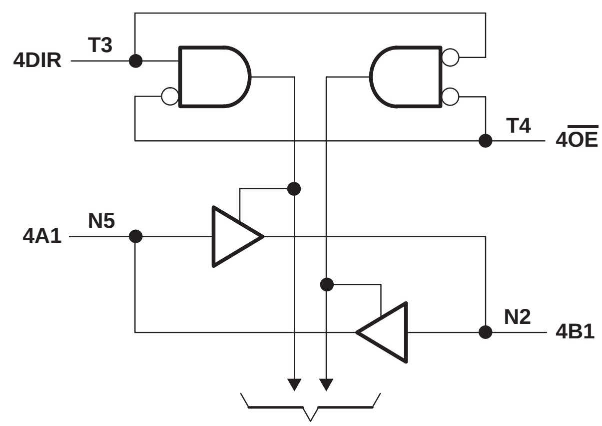
To Seven Other Channels



To Seven Other Channels



To Seven Other Channels



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): I/O ports (A port)	−0.5 V to 4.6 V
I/O ports (B port)	−0.5 V to 4.6 V
Control inputs	−0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): (A port)	−0.5 V to 4.6 V
(B port)	−0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2): (A port)	−0.5 V to V_{CCA} + 0.5 V
(B port)	−0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CCA}, V_{CCB}, or GND pin	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): GKE/ZKE package	40°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 6)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.4	3.6	V
V_{CCB}	Supply voltage				1.4	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		$V_{CCI} \times 0.65$	3.6	V
			1.95 V to 2.7 V		1.7	3.6	
			2.7 V to 3.6 V		2	3.6	
V_{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V		0	$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V		0	0.7	
			2.7 V to 3.6 V		0	0.8	
V_{IH}	High-level input voltage	Control inputs (Referenced to V_{CCB})	1.4 V to 1.95 V		$V_{CCB} \times 0.65$	V_{CCB}	V
			1.95 V to 2.7 V		1.7	V_{CCB}	
			2.7 V to 3.6 V		2	V_{CCB}	
V_{IL}	Low-level input voltage	Control inputs (Referenced to V_{CCB})	1.4 V to 1.95 V		0	$V_{CCB} \times 0.35$	V
			1.95 V to 2.7 V		0	0.7	
			2.7 V to 3.6 V		0	0.8	
V_O	Output voltage				0	V_{CCO}	V
I_{OH}	High-level output current			1.4 V to 1.6 V		−2	mA
				1.65 V to 1.95 V		−4	
				2.3 V to 2.7 V		−8	
				3 V to 3.6 V		−12	
I_{OL}	Low-level output current			1.4 V to 1.6 V		2	mA
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = −100 µA	$V_I = V_{IH}$	1.4 V to 3.6 V	1.4 V to 3.6 V	V_{CCO}−0.2			V
		I_{OH} = −2 mA	$V_I = V_{IH}$	1.4 V	1.4 V	1.05			
		I_{OH} = −4 mA	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		I_{OH} = −8 mA	$V_I = V_{IH}$	2.3 V	2.3 V	1.75			
		I_{OH} = −12 mA	$V_I = V_{IH}$	3 V	3 V	2.3			
V_{OL}		I_{OH} = 100 µA	$V_I = V_{IL}$	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		I_{OH} = 2 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35	
		I_{OH} = 4 mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		I_{OH} = 8 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.55	
		I_{OH} = 12 mA	$V_I = V_{IL}$	3 V	3 V			0.7	
V_{OH}		I_{OHD} = −6 mA	$V_I = V_{IH}$	1.4 V	1.4 V	1.05			V
		I_{OHD} = −9 mA	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		I_{OHD} = −15 mA	$V_I = V_{IH}$	2.3 V	2.3 V	1.75			
		I_{OHD} = −24 mA	$V_I = V_{IH}$	3 V	3 V	2.3			
V_{OL}		I_{OHD} = 6 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35	V
		I_{OHD} = 9 mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		I_{OHD} = 15 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.55	
		I_{OHD} = 24 mA	$V_I = V_{IL}$	3 V	3 V			0.7	
I_I	Control inputs	$V_I = V_{CCB}$ or GND		1.4 V to 3.6 V	3.6 V			±2.5	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V			±10	µA
	B port			0 to 3.6 V	0 V			±10	
I_{OZ}‡	A or B ports	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V			±12.5	µA
	B port		$\overline{OE}$ = don't care	0 V	3.6 V			±12.5	
	A port			3.6 V	0 V			±12.5	
I_{CCA}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.6 V	1.6 V			40	µA
				1.95 V	1.95 V			40	
				2.7 V	2.7 V			60	
				0 V	3.6 V			−80	
				3.6 V	0 V			80	
				3.6 V	3.6 V			80	
I_{CCB}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.6 V	1.6 V			40	µA
				1.95 V	1.95 V			40	
				2.7 V	2.7 V			60	
				0 V	3.6 V			80	
				3.6 V	0 V			−80	
				3.6 V	3.6 V			80	
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		4		pF
C_{io}	A or B ports	V_O = 3.3 V or GND		3.3 V	3.3 V		5		pF

† All typical values are at T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
NOTES: 4. V_{CCI} is the V_{CC} associated with the input port.
5. V_{CCO} is the V_{CC} associated with the output port.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.9	6.4	1.8	5.5	1.5	5.8	ns
	B	A	1.8	6.8	1.7	6.2	1.6	5.9	1.5	5.9	
t_{en}	$\overline{OE}$	A	2.1	9	2.9	9.8	3.2	10	3	9.8	ns
		B	2.5	8.4	2.4	8	2.3	7.6	2.2	7.5	
t_{dis}	$\overline{OE}$	A	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	ns
		B	2.2	6.9	1.8	6.4	1.1	5.8	1.8	5.7	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.4	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	2	6.6	1.8	6	1.8	5.6	1.8	5.5	
t_{en}	$\overline{OE}$	A	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	ns
		B	2.5	8.2	2.5	7.5	2.4	7.4	2.3	7.2	
t_{dis}	$\overline{OE}$	A	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	ns
		B	2.5	6.7	2.3	6.1	2.2	5.5	1.3	5.3	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.5	3.4	ns
	B	A	1.7	5.4	1.7	4.6	1.5	4	1.5	3.7	
t_{en}	$\overline{OE}$	A	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	ns
		B	3.1	6.1	2.5	5.6	2.2	5.3	1.9	4.2	
t_{dis}	$\overline{OE}$	A	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	ns
		B	2.4	6	3	5.2	1.4	3.6	1.2	3	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.5	5.8	1.5	4.2	1.5	3.3	1.4	3.1	
t_{en}	$\overline{OE}$	A	1.6	4.9	2	4.5	2	4.3	1.9	4.1	ns
		B	2	5.1	2	4.6	2.2	5.2	1.9	4.1	
t_{dis}	$\overline{OE}$	A	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	ns
		B	2.3	5.5	1.9	4.5	1.3	3.5	1.2	3.5	

operating characteristics, V_{CCA} and V_{CCB} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power-dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	14	pF
		Outputs disabled		7	
	Power-dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB} (V_{CCB})	Power-dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	20	pF
		Outputs disabled		7	
	Power-dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		14	
		Outputs disabled		7	

output description

The dynamic output control (DOC™) circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

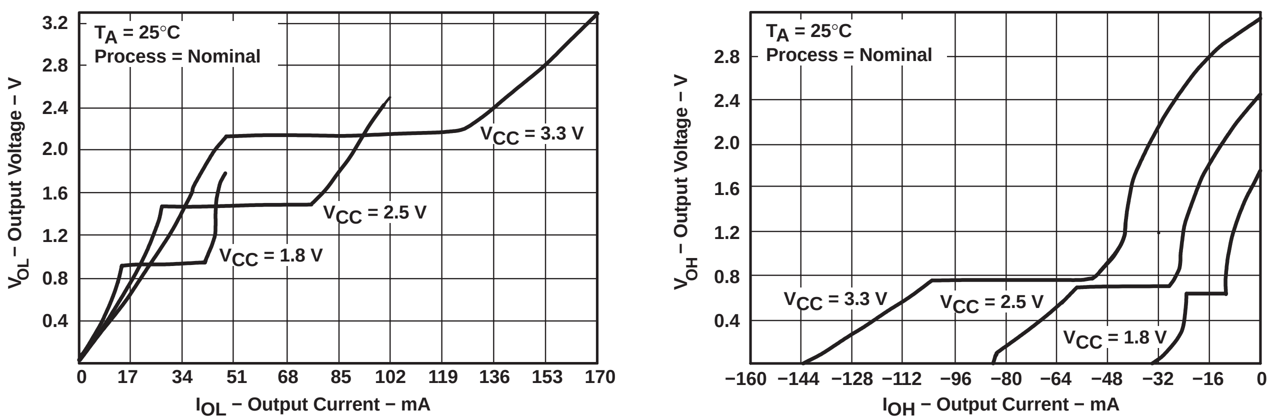
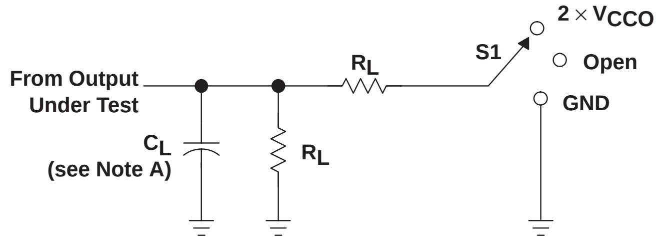


Figure 1. Typical Output Voltage vs Output Current

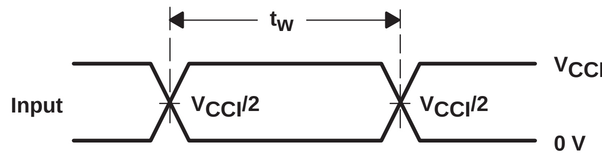
PARAMETER MEASUREMENT INFORMATION



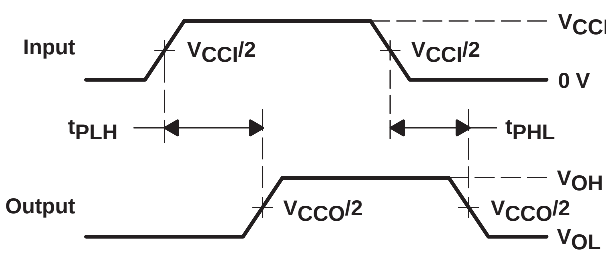
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

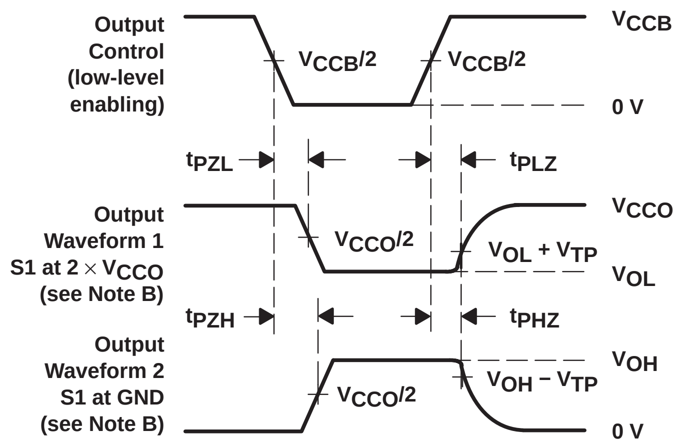
V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	30 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

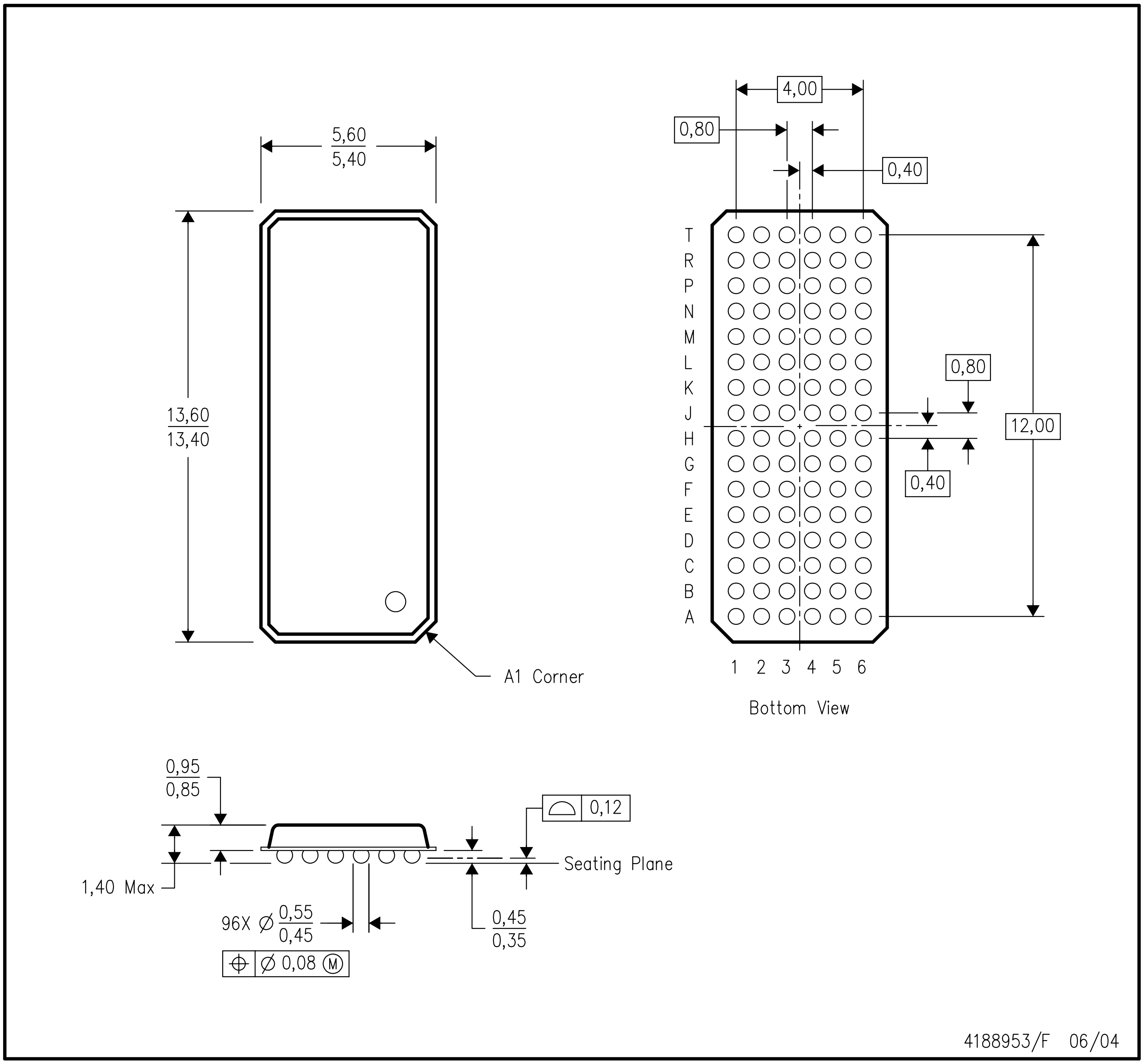


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns, dv/dt ≥1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

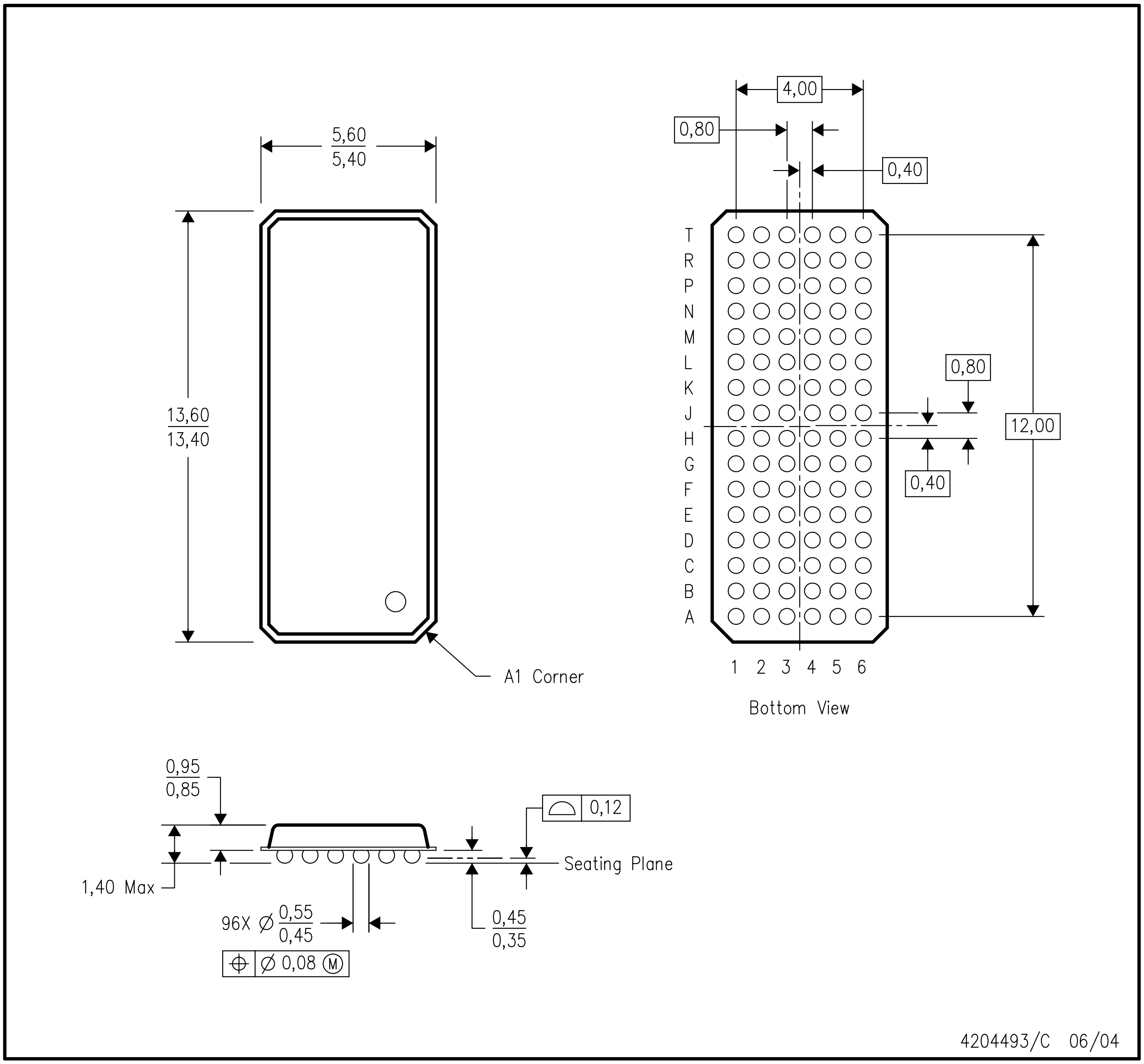
Figure 2. Load Circuit and Voltage Waveforms

GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–205 variation CC.
- D. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MO–205 variation CC.

D. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).