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- **Member of the Texas Instruments** Widebus+™ Family
- **DOC™ Circuitry Dynamically Changes** Output Impedance, Resulting in Noise **Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to** Standard Outputs With IOH and IOL of
  - ±24 mA at 3-V V<sub>CC</sub>
  - ±15 mA at 2.3-V V<sub>CC</sub>
  - $\pm$ 9 mA at 1.65-V V<sub>CC</sub>
  - $-\pm 6$  mA at 1.4-V V<sub>CC</sub>
- Control Inputs VIH/VIL Levels are Referenced to V<sub>CCB</sub> Voltage
- If Either V<sub>CC</sub> Input Is at GND, Both Ports Are in the High-Impedance State

- Inputs/Outputs Can Tolerate Up to 4.6 V, Which Allows Mixed-Voltage-Mode Data Communications
- Ioff Supports Partial-Power-Down Mode Operation
- **Fully Configurable Dual-Rail Design Allows** Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### description/ordering information

This 32-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track V<sub>CCB</sub>. V<sub>CCB</sub> accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCB324245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCB324245 is designed so that the control pins (1DIR, 2DIR,  $1\overline{OE}$ , and  $2\overline{OE}$ ) are supplied by  $V_{CCB}$ .

To ensure the high-impedance state during power up or power down,  $\overline{\sf OE}$  shall be tied to  ${\sf V}_{\sf CCB}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V<sub>CC</sub> input is at GND, both ports are in the high-impedance state.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA – GKE	Tono and roal	SN74AVCB324245KR	WD4245
-40 C 10 85°C	LFBGA – ZKE (Pb-free)	Tape and reel	74AVCB324245ZKER	VV D4240

<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



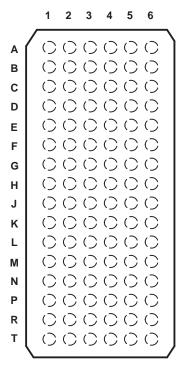
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# GKE OR ZKE PACKAGE (TOP VIEW)



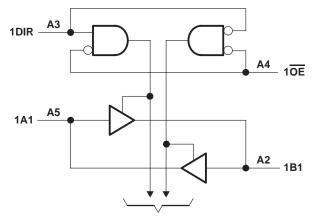
### terminal assignments

	1	2	3	4	5	6
Α	1B2	1B1	1DIR	1OE	1A1	1A2
В	1B4	1B3	GND	GND	1A3	1A4
С	1B6	1B5	VCCB	VCCA	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	VCCB	VCCA	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
Н	2B7	2B8	2DIR	2OE	2A8	2A7
J	3B2	3B1	3DIR	3OE	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	VCCB	VCCA	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
Р	4B4	4B3	VCCB	VCCA	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
Т	4B7	4B8	4DIR	4OE	4A8	4A7

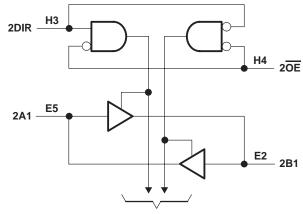
# FUNCTION TABLE (each 8-bit section)

INP	UTS	
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

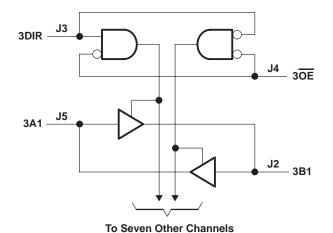
### logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels



Т3 4DIR -**T4** - 4<del>0E</del> N5 4A1 -N2 4B1 To Seven Other Channels

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, $V_{CCA}$ and $V_{CCB}$	.6 V .6 V
Voltage range applied to any output in the high-impedance or power-off state, V <sub>O</sub>	
(see Note 1): (A port)	.6 V
(B port)	
Voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2): (A port)	.5 V
(B port)	.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	mΑ
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	mΑ
Continuous output current, IO ±50	mΑ
Continuous current through each V <sub>CCA</sub> , V <sub>CCB</sub> , or GND pin ±100	mΑ
Package thermal impedance, θ <sub>JA</sub> (see Note 3): GKE/ZKE package	C/W
Storage temperature range, T <sub>stg</sub> –65°C to 15	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

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### recommended operating conditions (see Notes 4 through 6)

			VCCI	Vcco	MIN	MAX	UNIT
VCCA	Supply voltage				1.4	3.6	V
V <sub>CCB</sub>	Supply voltage				1.4	3.6	V
			1.4 V to 1.95 V		V <sub>CCI</sub> × 0.65	3.6	
٧ <sub>IH</sub>	High-level input voltage	Data inputs	1.95 V to 2.7 V		1.7	3.6	V
	voltage		2.7 V to 3.6 V		2	3.6	
			1.4 V to 1.95 V		0	V <sub>CCI</sub> × 0.35	
$\vee_{IL}$	Low-level input voltage	Data inputs	1.95 V to 2.7 V		0	0.7	V
	voltago		2.7 V to 3.6 V		0		
			1.4 V to 1.95 V		V <sub>CCB</sub> ×0.65	V <sub>CCB</sub>	
$V_{IH}$	High-level input voltage	Control inputs (Referenced to V <sub>CCB</sub> )	1.95 V to 2.7 V		1.7	V <sub>CCB</sub>	V
	voltage	(vereinged to ACCB)	2.7 V to 3.6 V		2	VCCB	
			1.4 V to 1.95 V		0	V <sub>CCB</sub> ×0.35	
$V_{IL}$	Low-level input voltage	Control inputs (Referenced to V <sub>CCB</sub> )	1.95 V to 2.7 V		0	0.7	V
	voltage	(Izeleteticed to ACCB)	2.7 V to 3.6 V		0	0.8	
VO	Output voltage				0	Vcco	V
				1.4 V to 1.6 V		-2	
				1.65 V to 1.95 V		-4	
ІОН	High-level output curre	ent		2.3 V to 2.7 V		-8	mA
				3 V to 3.6 V		-12	
				1.4 V to 1.6 V		2	
				1.65 V to 1.95 V		4	
lOL	Low-level output curre	nτ		2.3 V to 2.7 V		8	mA
				3 V to 3.6 V		12	
Δt/Δν	Input transition rise or	fall rate				5	ns/V
TA	Operating free-air tem	perature			-40	85	°C

NOTES: 4.  $V_{CCI}$  is the  $V_{CC}$  associated with the data input port.

5.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.



All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 4 and 5)

PA	RAMETER	TEST CONDIT	IONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>†</sup>	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	$V_I = V_{IH}$	1.4 V to 3.6 V	1.4 V to 3.6 V	V <sub>CCO</sub> -0.2				
		I <sub>OH</sub> = -2 mA	$V_I = V_{IH}$	1.4 V	1.4 V	1.05				
Vон		I <sub>OH</sub> = -4 mA	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			V	
		I <sub>OH</sub> = -8 mA	$V_I = V_{IH}$	2.3 V	2.3 V	1.75				
		I <sub>OH</sub> = -12 mA	$V_I = V_{IH}$	3 V	3 V	2.3				
		ΙΟΗ = 100 μΑ	$V_I = V_{IL}$	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2		
		I <sub>OH</sub> = 2 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35		
VOL		I <sub>OH</sub> = 4 mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	V	
		I <sub>OH</sub> = 8 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.55		
		I <sub>OH</sub> = 12 mA	$V_I = V_{IL}$	3 V	3 V			0.7		
		$I_{OHD} = -6 \text{ mA}$	$V_I = V_{IH}$	1.4 V	1.4 V	1.05				
.,		$I_{OHD} = -9 \text{ mA}$	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			V	
VOH		I <sub>OHD</sub> = -15 mA	VI = VIH	2.3 V	2.3 V	1.75			V	
		I <sub>OHD</sub> = -24 mA	$V_I = V_{IH}$	3 V	3 V	2.3				
		I <sub>OHD</sub> = 6 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35		
,,		I <sub>OHD</sub> = 9 mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	.,	
VOL		IOHD = 15 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.55	V	
		I <sub>OHD</sub> = 24 mA	$V_I = V_{IL}$	3 V	3 V			0.7		
IĮ	Control inputs	$V_I = V_{CCB}$ or GND		1.4 V to 3.6 V	3.6 V			±2.5	μΑ	
	A port	V -= V 04- 2 C V		0 V	0 to 3.6 V			±10		
loff	B port	$V_I$ or $V_O = 0$ to 3.6 V		0 to 3.6 V	0 V			±10	μΑ	
	A or B ports		OE = V <sub>IH</sub>	3.6 V	3.6 V			±12.5		
loz‡	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	OE = don't	0 V	3.6 V			±12.5	.5 μΑ	
	A port	17 1667 5.15	care	3.6 V	0 V			±12.5		
	•			1.6 V	1.6 V			40		
				1.95 V	1.95 V			40		
				2.7 V	2.7 V			60		
ICCA		$V_I = V_{CCI}$ or GND,	IO = 0	0 V	3.6 V			-80	μΑ	
				3.6 V	0 V			80		
				3.6 V	3.6 V			80		
				1.6 V	1.6 V			40		
				1.95 V	1.95 V			40		
l		V. V OND	1- 0	2.7 V	2.7 V			60		
ICCB		$V_I = V_{CCI}$ or GND,	IO = 0	0 V	3.6 V			80	μΑ	
				3.6 V	0 V			-80		
				3.6 V	3.6 V			80		
Ci	Control inputs	V <sub>I</sub> = 3.3 V or GND		3.3 V	3.3 V		4		pF	
C <sub>io</sub>	A or B ports	$V_O = 3.3 \text{ V or GND}$		3.3 V	3.3 V		5		pF	

<sup>†</sup> All typical values are at  $T_A = 25^{\circ}C$ .

NOTES: 4.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

5.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.



<sup>‡</sup> For I/O ports, the parameter IOZ includes the input leakage current.

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# switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 V $\pm$ 0.1 V (see Figure 2)

PARAMETER	FROM	TO		/ <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V	
(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
	Α	В	1.7	6.7	1.9	6.4	1.8	5.5	1.5	5.8	
<sup>t</sup> pd	В	Α	1.8	6.8	1.7	6.2	1.6	5.9	1.5	5.9	ns
	<del></del>	Α	2.1	9	2.9	9.8	3.2	10	3	9.8	
<sup>t</sup> en	ŌĒ	В	2.5	8.4	2.4	8	2.3	7.6	2.2	7.5	ns
	ŌĒ	А	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	
<sup>t</sup> dis	OE OE	В	2.2	6.9	1.8	6.4	1.1	5.8	1.8	5.7	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 1.8 V $\pm$ 0.15 V (see Figure 2)

PARAMETER	FROM			V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V	
(INPUT	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Α	В	1.7	6.4	1.8	6	1.7	4.7	1.6	4.3	
<sup>t</sup> pd	В	Α	2	6.6	1.8	6	1.8	5.6	1.8	5.5	ns
	<del></del>	А	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t <sub>en</sub>	ŌĒ	В	2.5	8.2	2.5	7.5	2.4	7.4	2.3	7.2	ns
	ŌĒ	А	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	
<sup>t</sup> dis	OE	В	2.5	6.7	2.3	6.1	2.2	5.5	1.3	5.3	ns

# switching characteristics over recommended operating free-air temperature range, $V_{\text{CCA}}$ = 2.5 V $\pm$ 0.2 V (see Figure 2)

PARAMETER	FROM	TO	V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
,	Α	В	1.6	6	1.8	5.6	1.5	4	1.5	3.4	
<sup>t</sup> pd	В	А	1.7	5.4	1.7	4.6	1.5	4	1.5	3.7	ns
,	<del></del>	А	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
<sup>t</sup> en	ŌĒ	В	3.1	6.1	2.5	5.6	2.2	5.3	1.9	4.2	ns
	<del></del>	А	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	
<sup>t</sup> dis	ŌĒ	В	2.4	6	3	5.2	1.4	3.6	1.2	3	ns

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# switching characteristics over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V $\pm$ 0.3 V (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)		V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Α	В	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	
<sup>t</sup> pd	В	Α	1.5	5.8	1.5	4.2	1.5	3.3	1.4	3.1	ns
	ŌĒ	Α	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t <sub>en</sub>	OE	В	2	5.1	2	4.6	2.2	5.2	1.9	4.1	ns
	<del></del>	Α	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	
<sup>t</sup> dis	ŌĒ	В	2.3	5.5	1.9	4.5	1.3	3.5	1.2	3.5	ns

## operating characteristics, $V_{CCA}$ and $V_{CCB}$ = 3.3 V, $T_A$ = 25°C

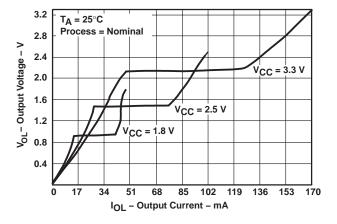
	PARAMETER		TEST C	ONDITIONS	TYP	UNIT
	Power-dissipation capacitance per transceiver,	Outputs enabled			14	
C <sub>pdA</sub>	A-port input, B-port output	Outputs disabled	]	4 40 MIL	7	
(VCCA)	Power-dissipation capacitance per transceiver,	Outputs enabled	$C_L = 0$ ,	f = 10 MHz	20	pF
	B-port input, A-port output	Outputs disabled			7	
	Power-dissipation capacitance per transceiver,	Outputs enabled			20	
C <sub>pdB</sub>	A-port input, B-port output	Outputs disabled	]	( 40 MIL	7	
(VCCB)	Power-dissipation capacitance per transceiver,	Outputs enabled	$C_L = 0$ ,	f = 10 MHz	14	pF
	B-port input, A-port output	Outputs disabled			7	



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#### output description

The dynamic output control ( $DOC^{TM}$ ) circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, AVC Logic Family Technology and Applications, literature number SCEA006, and Dynamic Output Control ( $DOC^{TM}$ ) Circuitry Technology and Applications, literature number SCEA009.



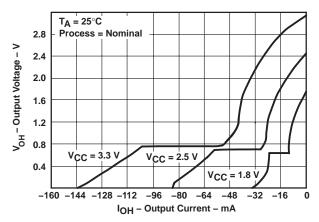
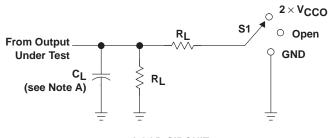


Figure 1. Typical Output Voltage vs Output Current

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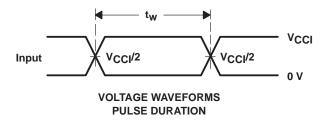
#### PARAMETER MEASUREMENT INFORMATION



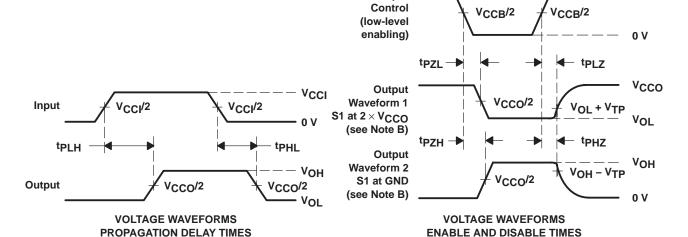
TEST	S1
t <sub>pd</sub>	Open
tPLZ/tPZL	2×V <sub>CCO</sub>
tPHZ/tPZH	GND

**LOAD CIRCUIT** 

Vcco	CL	RL	V <sub>TP</sub>
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	30 pF	<b>500</b> Ω	0.3 V



**VCCB** 



Output

NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

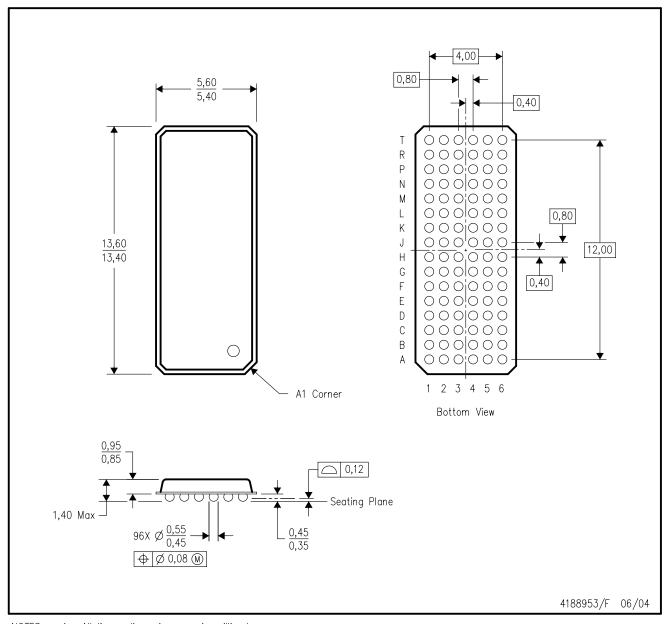
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{O}$  = 50  $\Omega$ , dv/dt  $\geq$  1 V/ns, dv/dt ≥1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. VCCI is the VCC associated with the input port.
- I. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms



## GKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY



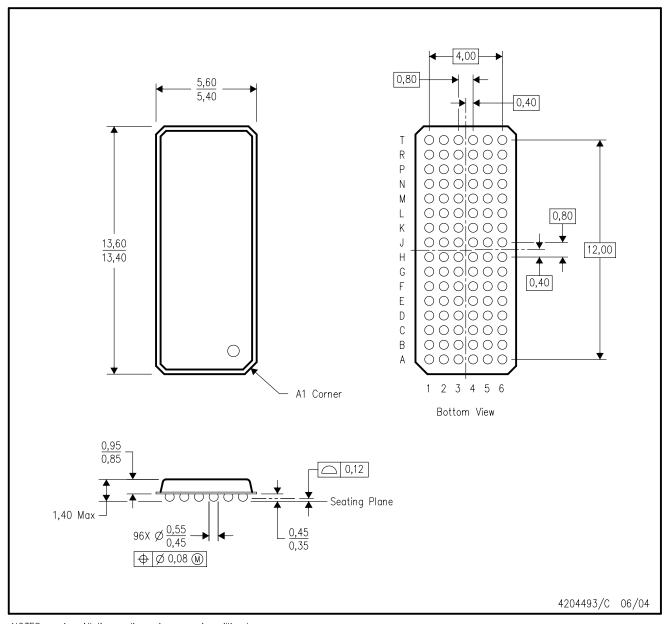
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.



## ZKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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