

SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

- 3-State Q Outputs Drive Bus Lines Directly
- Counter Operation Independent of 3-State Output
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

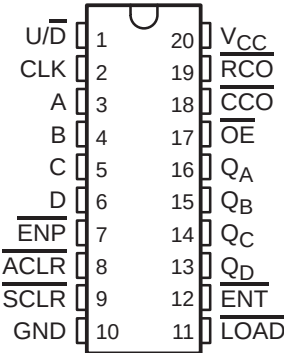
The SN74ALS568A decade counter and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock (CLK) input.

The clear function is initiated by applying a low level to either asynchronous clear ($\overline{\text{ACLR}}$) or synchronous clear ($\overline{\text{SCLR}}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding load ($\overline{\text{LOAD}}$) low during a positive-going clock transition. The counting function is enabled only when enable P ($\overline{\text{ENP}}$) and enable T ($\overline{\text{ENT}}$) are low and $\overline{\text{ACLR}}$, $\overline{\text{SCLR}}$, and $\overline{\text{LOAD}}$ are high. The up/down ($\text{U}/\overline{\text{D}}$) input controls the direction of the count. These counters count up when $\text{U}/\overline{\text{D}}$ is high and count down when $\text{U}/\overline{\text{D}}$ is low.

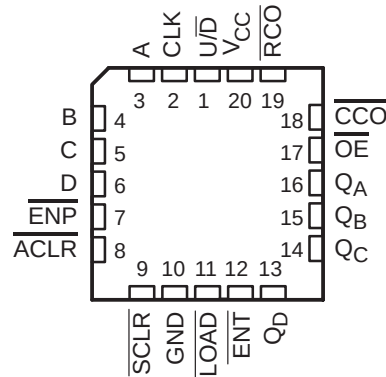
A high level at the output-enable ($\overline{\text{OE}}$) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{\text{OE}}$. $\overline{\text{ENT}}$ is fed forward to enable the ripple-carry output ($\overline{\text{RCO}}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The clocked carry output ($\overline{\text{CCO}}$) produces a low-level pulse for a duration equal to that of the low level of the clock when $\overline{\text{RCO}}$ is low and the counter is enabled (both $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ are low); otherwise, $\overline{\text{CCO}}$ is high. $\overline{\text{CCO}}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting $\overline{\text{RCO}}$ or $\overline{\text{CCO}}$ of the first counter to $\overline{\text{ENT}}$ of the next counter. However, for very high-speed counting, $\overline{\text{RCO}}$ should be used for cascading since $\overline{\text{CCO}}$ does not become active until the clock returns to the low level.

The SN54ALS569A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS568A and SN74ALS569A are characterized for operation from 0°C to 70°C .

SN54ALS569A . . . J PACKAGE
SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS569A . . . FK PACKAGE
(TOP VIEW)



SN54ALS569A, SN74ALS568A, SN74ALS569A

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS								OPERATION
$\overline{OE}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	$U/\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	↑	Synchronous clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count up
L	H	H	H	L	L	L	↑	Count down
L	H	H	H	H	X	X	X	Inhibit count
L	H	H	H	X	H	X	X	Inhibit count

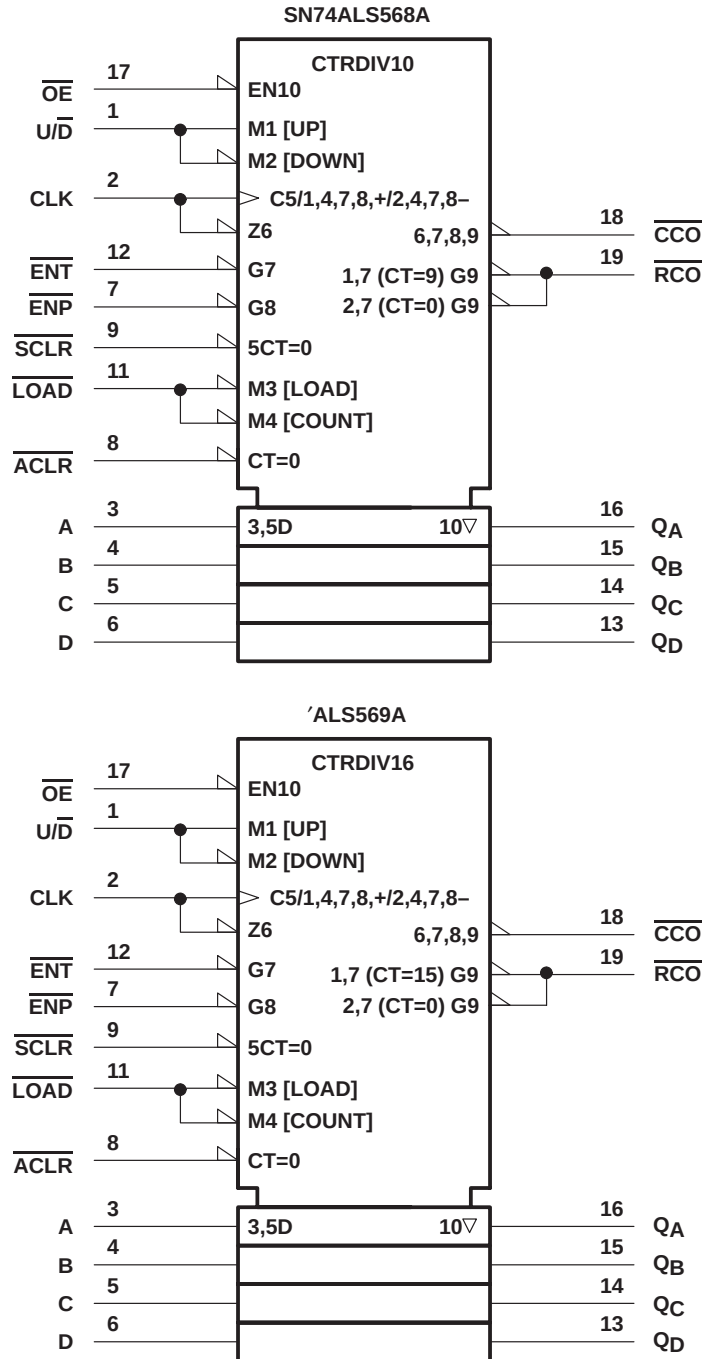


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logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

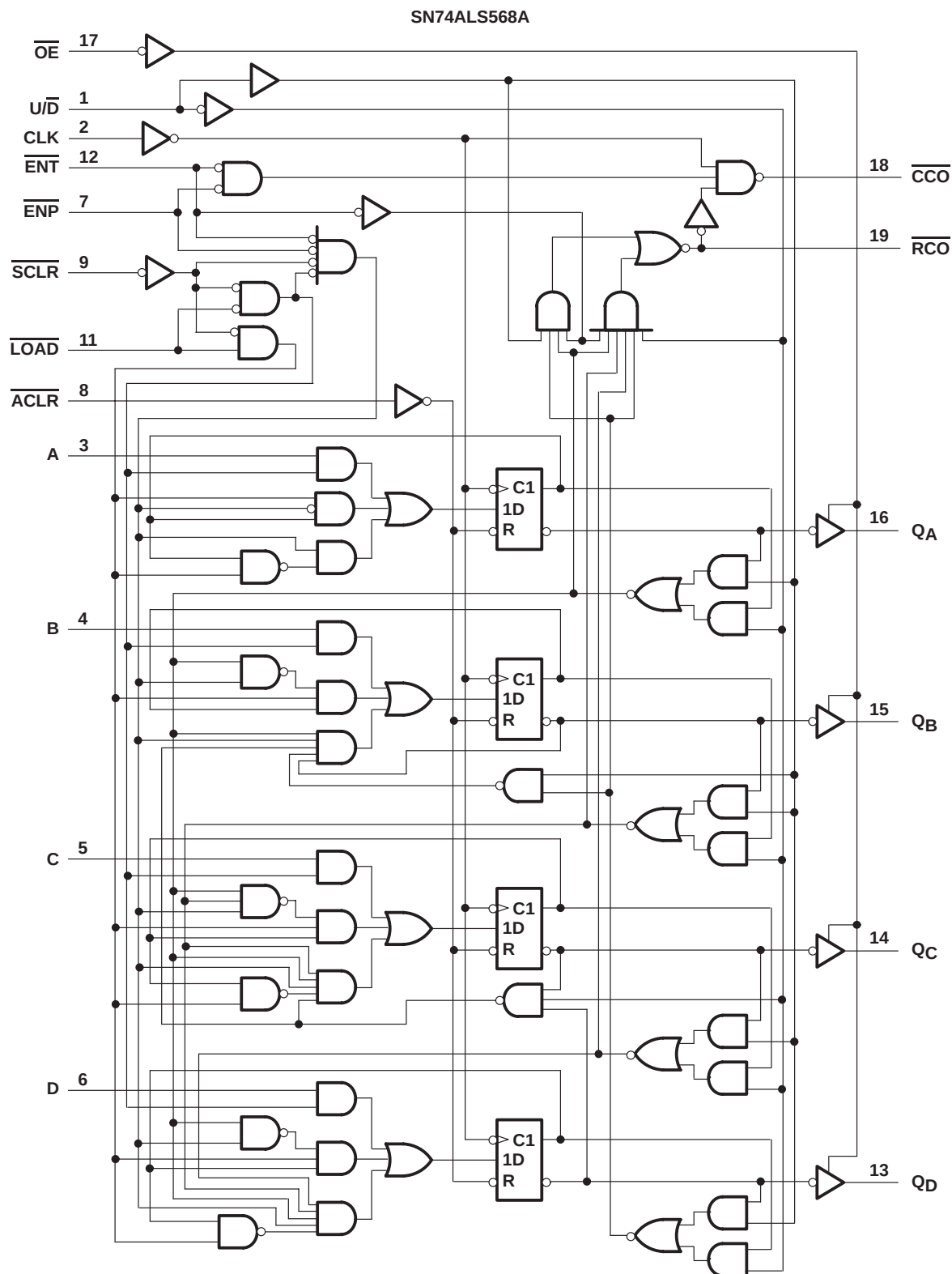
SN54ALS569A, SN74ALS568A, SN74ALS569A

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

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logic diagrams (positive logic)

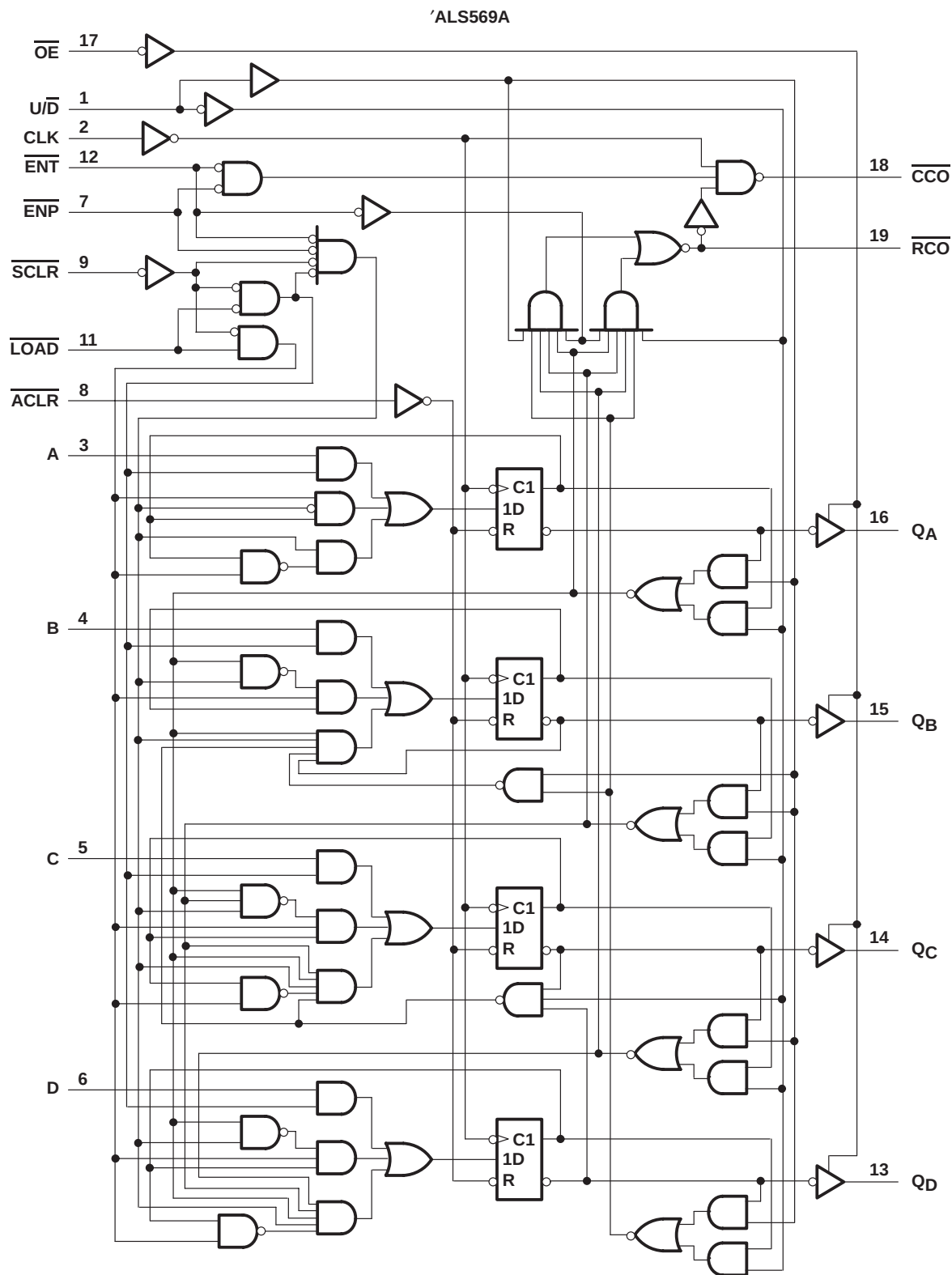


SN54ALS569A, SN74ALS568A, SN74ALS569A

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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logic diagrams (positive logic) (continued)



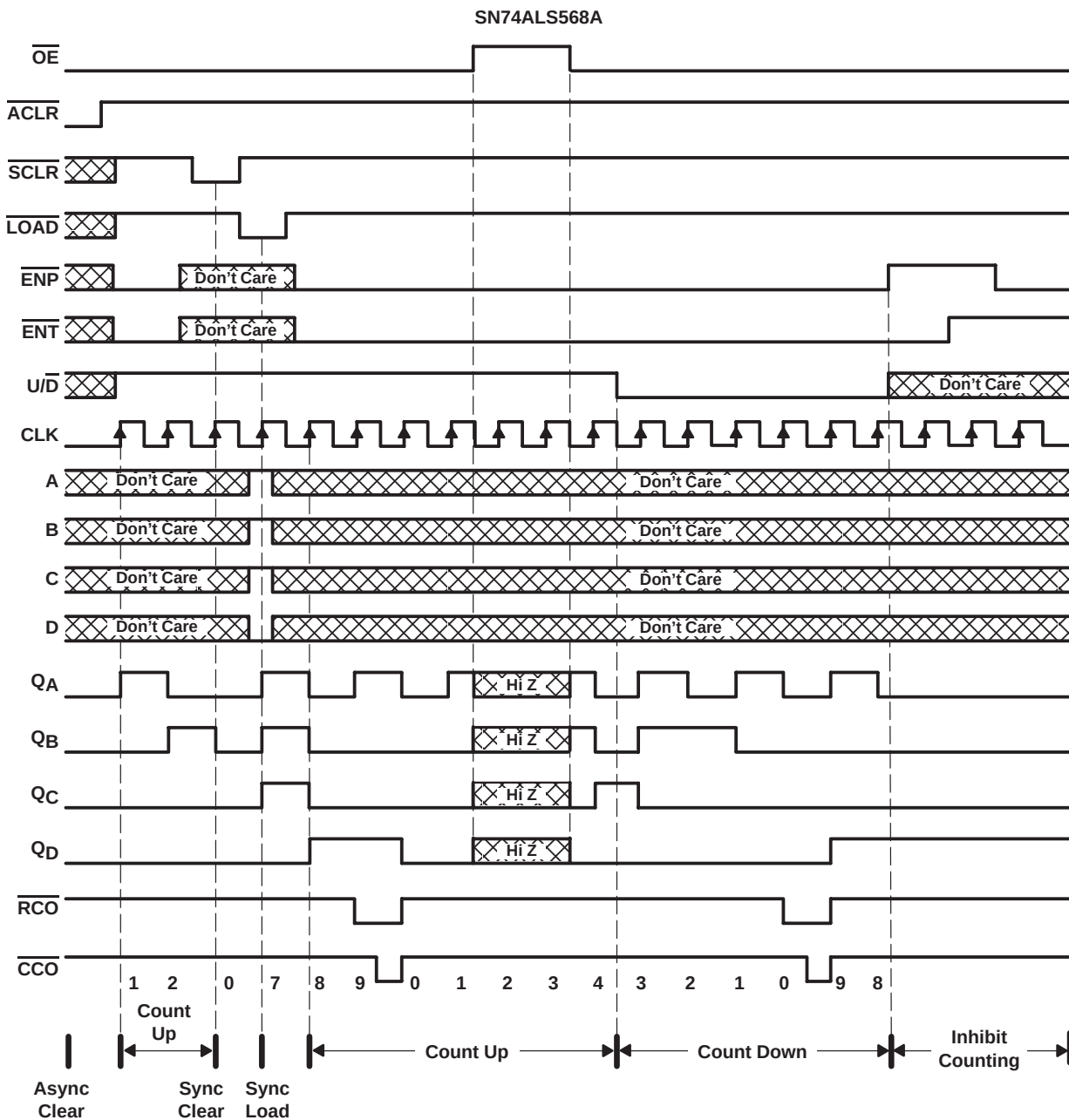
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typical load, count, and inhibit sequences



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The timing diagram for the 74ALS569A 4-bit counter shows the following signals and their behavior:

- OE**: Output Enable. Active low. High when outputs are disabled (Hi Z).
- ACLR**: Asynchronous Clear. Active low. High when counter is cleared to 0.
- SCLR**: Synchronous Clear. Active low. High when counter is cleared to 0 on the next clock edge.
- LOAD**: Load. Active low. High when counter is loaded with the value in A, B, C, D on the next clock edge.
- ENP**: Enable P. Active low. High when counting is enabled.
- ENT**: Enable T. Active low. High when counting is enabled.
- U/D**: Up/Down. Active low. High for Count Up, Low for Count Down.
- CLK**: Clock. Square wave signal.
- A, B, C, D**: Data inputs. High-Z when OE is high.
- QA, QB, QC, QD**: Data outputs. High-Z when OE is high.
- RCO**: Ripple Carry Out. Active low. High when the counter reaches 15 in Count Up mode or 0 in Count Down mode.
- CCO**: Carry/Count Out. Active low. High when the counter reaches 15 in Count Up mode or 0 in Count Down mode.

The diagram illustrates the counter's operation in three modes: Count Up, Count Down, and Inhibit Counting. The CCO signal indicates the current count value.

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SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS569A	–55°C to 125°C
SN74ALS568A, SN74ALS569A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT	
				MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage			2			2			V	
V _{IL}	Low-level input voltage			0.7			0.8			V	
I _{OH}	High-level output current	Q outputs		−1			−2.6			mA	
		$\overline{CCO}$ and $\overline{RCO}$		−0.4			−0.4				
I _{OL}	Low-level output current	Q outputs		12			24			mA	
		$\overline{CCO}$ and $\overline{RCO}$		4			8				
f _{clock}	Clock frequency	SN74ALS568A					0			MHz	
		ʹALS569A		0			22				
t _w	Pulse duration	$\overline{ACLR}$ or $\overline{LOAD}$ low		20			15			ns	
		SN74ALS568A	CLK high					25			
			CLK low					25			
		ʹALS569A	CLK high		20			16.5			
			CLK low		23			16.5			
t _{su}	Setup time before CLK↑	Data at A, B, C, D		25			20			ns	
		$\overline{ENP}$, $\overline{ENT}$	High		35			30			
			Low		25			20			
		$\overline{SCLR}$	Low		20			15			
			High (inactive)		35			30			
		$\overline{LOAD}$	Low		20			15			
			High (inactive)		35			30			
		U/ $\overline{D}$		35			30				
$\overline{ACLR}$ inactive		10			10						
t _h	Hold time after CLK↑ for any input			0			0			ns	
T _A	Operating free-air temperature			−55			125			°C	



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SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.5			−1.5			V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2			V _{CC} − 2			V
	Q outputs	V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4	3.3					
			I _{OH} = −2.6 mA				2.4	3.2		
V _{OL}	Q outputs	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25 0.4			V	
			I _{OL} = 24 mA	0.35 0.5						
	$\overline{\text{CCO}}$ and $\overline{\text{RCO}}$	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25 0.4				
			I _{OL} = 8 mA	0.35 0.5						
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		20			20			μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V		−20			−20			μA
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V		−0.2			−0.2			mA
I _O ‡	$\overline{\text{CCO}}$ and $\overline{\text{RCO}}$	V _{CC} = 5.5 V, V _O = 2.25 V		−15	−70	−15	−70	mA		
	Q outputs			−20	−112	−30	−112			
I _{CC}		V _{CC} = 5.5 V	Outputs high	16	26	16	26	mA		
			Outputs low	20	32	20	32			
			Outputs disabled	20	32	20	32			

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

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switching characteristics (see Figure 1)

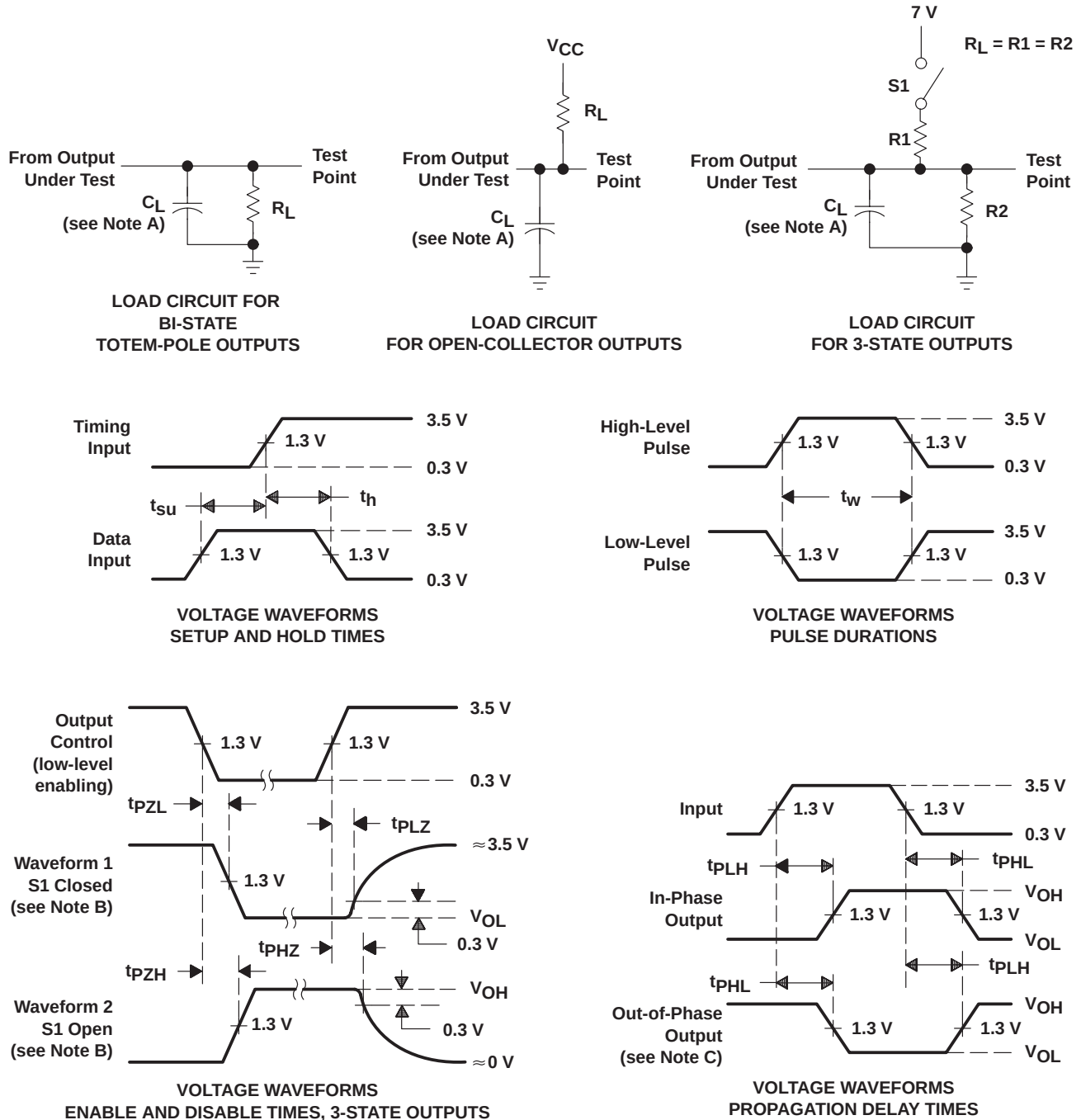
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS569A		SN74ALS568A SN74ALS569A		
			MIN	MAX	MIN	MAX	
f _{max}	SN74ALS568A				20		MHz
	'ALS569A		22		30		
t _{PLH}	CLK	Any Q	4	21	4	13	ns
t _{PHL}			7	19	7	16	
t _{PLH}	CLK	$\overline{RCO}$	12	37	12	28	ns
t _{PHL}			10	28	10	19	
t _{PLH}	CLK	$\overline{CCO}$	5	17	5	13	ns
t _{PHL}			6	30	6	25	
t _{PLH}	U/ $\overline{D}$	$\overline{RCO}$	9	31	9	23	ns
t _{PHL}			9	33	9	19	
t _{PLH}	$\overline{ENT}$	$\overline{RCO}$	6	21	6	15	ns
t _{PHL}			4	20	4	13	
t _{PLH}	$\overline{ENT}$	$\overline{CCO}$	5	18	5	13	ns
t _{PHL}			9	32	9	23	
t _{PLH}	$\overline{ENP}$	$\overline{CCO}$	4	18	4	12	ns
t _{PHL}			5	18	5	14	
t _{PHL}	$\overline{ACLR}$	Any Q	9	25	9	20	ns
t _{PZH}	$\overline{OE}$	Any Q	6	23	6	18	ns
t _{PZL}			6	29	6	24	
t _{PHZ}	$\overline{OE}$	Any Q	1	12	1	10	ns
t _{PLZ}			3	29	3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
83025022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
8302502RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	Purchase Samples
8302502SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	Purchase Samples
SN54ALS569AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN74ALS568AN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available
SN74ALS569ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS569ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS569ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS569AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS569ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SNJ54ALS569AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54ALS569AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54ALS569AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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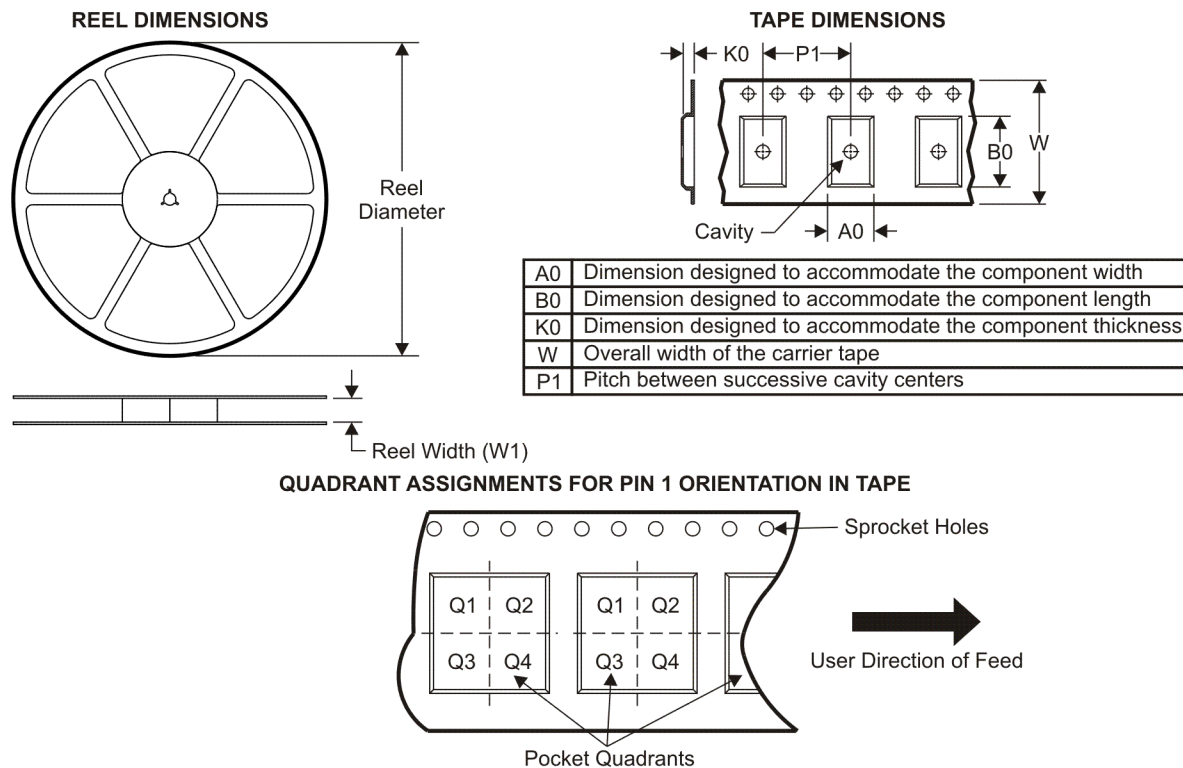
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS569A, SN74ALS569A :

- Catalog: [SN74ALS569A](#)
- Military: [SN54ALS569A](#)

NOTE: Qualified Version Definitions:

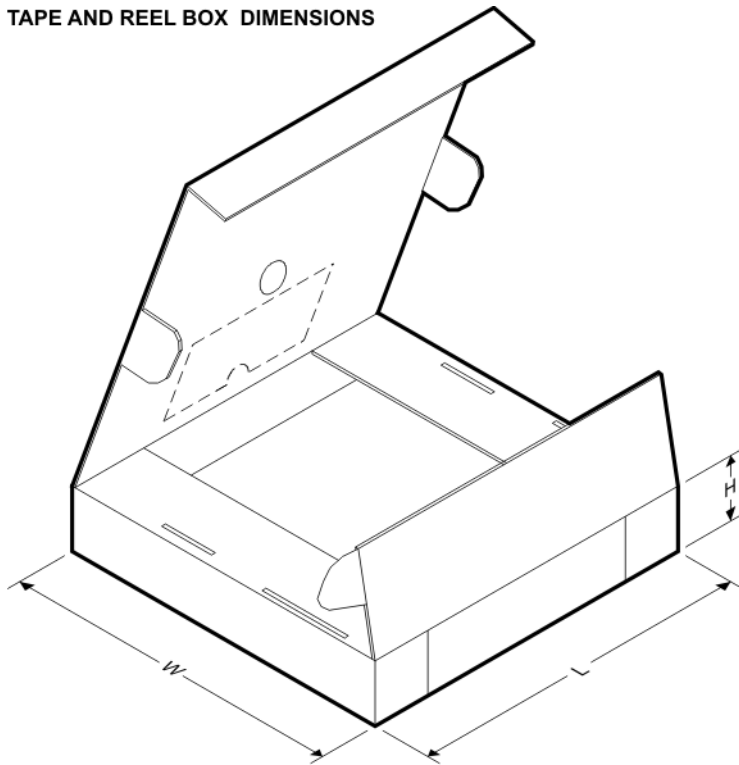
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS569ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



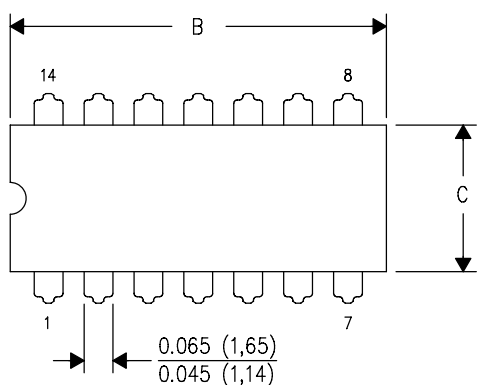
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS569ADWR	SOIC	DW	20	2000	346.0	346.0	41.0

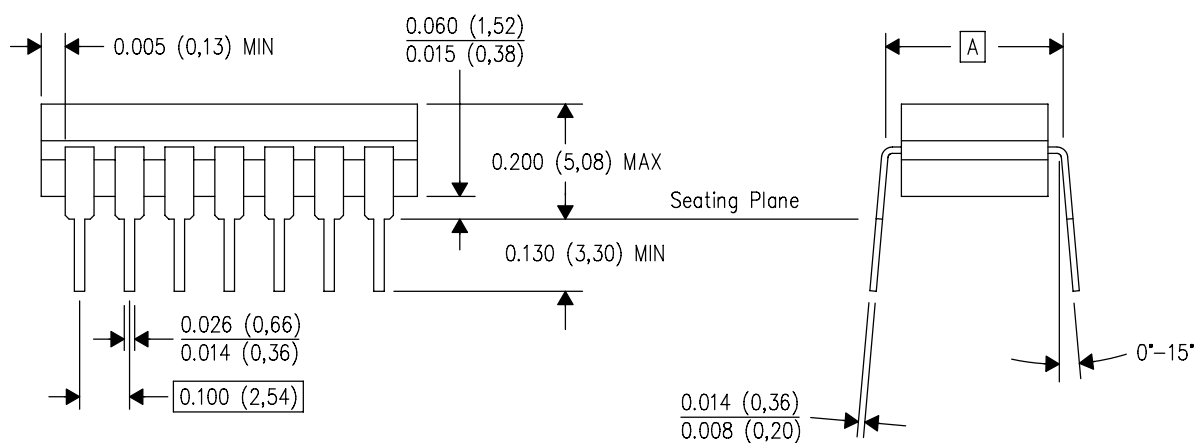
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

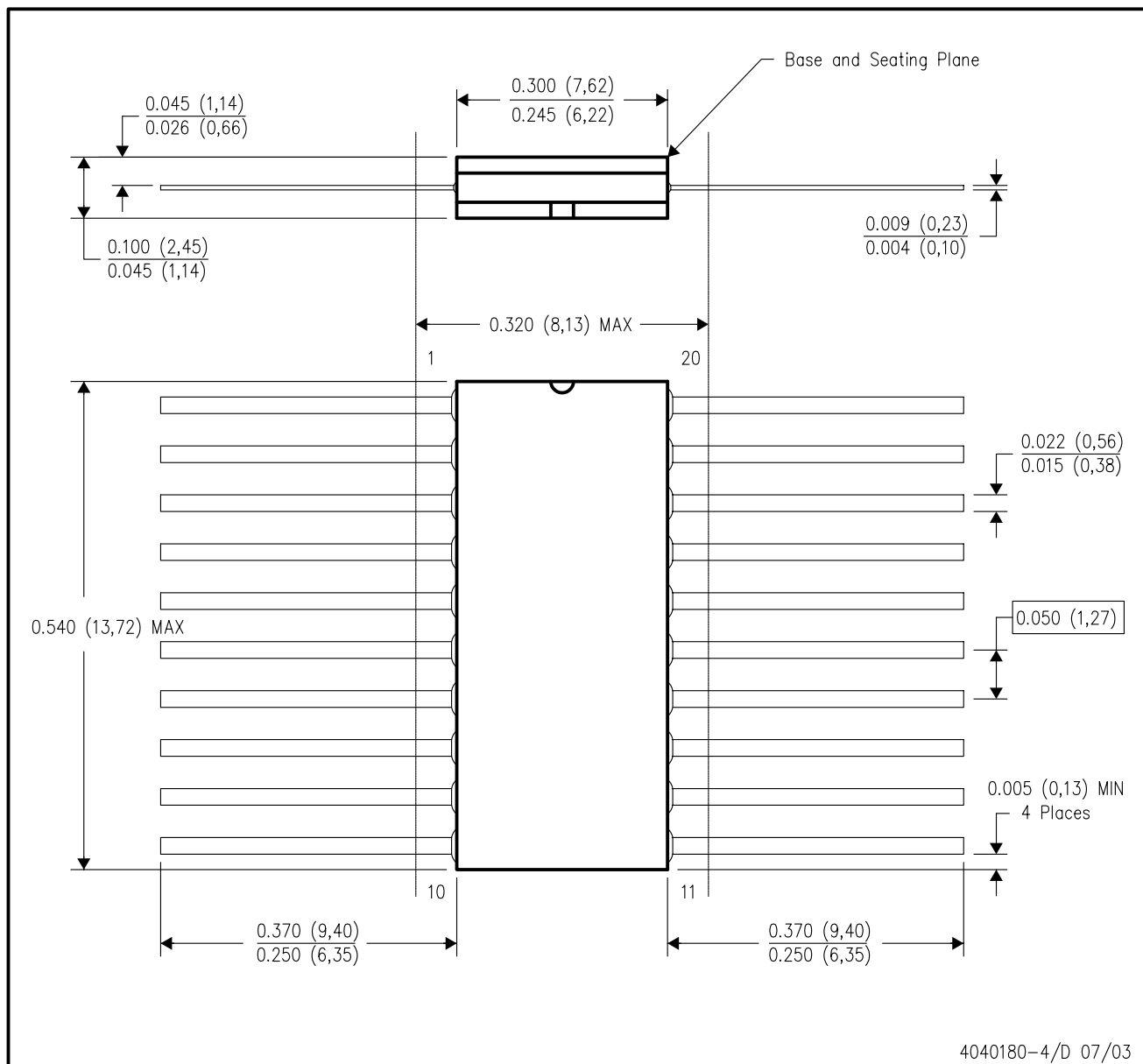


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

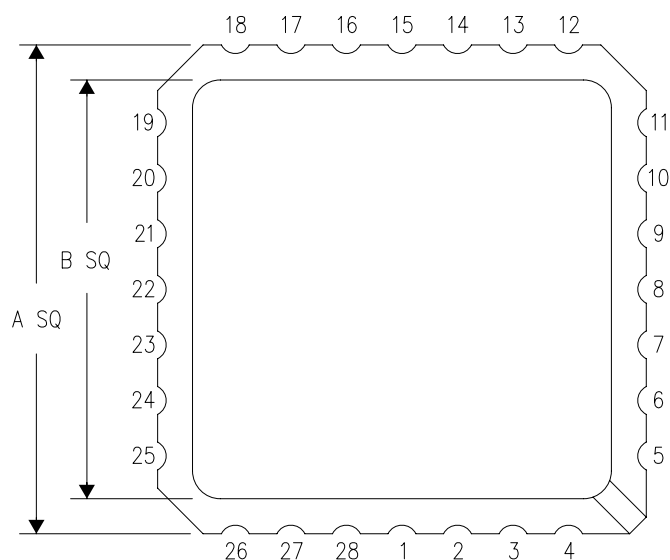


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

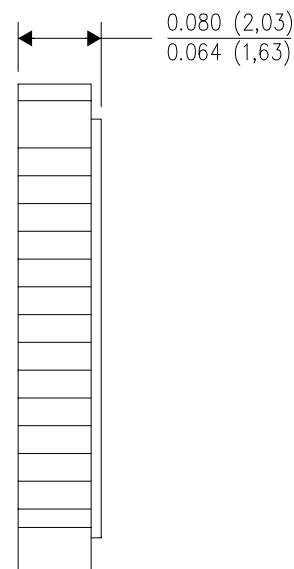
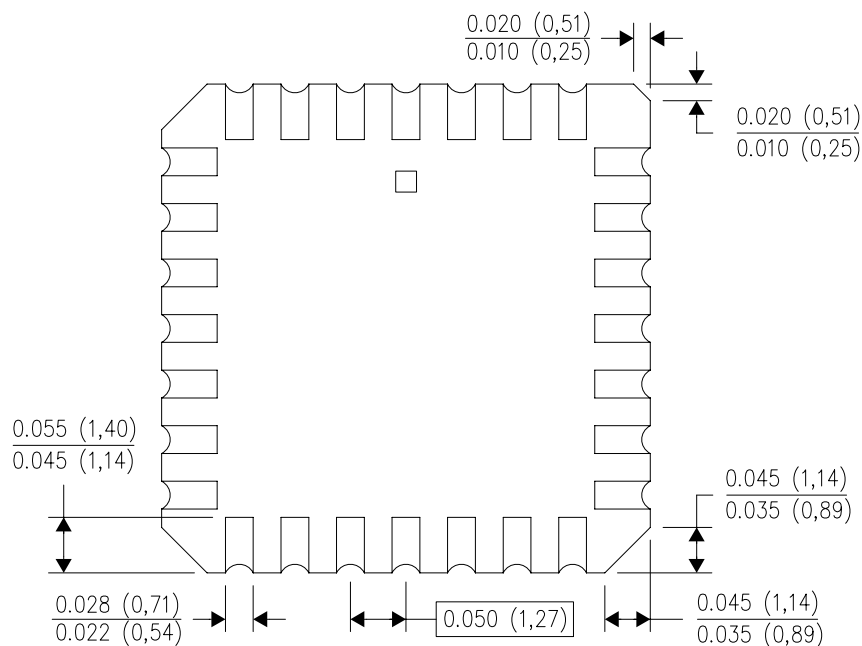
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



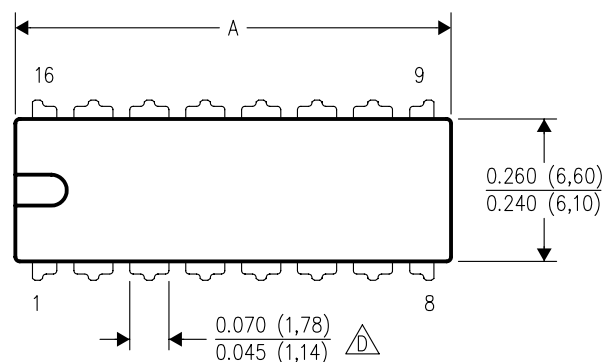
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

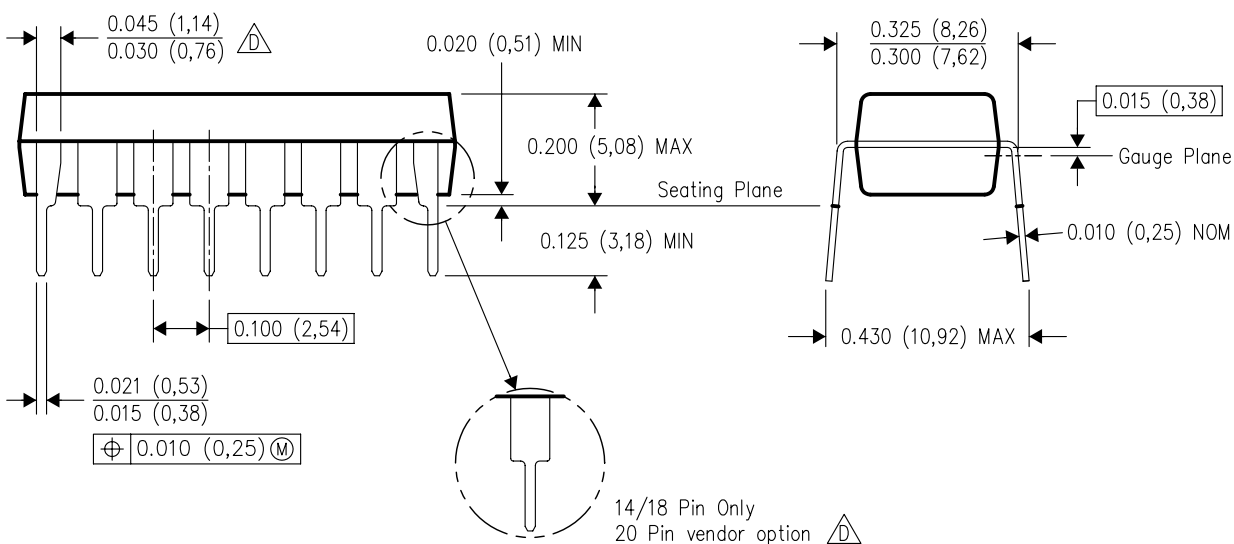
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



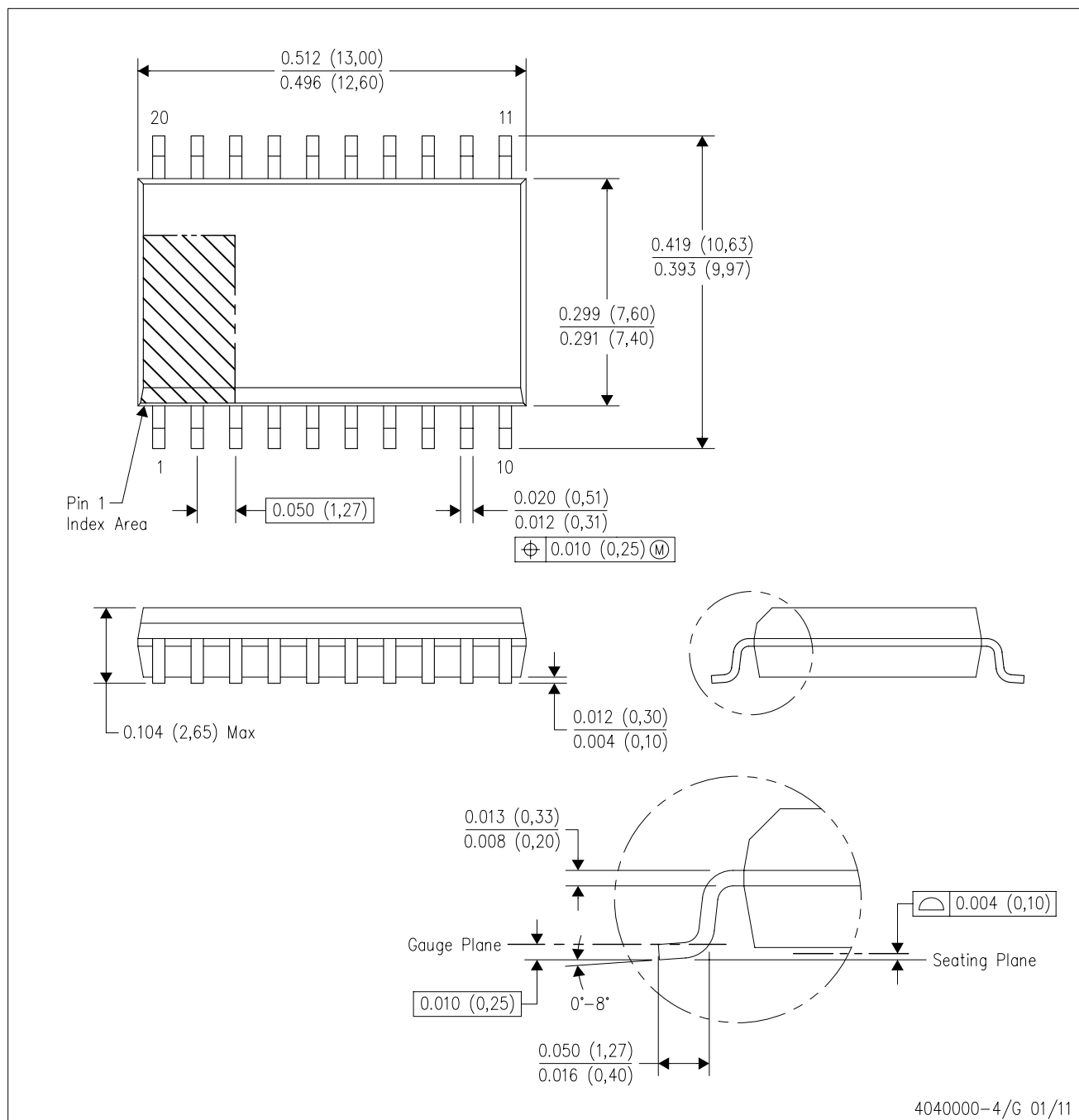
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

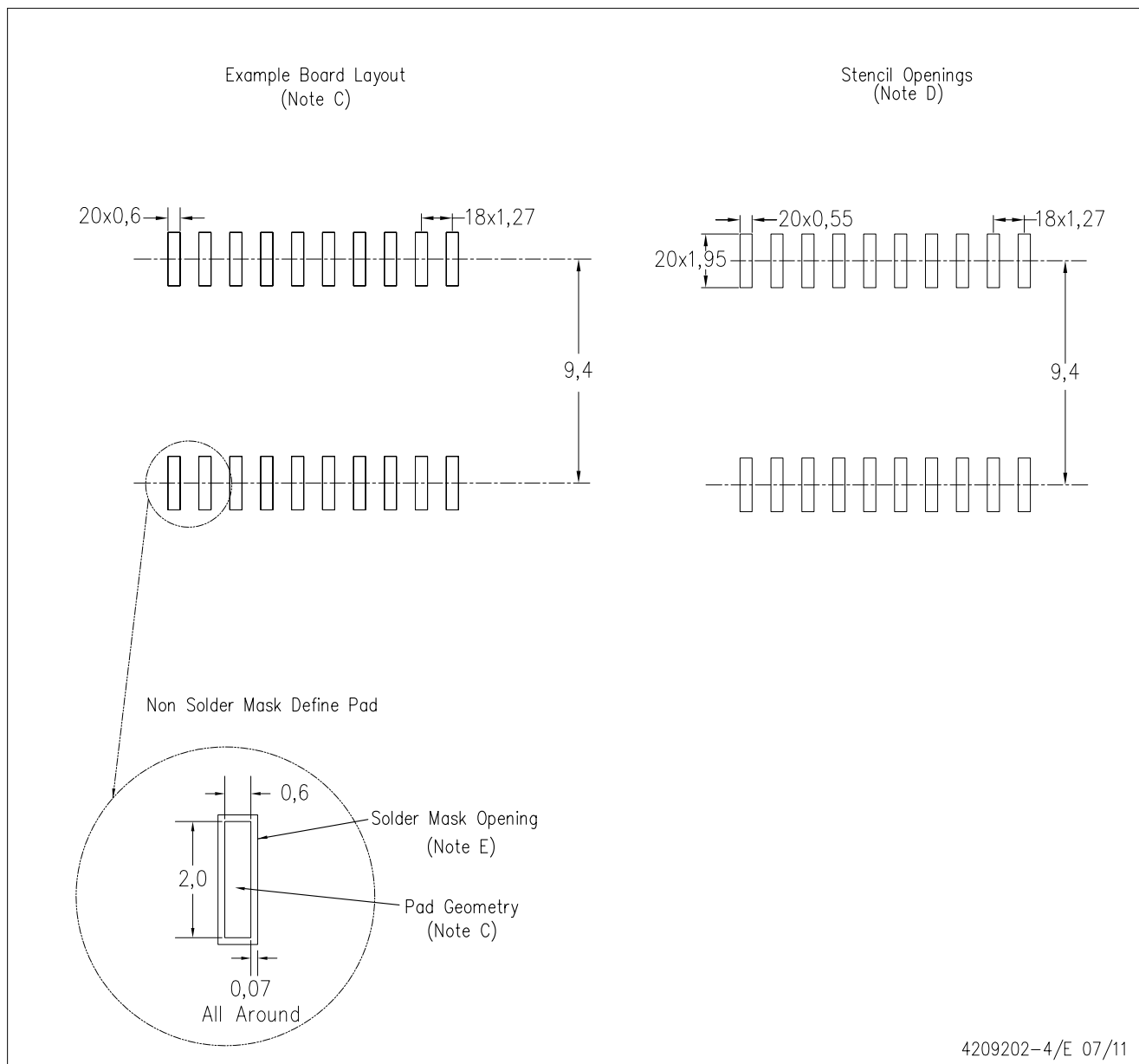
PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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