NiCd/NiMH Fast-Charge Management ICs

Features

General Description

 Fast charge of nickel cadmium or nickel-metal hydride batteries

- Direct LED output displays charge status
- ► Fast-charge termination by -∆V, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

Pin Connections



The bq2002E and bq2002G Fast-Charge ICs are low-cost CMOS battery-charge controllers providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002E/G to be the basis for a costeffective stand-alone or system-integrated charger. The bq2002E/G integrates fast charge with optional top-off and pulsed- trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits. Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage $(-\Delta V)$
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002E/G optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002E/G may also be placed in low-standby-power mode to reduce system power consumption.

The bq2002E differs from the bq2002G only in that a slightly different set of fast-charge and top-off time limits is available. All differences between the two ICs are illustrated in Table 1.

Pin Names

 TM
 Timer mode select input

 LED
 Charging status output

 BAT
 Battery voltage input

 V_{SS}
 System ground

TS	Temperature sense input
V _{CC}	Supply voltage input
INH	Charge inhibit input
CC	Charge control output

bq2002E/G Selection Guide

Part No.	LBAT	тсо	HTF	LTF	-∆V	PVD	Fast Charge	tмто	Top-Off	Maintenance
bq2002E	0.175 *	0.5 *	0.6 *	None		~	C/2	200	None	C/32
	VCC	V _{CC}	V _{CC}			~	1C	80	C/16	C/32
					~		2C	40	None	C/32
bq2002G	0.175 *	0.5 *	0.6 *	None		~	C/2	160	None	C/32
	VCC	V _{CC}	V _{CC}			~	1C	80	C/16	C/32
					~		2C	40	None	C/32

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Pin Descriptions

TM Timer mode input

CC

A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.

LED Charging output status

Open-drain output that indicates the charging status.

BAT Battery input voltage

The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} System ground

TS Temperature sense input

Input for an external battery temperature monitoring thermistor.

V_{CC} Supply voltage input

 $5.0V \pm 20\%$ power input.

INH Charge inhibit input

When high, INH suspends the fast charge in progress. When returned low, the IC re-

sumes operation at the point where initially suspended.

Charge control output

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002E/G.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{\text{RB1}}{\text{RB2}} = \text{N} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least $200k\Omega$ and less than $1 M\Omega$.



Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration



Figure 2. State Diagram



Figure 3. Block Diagram



Figure 4. Charge Cycle Phases

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and $V_{SS}.$ See Figure 1.

1. Application of power to $V_{CC}\, or$

2. Voltage at the BAT pin falling through the maximum cell voltage $V_{MCV} \mbox{ where }$

 $V_{MCV} = 2V \pm 5\%$.

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{LBAT} < V_{BAT} < V_{MCV}$, where

Corre- sponding Fast-Charge			Charg Top Time	Il Fast- je and -Off Limits utes)	Typical PVD and -∆V Hold-Off Time	Top Off	Pulse- Trickle	Pulse- Trickle Width	Maximum Synchro- nized Sampling Period (seconds)	
Rate	тм	Termination	bq2002E	bq2002G	(seconds)	Top-Off Rate	Rate	(ms)		
C/2	Mid	PVD	200	160	300	Disabled	C/32	73	18.7	
1C	Low	PVD	80	80	150	C/16	C/32	37	18.7	
2C	High	-ΔV	40	40	75	Disabled	C/32	18	9.4	

Table 1. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Notes: Typical conditions = 25° C, V_{CC} = 5.0V Mid = $0.5 * V_{CC} \pm 0.5$ V Tolerance on all timing is $\pm 12\%$.

$$V_{LBAT} = 0.175 \, * \, V_{CC} \, \pm 20\%$$

The valid temperature range is $V_{TS}\!>\!V_{HTF}$ where

 $V_{HTF} = 0.6 * V_{CC} \pm 5\%$.

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the next new charge cycle begins.

If $V_{MCV} < V_{BAT} < V_{PD}$ (see "Low-Power Mode") when a new battery is inserted, a delay of 0.35 to 0.9s is imposed before the new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage $(-\Delta V)$
- Maximum voltage
- Maximum temperature
- Maximum time

PVD and - ΔV Termination

There are two modes for voltage termination, depending on the state of TM. For $-\Delta V$ (TM = high), if V_{BAT} is lower than any previously measured value by 12mV ±3mV, fast charge is terminated. For PVD (TM = low or mid), a decrease of 2.5mV ±2.5mV terminates fast charge. The PVD and $-\Delta V$ tests are valid in the range $1V < V_{BAT} < 2V$.

Synchronized Voltage Sampling

Voltage sampling at the BAT pin for PVD and - ΔV termination may be synchronized to an external stimulus using the INH input. Low-high-low input pulses between 100ns and 3.5ms in width must be applied at the INH pin with a frequency greater than the "maximum synchronized sampling period" set by the state of the TM pin as shown in Table 1. Voltage is sampled on the falling edge of such pulses.

If the time between pulses is greater than the synchronizing period, voltage sampling "free-runs" at once every 17 seconds. A sample is taken by averaging together voltage measurements taken 57 μ s apart. The IC takes 32 measurements in PVD mode and 16 measurements in - Δ V mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources.

If the INH input remains high for more than 12ms, the voltage sample history kept by the IC and used for PVD and $-\Delta V$ termination decisions is erased and a new history is started. Such a reset is required when transitioning from free-running to synchronized voltage sampling.

The response of the IC to pulses less than 100ns in width or between 3.5ms and 12ms is indeterminate. Tolerance on all timing is $\pm 12\%$.

Voltage Termination Hold-off

V,

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and $-\Delta V$ terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage, V_{MCV} , fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO} where

$$TCO = 0.5 * VCC \pm 5\%$$

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/2 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge before reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 73ms active for every 1097ms inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active once every 1.17s for the period specified in Table 1. This results in a trickle rate of C/32.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle

rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The midlevel selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2\pm0.5V$. See Figure 4.

Charge Status Indication

<u>A fast charge in progress is uniquely indicated when the LED pin goes low. The LED pin is driven to the high-Z state for all conditions other than fast charge. Figure 2 outlines the state of the LED pin during charge.</u>

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{\text{LED}}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002E/G continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold $\left(V_{PD}\right)$ where

$V_{PD} = V_{CC} - (1V \pm 0.5V)$

Both the CC pin and the $\overline{\text{LED}}$ pin are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When V_{BAT} returns to a value below V_{PD} , the IC pulse-trickle charges until the next new charge cycle begins.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V _{CC}	V _{CC} relative to V _{SS}	-0.3	+7.0	v	
VT	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	v	
T _{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T _{STG}	Storage temperature	-40	+85	°C	
T _{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T _{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (TA = 0 to 70°C; V_{CC} \pm 20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V _{TCO}	Temperature cutoff	0.5 * V _{CC}	±5%	v	$V_{TS} \le V_{TCO}$ inhibits/terminates fast charge and top-off
V _{HTF}	High temperature fault	0.6 * VCC	±5%	v	V _{TS} < V _{HTF} inhibits fast charge start
V _{MCV}	Maximum cell voltage	2	±5%	v	$V_{BAT} \ge V_{MCV}$ inhibits/terminates fast charge and top-off
V _{LBAT}	Minimum cell voltage	0.175 * V _{CC}	±20%	v	V_{BAT} < V_{LBAT} inhibits fast charge start
-ΔV	BAT input change for -ΔV detection	-12	±3	mV	
PVD	BAT input change for PVD detection	-2.5	±2.5	mV	

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V _{CC}	Supply voltage	4.0	5.0	6.0	v	
V _{DET}	$-\Delta V$, PVD detect voltage	1	-	2	v	
VBAT	Battery input	0	-	V _{CC}	v	
V _{TS}	Thermistor input	0.5	-	V _{CC}	v	$V_{TS} < 0.5V$ prohibited
V _{IH}	Logic input high	0.5	-	-	v	INH
	Logic input high	V _{CC} - 0.5	-	-	v	ТМ
V _{IM}	Logic input mid	$\frac{V_{CC}}{2} - 0.5$	-	$\frac{\mathrm{V}_{\mathrm{CC}}}{2} + 0.5$	v	TM
VIL	Logic input low	-	-	0.1	v	INH
	Logic input low	-	-	0.5	v	ТМ
VOL	Logic output low	-	-	0.8	v	$\overline{\text{LED}}$, CC, $I_{OL} = 10\text{mA}$
V _{PD}	Power down	V _{CC} - 1.5	-	V _{CC} - 0.5	V	V _{BAT} ≥ V _{PD} max. powers down bq2002E/G; V _{BAT} < V _{PD} min. = normal operation.
I _{CC}	Supply current	-	-	500	μA	Outputs unloaded, $V_{CC} = 5.1V$
I _{SB}	Standby current	-	-	1	μΑ	$V_{CC} = 5.1 \text{V}, V_{BAT} = V_{PD}$
IOL	LED, CC sink	10	-	-	mA	$@V_{OL} = V_{SS} + 0.8V$
I_L	Input leakage	-	-	±1	μΑ	INH, CC, $V = V_{SS}$ to V_{CC}
I _{OZ}	Output leakage in high-Z state	-5	-	-	μΑ	IED, CC

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R _{BAT}	Battery input impedance	50	-	-	ΜΩ
R _{TS}	TS input impedance	50	-	-	ΜΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d _{FCV}	Time base variation	-12	-	12	%	
t _{DLY}	Start-up delay	0.35	-	0.9	s	Starting from $V_{MCV} < V_{BAT} < V_{PD}$

Note: Typical is at $T_A = 25^{\circ}C$, $V_{CC} = 5.0V$.

8-Pin DIP (PN)





	Inc	hes	Millim	neters
Dimension	Min.	Max.	Min.	Max.
А	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
В	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
С	0.008	0.013	0.20	0.33
D	0.350	0.380	8.89	9.65
Е	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

8-Pin PN (0.300" DIP)

8-Pin SOIC Narrow (SN)





8-Pin SN (0.150" SOIC)

-		-				
	Inc	hes	Millimeters			
Dimension	Min.	Max.	Min.	Max. 2 1.78 0 0.25 3 0.51 8 0.25 0 5.08 1 4.06 4 1.40 2 6.22		
А	0.060	0.070	1.52	1.78		
A1	0.004	0.010	0.10	0.25		
В	0.013	0.020	0.33	0.51		
С	0.007	0.010	0.18	0.25		
D	0.185	0.200	4.70	5.08		
Е	0.150	0.160	3.81	4.06		
e	0.045	0.055	1.14	1.40		
Н	0.225	0.245	5.72	6.22		
L	0.015	0.035	0.38	0.89		

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
BQ2002EPN	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
BQ2002EPNE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
BQ2002ESN	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002ESNG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002ESNTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002ESNTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002GPN	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
BQ2002GPNE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
BQ2002GSN	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002GSNG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002GSNTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ2002GSNTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

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⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2002ESNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
BQ2002GSNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

19-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2002ESNTR	SOIC	D	8	2500	340.5	338.1	20.6
BQ2002GSNTR	SOIC	D	8	2500	340.5	338.1	20.6

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