PowerLAN™ Dual-Cell Li-Ion Battery Monitor With PowerPump™ Cell Balancing

FEATURES

- **Monitors up to Two Individual Cell Voltages and Temperatures**
- **Part of a Complete Low-Cost Solution for Battery Packs of up to 12 Series and One or More Parallel Cells (When Used With bq78PL114).**
- **Advanced PowerPump™ Balancing Technology Equalizes Cells in Li-Ion Battery Packs, Resulting in Longer Run Time and Cell Life.**
- **PowerPump™ Cell Balancing Transfers Charge From Cell to Cell During all Operating Conditions – No Wasteful Current Bleeding or Associated Heat Buildup.**
- **Unique PowerLAN™ Isolated Communications Technology Permits Simultaneous Measurement of All Individual Cell Voltages in a Series String.**
- **Low Current Consumption:**
  - **<250 μA Active**
  - **<35 μA Standby**
  - **<1 μA Undervoltage Shutdown**
- **Connects Directly to Cells, No Resistive Dividers**
- **Internal LDO Regulator for Support Circuitry**
- **Ultrasmall Footprint, 3-mm × 3-mm**
- **Millivolt Measurement Resolution Using Delta-Sigma A/D Converter**
- **Self-Calibrating Time Base – No Crystal Required When Used With bq78PL114**

APPLICATIONS

- **Uninterruptible Power Supplies (UPS)**
- **Portable Medical and Test Equipment**
- **Electric Bikes and Mild-EV Battery Packs**
- **Multicell Series Strings ≥ 5S**

RELATED DEVICES

- **bq78PL114 Master Gateway Battery Controller**

DESCRIPTION

The bq76PL102 PowerLAN dual-cell battery monitor is part of a complete scalable battery management system for use with arrays of up to 12 Li-Ion rechargeable cells. The bq76PL102 connects to one or two cells in a series string, performs voltage and temperature monitoring of each individual cell, and reports these parameters over the PowerLAN communication network. Together with a bq78PL114 master-gateway battery controller, the bq76PL102 forms a complete battery monitoring and management system for higher cell-count applications.

Partitioning of the battery monitor function on a per cell basis permits connection and measurement close to the cell. This results in superior accuracy and management over competing solutions. This scheme also facilitates the PowerPump cell balancing system, a technique which actively balances capacities of Li-Ion batteries without the excessive heat or limitations of bleed-balancing techniques.

The bq76PL102 PowerPump cell balancing technology uses a charge-transfer methodology which does not bleed off excess energy as heat, but instead moves energy dynamically from cell to cell as needed. Balancing is performed during all battery operational modes – charge, discharge, and rest. Balancing is automatically coordinated between all cells on a PowerLAN system. PowerPump balancing technology results in longer run time and longer cell life.

The PowerLAN communications architecture has been engineered to provide robust communications in tough EMI/RFI environments while avoiding the excessive power draw, high parts count, and elevated cost of other solutions. PowerLAN permits easy scalability using series connections of bq76PL102 dual-cell battery monitors. High-cell-count battery systems of up to 12 series cells are easily constructed without complicated high-voltage cell measurement restrictions.

The bq76PL102 works with the bq78PL114 master-gateway battery controller.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

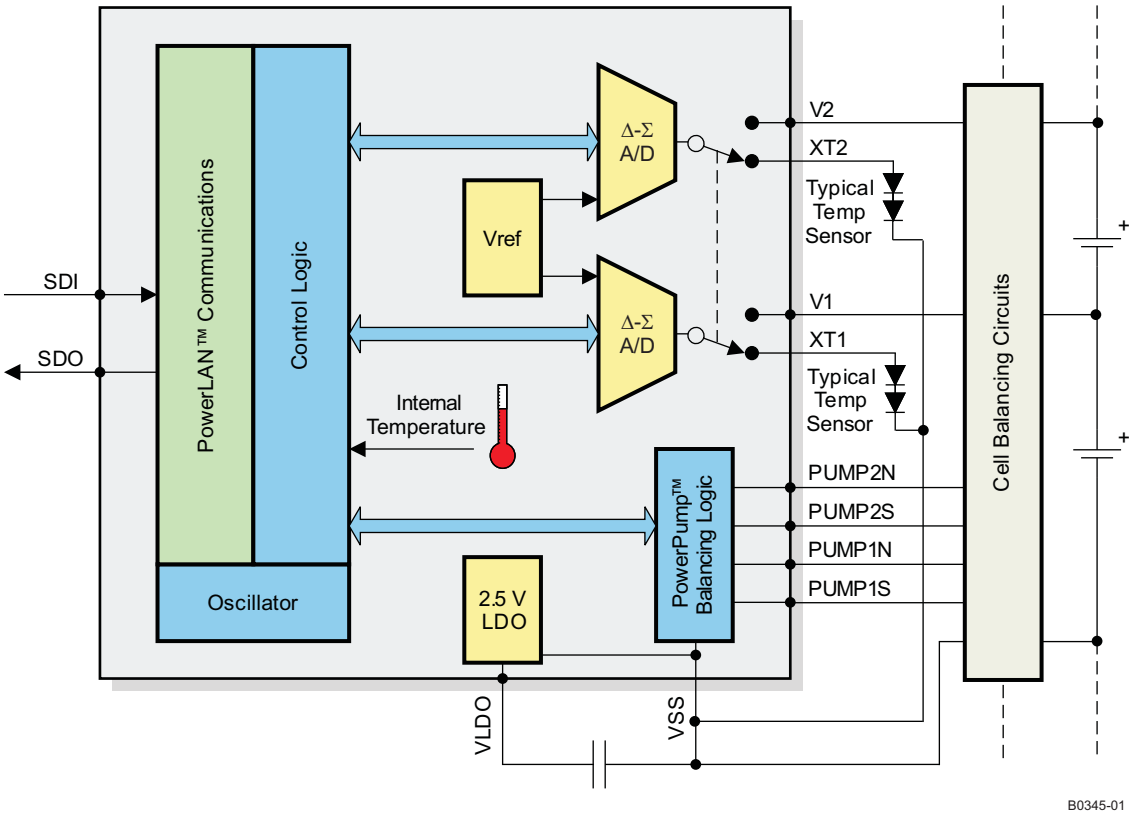


Figure 1. bq76PL102 Simplified Internal Block Diagram

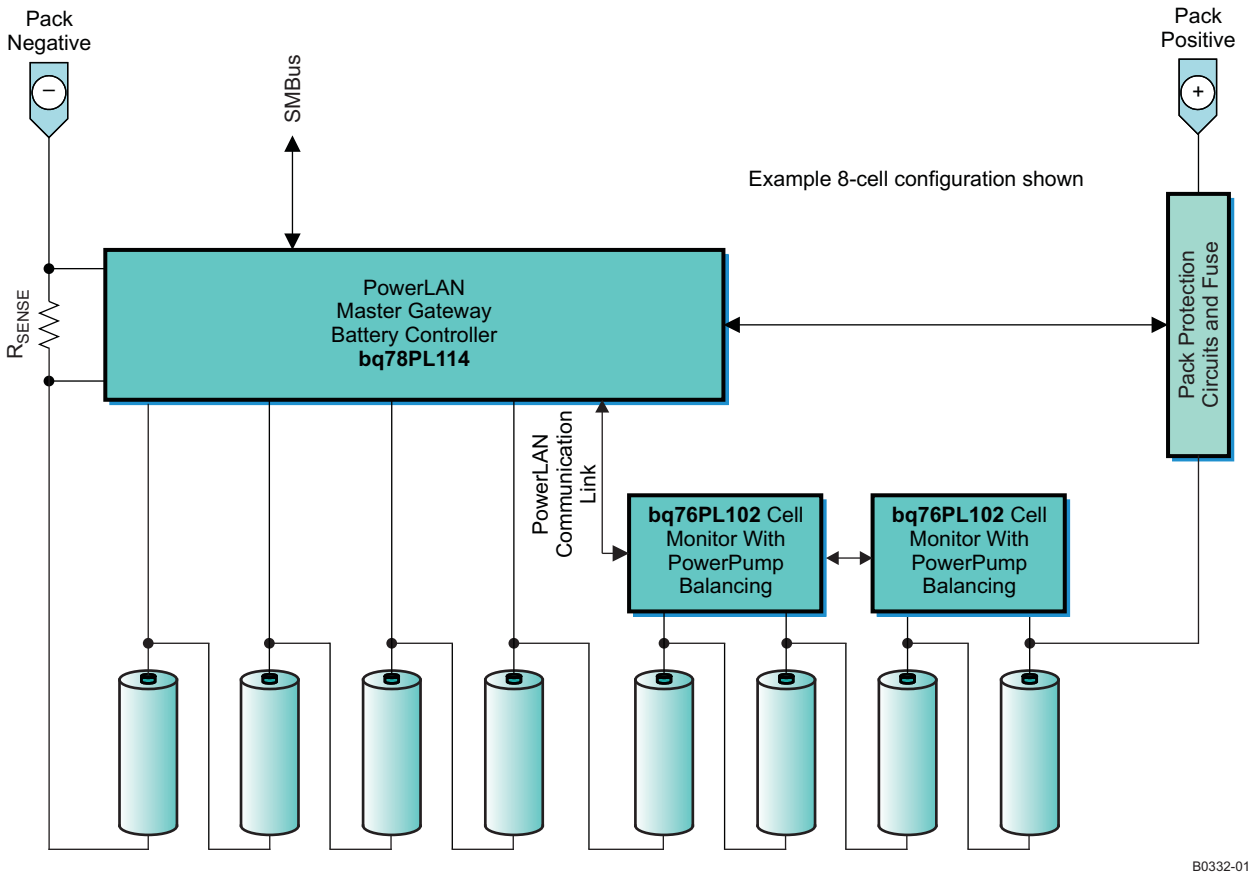


Figure 2. Example Multicell PowerLAN System Implementation

AVAILABLE OPTIONS

The bq76PL102 is currently available in a 3-mm square QFN-16 package, bq76PL102RGT, with a rated operational temperature range of –40°C to 85°C. (See Figure 5 for specific package information, dimensions, and tolerances.)

- Order bq76PL102RGTT for 250 quantity, tape and reel
- Order bq76PL102RGTR for 3000 quantity, tape and reel

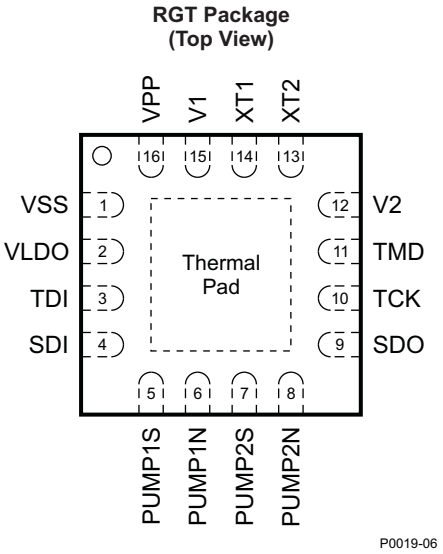


Figure 3. bq76PL102 Pinout (Top View)

CAUTION:

This device is subject to damage from Electrostatic Discharge (ESD). The device should be stored and handled using appropriate ESD precautions to prevent damage to the internal circuitry.

PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION(2)
NAME	NO.		
PUMP1N	6	O	Charge-balance gate drive for cell 1 north
PUMP1S	5	O	Charge-balance gate drive for cell 1 south
PUMP2N	8	O	Charge-balance gate drive cell 2 north
PUMP2S	7	O	Charge-balance gate drive cell 2 south
SDI	4	I	PowerLAN serial data input from lower south, downstream part
SDO	9	O	PowerLAN serial data output to north, upstream part
XT1	14	IA	External temperature sensor 1 input (calibrated 50 µA)
XT2	13	IA	External temperature sensor 2 input (calibrated 50 µA)
TCK	10	NC	Do not connect
TDI	3	NC	Do not connect
TMD	11	NC	Do not connect
V1	15	IA	Midpoint cell connection (cell 1 positive and cell 2 negative)
V2	12	P, IA	Connect to most-positive cell voltage (cell 2 positive)(3)
VLDO	2	P	Low-dropout regulator output – connect to VPP (bypass with 4.7 µF capacitor)
VPP	16	P	Connect to VLDO
VSS	1	P	Connect to most-negative cell voltage (cell 1 negative)
	—	P	Thermal pad – connect to VSS

(1) I - input, IA - analog input, O - output, P - power, NC - no connect
(2) Cell numbering convention is from more-negative (cell 1) to more-positive (cell 2) and is locally referenced.
(3) When there is an odd number of series cells in a battery pack, connect pin V2 of the topmost bq76PL102 to pin V1 of the same bq76PL102.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
T_A	Operating free-air temperature (ambient)	–40 to 85	°C
T_{stg}	Storage temperature	–65 to 150	°C
Voltage on SDO	Note: not VSS-referenced	(V1 – 0.5) to (V2 + 0.5)(2)	V
Voltage on SDI	Limited by lower cell voltage	(VSS – 0.5) to (V1 + 0.5)(2)	V
Voltage on V1 (V1 – VSS)(2)	Maximum cell voltage	–0.5 to 5	V
Voltage on V2 (V2 – V1) (2)	Maximum cell voltage (not VSS-referenced)	–0.5 to 5	V
Voltage on XT1 or XT2	With respect to VSS	(VSS – 0.5) to (V1 + 0.5)	V
ESD tolerance	JEDEC, JESD22-A114 human-body model, R = 1500 Ω, C = 100 pF	2	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is note implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Cell numbering convention is from most negative (Cell 1) to most positive (Cell 2) and is locally referenced.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{CELL} (1)(2)	Cell voltage input	Two-cell configuration	2.5	3.6	4.5	V
		One-cell configuration(2)	2.8	3.6	4.5	
I_{DD}	Operating current (cell 2)	Measuring, reporting, or balancing		250	350	µA
I_{STBY}	Standby-mode current (cell 2)	Idle		32	50	µA
I_{SHIP}	Ship-mode current (cell 2)			10	30	µA
I_{UVM}(3)	Cell extreme undervoltage-mode current (cell 2)	V1 < 2.8 V		0.5	1	µA
$V_{Startup}$	Minimum startup voltage, V1 and V2		2.9			V
CELL VOLTAGE MEASUREMENT CHARACTERISTICS						
	V1 measurement range		2.75		4.5	V
	V2 measurement range		2.75		4.5	V
	Analog resolution			<1		mV
	Accuracy (after calibration)	25°C		±3	±7	mV
		0°C to 85°C		±10(4)		
	Measurement temperature coefficient			+150		µV/°C
	Conversion time(5)				80	ms
INTERNAL TEMPERATURE MEASUREMENT CHARACTERISTICS						
	Measurement range		–30		85	°C
	Resolution			0.1		°C
	Accuracy (after calibration)(4)	0°C to 85°C			±2	°C
	Temperature coefficient			+1.28		mV/°C

(1) For single-cell operation, V1 must be connected to V2.
(2) During operation after power up
(3) Condition forced by bq78PL114
(4) With respect to voltage shift induced by temperature coefficient at 85C.
(5) Does not include delay due to internode timing delays.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL TEMPERATURE SENSOR(S) TYPICAL CHARACTERISTICS(6)						
	Measurement range(7)		–40		90	°C
	Resolution			0.2		°C
	Accuracy(8)	25°C			±2	°C
		0°C to 85°C			±2	°C
PowerPump ELECTRICAL CHARACTERISTICS (FOR bq76PL102)(9)						
V_{OH}	High drive, PUMP1S, PUMP2S	I_{OUT} = 10 µA	0.9 V1			V
V_{OL}	Low drive, PUMP1S, PUMP2S	I_{OUT} = –200 µA			0.1 V1	V
V_{OH}	High drive, PUMP1N, PUMP2N	I_{OUT} = 200 µA	0.9 V1			V
V_{OL}	Low drive, PUMP1N, PUMP2N	I_{OUT} = –10 µA			0.1 V1	V
I_{OH}	Source current, PUMP1S, PUMP2S	V_{OH} = V1 – 0.8 V	250			µA
I_{OL}	Sink current, PUMP1N, PUMP2N	V_{OH} = V1 + 0.2 V	–250			µA
t_r	Signal rise time	C_{Load} = 300 pF			100	ns
t_f	Signal FET fall time	C_{Load} = 300 pF			100	ns
f_P	Frequency			204.8		kHz
	PWM duty cycle(10)	PUMP1S, PUMP2S		67%		
		PUMP1N, PUMP2N		33%		
LDO VOLTAGE CHARACTERISTICS(11)						
V_{LDO}	Single-cell operation, referenced to VSS	Load = 200 µA at 25°C, V1 = 2.8 V	2.425	2.5	2.575	V
V_{LDO}	Dual-cell operation, V1 = V2 = cell voltage	Load = 2 mA at 25°C	2.425	2.5	2.575	V
V_{LAN} SIGNALS(12)(13)(14)						
C_L	Load capacitance	SDI, C coupling = 1000 pf			100	pF
		SDO			100	
V_{IH}	Input logic high	SDI	0.8 V_{LDO}			V
V_{OH}	Output logic high	SDO	0.9 V_{LDO}			V
V_{IL}	Input logic low	SDI			0.2 V_{LDO}	V
V_{OL}	Output logic low	SDO			0.1 V_{LDO}	V
t_r	Input rise time	SDI			500	ns
t_f	Input fall time	SDI			500	ns
t_{or}	Output rise time	SDO		30	50	ns
t_{of}	Output fall time	SDO		30	50	ns

(6) Typical for dual-diode (MMBD4148 or equivalent) external sensor using recommended circuit
(7) Range of diode sensors may exceed operation limits of IC and battery cells.
(8) Typical behavior after calibration; final result depends on specific component characteristics
(9) All parameters tested at typical cell voltages = 3.6 V.
(10) The frequency and duty cycle of each pump gate drive signal is set by the bq78PL114. The PUMPxN signals have a positive duty cycle and switch on the N-Channel MOSFETs. The duty cycle of the PUMPxS signals is (100 – the duty cycle of the PUMPxN signals).
(11) After calibration
(12) Values specified by design
(13) The SDI and SDO pins on the bq76PL102 are ac-coupled from the cell circuits downstream and upstream, respectively. The limits specified here are the voltage transitions which must occur within the SDI and SDO rise- and fall-time specifications.
(14) The value specified is over the full input voltage range and the maximum load capacitance.

FEATURE SET

The bq76PL102 dual-cell li-ion battery monitor with PowerPump balancing implements battery voltage measurement, temperature measurement, and balancing for one or two Li-Ion cells in series, and any number in parallel (limited by other design considerations).

Functions include:

- Two external temperature sensors are supported
- Simultaneous, synchronous measurement of all cell voltages in a series string
- Asynchronous reporting of most-recent measurements for each cell
- Fully independent measurements on a cell-by-cell basis
- PowerPump cell balancing using charge transfer from cell to cell
- PowerLAN isolated communications to other bq76PL102 devices or bq78PL114 master-gateway battery-management controller
- Low-power operation

OPERATION

Cell-Voltage Measurement

Voltage measurements are made using one-per-cell precision delta-sigma analog-to-digital converters (ADC). An internal calibrated band-gap voltage reference is provided with each part. Measurements are performed when commanded by the bq78PL114 master-gateway battery-management controller via the one-wire PowerLAN serial communications bus. This allows all cells to be measured at exactly the same time under the same load conditions.

Cell-Temperature Measurement

Temperature measurements can be obtained using one internal and up to two external sensors. Each external sensor consists of one (or two for increased accuracy) series-connected diodes and a capacitor for filtering. The use of dual diodes in a single SMT package is recommended (MMBD4148SE or equivalent). The diode can be located up to 6 inches (15 cm) from the circuit board. The RF filter capacitor should be co-located very close to the diode to minimize unwanted noise coupling.

The temperature measurement subsystem uses the same dual ADCs that are used for measuring voltages. Temperature measurements are fully independent of voltage readings, and are ordinarily interleaved at a fractional rate of the voltage readings by commands from the bq78PL114 master-gateway battery-management controller.

Cell Balancing

Balancing is provided among any number of supported cells. The bq76PL102 and PowerLAN family of master-gateway battery controllers is optimized for designs using more than four cells in series.

The patented PowerPump reactive cell balancing dramatically increases the useful life of battery systems by eliminating the cycle life fade of multicell batteries due to cell imbalance. PowerPump efficiently transfers charge from cell to cell, rather than simply bleeding off charging energy as heat. Charge is moved from higher-capacity cells to lower-capacity ones, and can be moved as needed between any number of series cell elements. Balancing is performed during all battery operational modes – charge, discharge, and rest. Compared to resistive bleed balancing, virtually no energy is lost as heat. The actual balance current is externally scalable with component selection and can range from 10 mA to 1 A (100 mA typical) depending on application or cell requirements. (See the reference schematic, Figure 7.)

Algorithms for cell balancing are centrally coordinated by the bq78PL114 PowerLAN master-gateway battery-management controller and directed across the array of bq76PL102 dual-cell Li-Ion battery monitors. Balancing is done in both directions by the bq76PL102s within the cell stack array: *north* or up the cell stack and *south* or down the cell stack. Each bq76PL102 node provides the circuitry to transfer (pump) the charge from cell to cell to provide balancing. The balancing algorithm is implemented in the bq78PL114 master-gateway battery controller, and commands are communicated to the bq76PL102s via the PowerLAN communications link. By tracking the balancing required by individual cells, overall battery safety is enhanced – often allowing early detection of internal micro-shorts or other cell failures.

Cell balancing *pumping*, or charge transfer from one cell to another, is accomplished using a circuit that forms a simple flyback converter under control of the bq76PL102, which is in turn controlled by the master gateway. The outputs of PUMP*nd (cell number, direction)* control MOSFET transistors which charge an inductor from one cell and then discharge the inductor into an adjacent cell through the intrinsic body diode of the other MOSFET.

- **PUMP1S**: Pumps charge from cell 1 to the next lower cell (closer to battery negative). This signal is unused by the first or lowest cell in the string.
- **PUMP1N:** Pumps charge from cell 1 to cell 2.
- **PUMP2S:** Pumps charge from cell 2 to cell 1
- **PUMP2N:** Pumps charge from cell 2 to the next higher cell in a pack (closer to battery positive). This signal is unused by the highest cell in the string.

PowerLAN Communications

PowerLAN communications technology is a patented serial network and protocol designed specifically for battery management in a multicell environment. PowerLAN is used to initiate and report measurements of cell voltage and temperature, as well as control cell balancing. Using only a capacitor, PowerLAN isolates voltages from adjacent bq76PL102 parts to permit high-voltage stack assemblies without compromising precision and accuracy. PowerLAN is expandable to support up to 12 cells in series, with each bq76PL102 handling two series cells. PowerLAN provides high ESD standoff and high immunity to noise generated by nearby digital circuitry or switching currents. Each bq76PL102 has both a PowerLAN serial input and serial output pin. Received data is buffered and retransmitted, permitting high numbers of nodes without loss of signal fidelity. Signals are capacitor-coupled between nodes to provide high dc isolation.

Operation Modes

The bq76PL102 normally operates in one of two modes: active or standby. The bq76PL102 is normally in standby mode and consumes typically less than 50 μA. The low-dropout regulator output is still functional in this mode, as are internal system protection functions (undervoltage, communications timeout, etc.)

When a PowerLAN communications event occurs, then the bq76PL102 transitions to active mode and current drain increases to 250 μA typically. The bq76PL102 stays in this mode to complete any measurements or cell-balancing pumping operations. Once activity in this mode ceases, the return to standby is automatic, thus reducing overall power consumption.

An undervoltage ultralow-current mode is also available when initiated by the bq78PL114 master-gateway battery controller and when the cell voltages drop below a preset threshold. This mode is used to preserve battery capacity during long periods of non-use and therefore has a current drain of approximately 1 μA.

Note that cell balancing currents are external to the bq76PL102 and may be sized according to the needs of the application (typically 10 mA to 1 A). These currents are fixed by the cell-balancing circuitry and only enabled or disabled by the bq76PL102 (under control of the bq78PL114) to achieve the necessary cell-balance operations.

COMPLEMENTARY PRODUCTS

PowerLAN Master Gateway Battery Controller

The bq78PL114 master-gateway battery-management controller with PowerPump cell balancing from Texas Instruments is the central controller for a complete multicell battery system.

This advanced master-gateway battery controller works with up to 12 series cells monitored by bq76PL102 cell monitors to provide battery voltage, temperature, current and safety monitoring; state-of-charge and state-of-health information; system-wide internal PowerLAN communications; as well as external communications of battery parameters via the industry-standard SMBus interface.

PowerLAN Six-Cell Battery Monitor

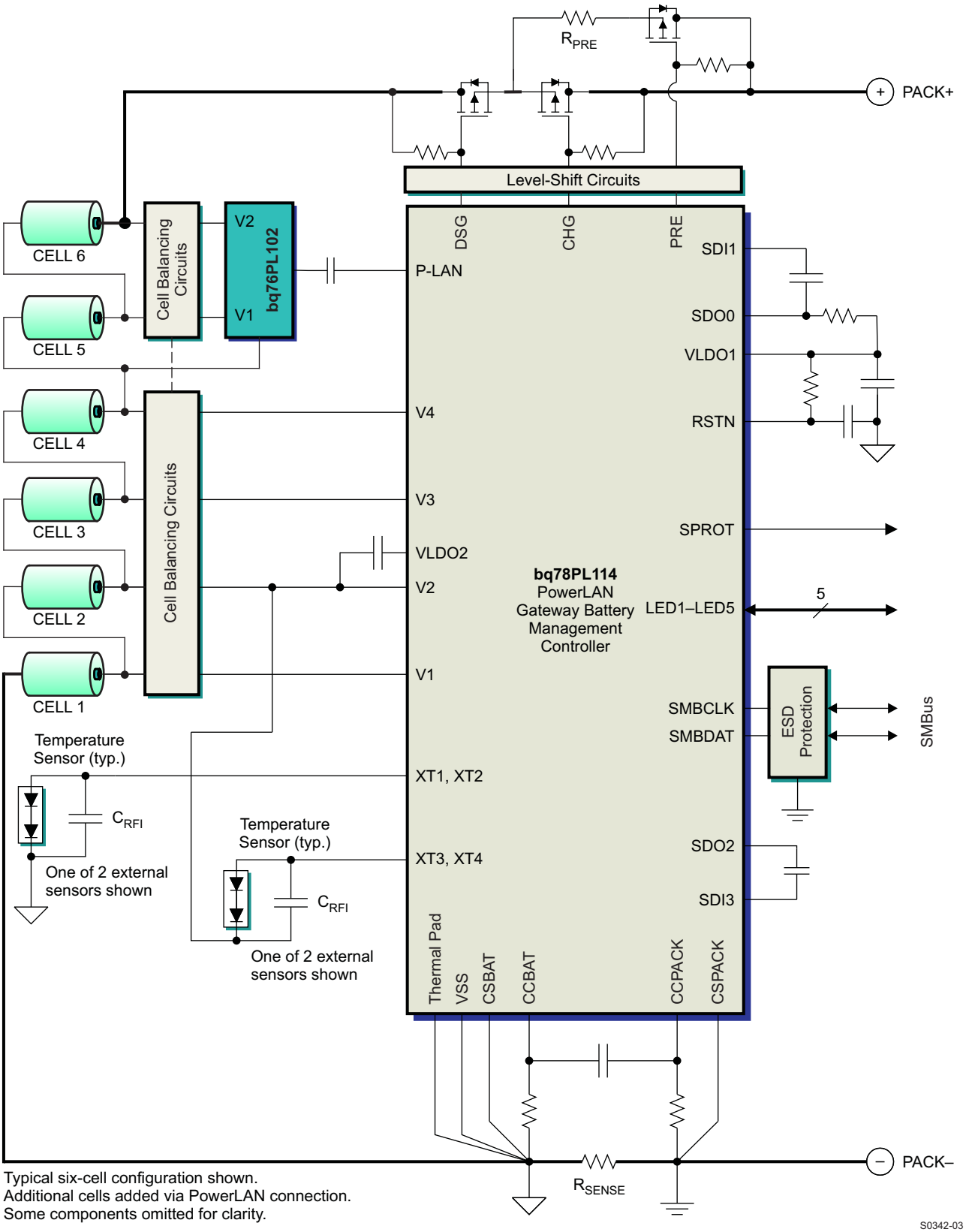


Figure 4. bq78PL114 Simplified 6-Cell Gateway Controller Circuit With bq76PL102

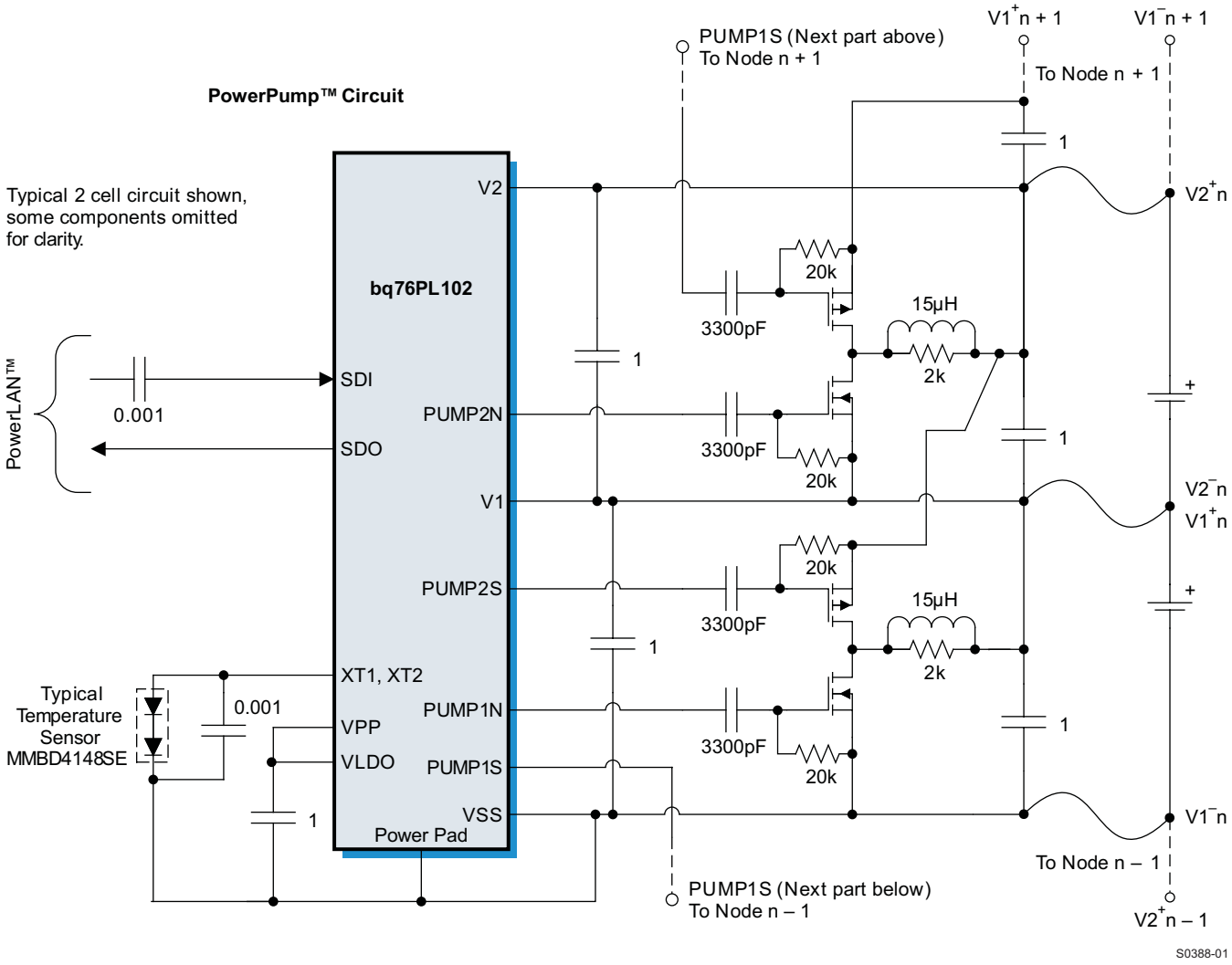


Figure 5. bq76PL102 Simplified Example Operating-Circuit Diagram

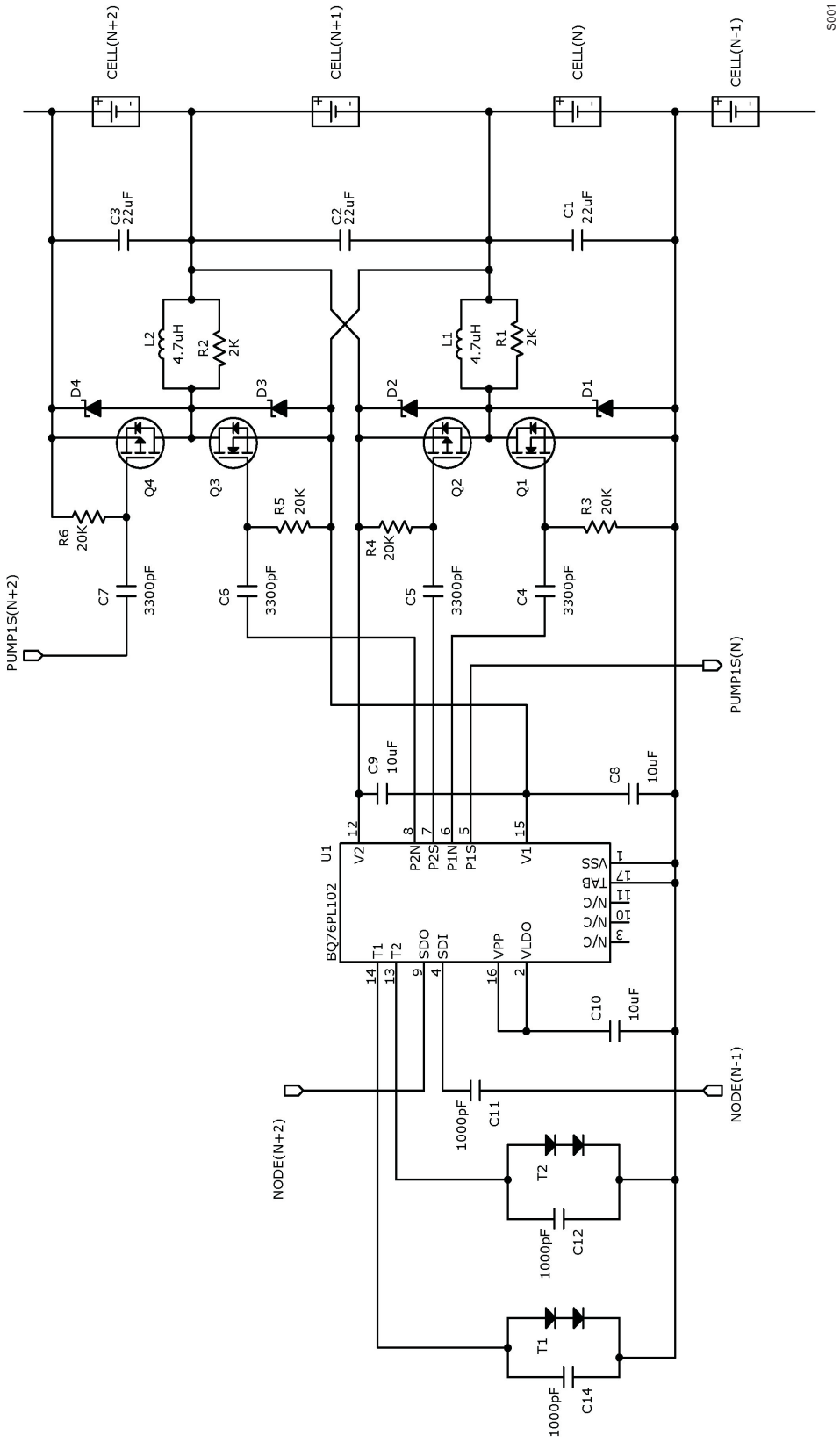


Figure 6. Higher-Balancing-Current bq76PL102 Operating-Circuit Diagram

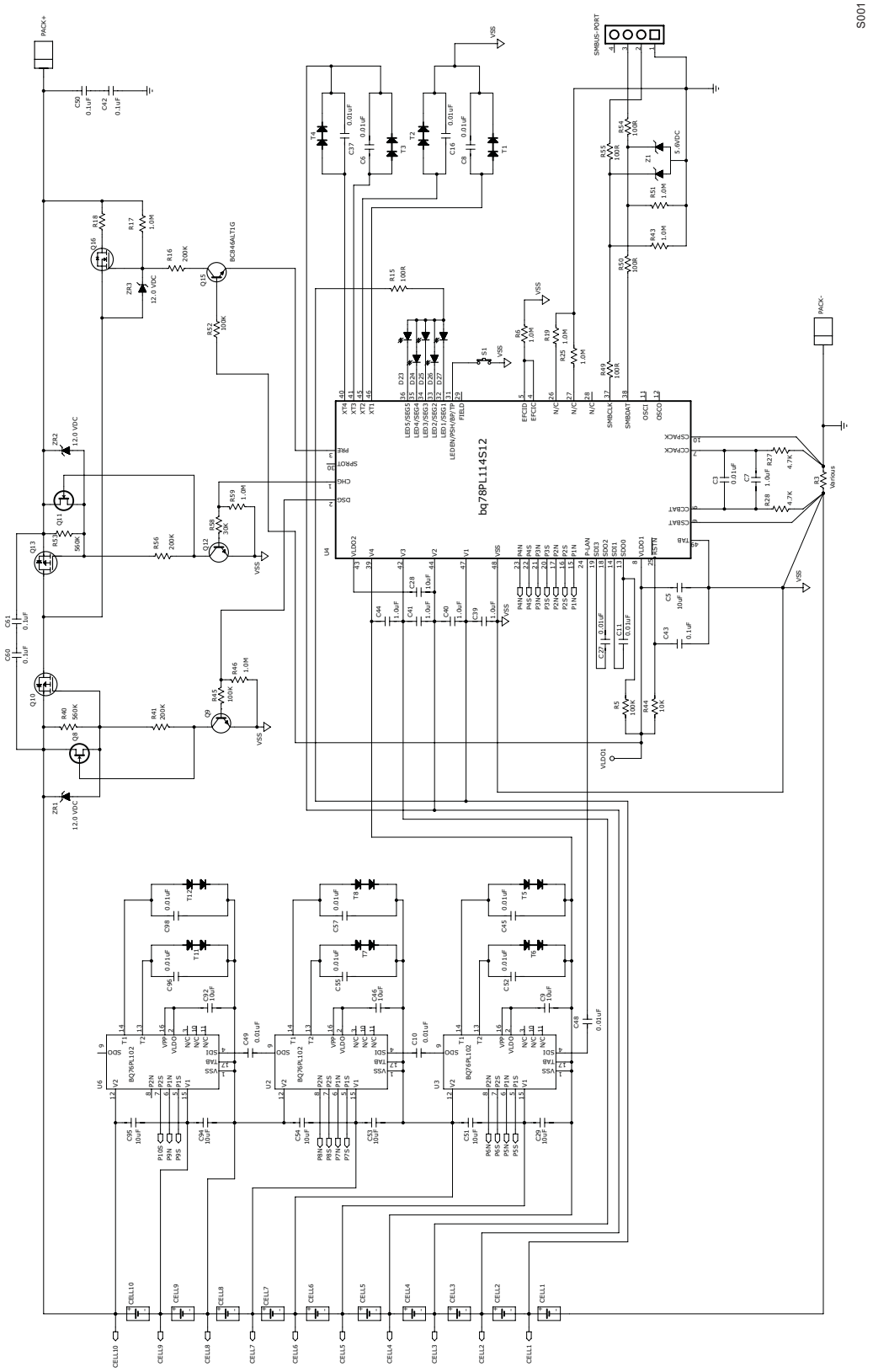


Figure 7. Reference Schematic (Sheet 1 of 2)

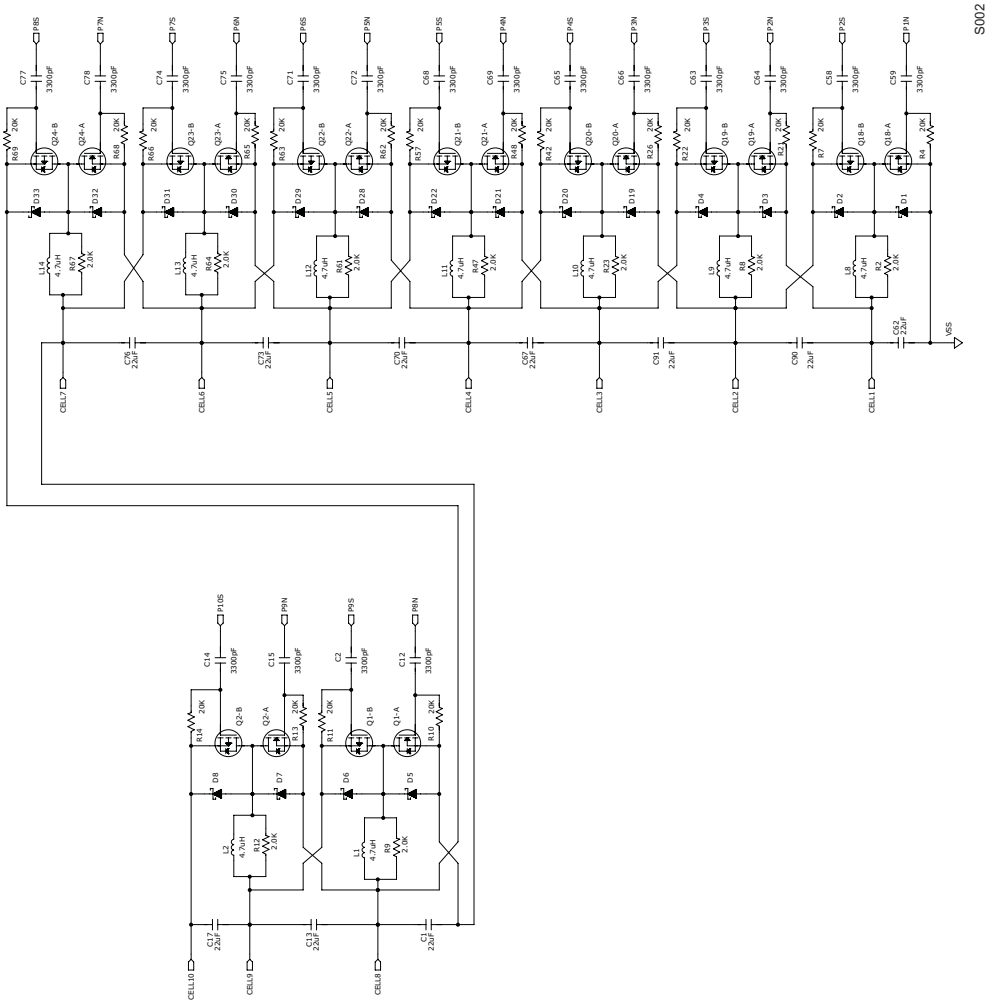


Figure 8. Reference Schematic (Sheet 2 of 2)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ76PL102RGTR	NRND	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OAG	
BQ76PL102RGTT	NRND	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OAG	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

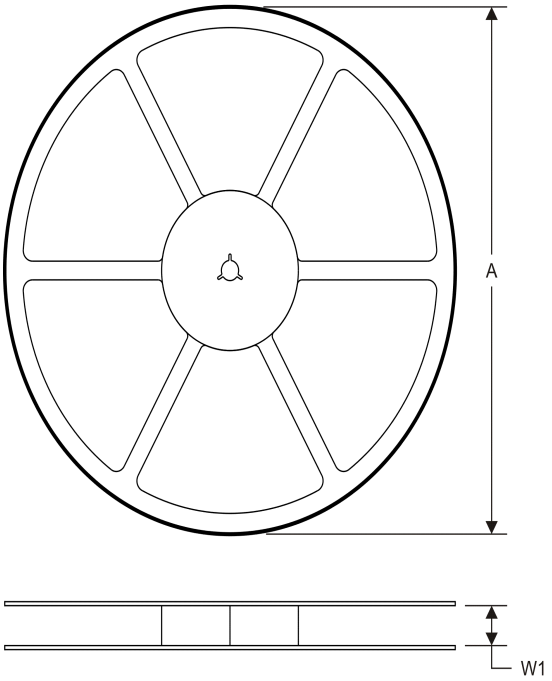
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

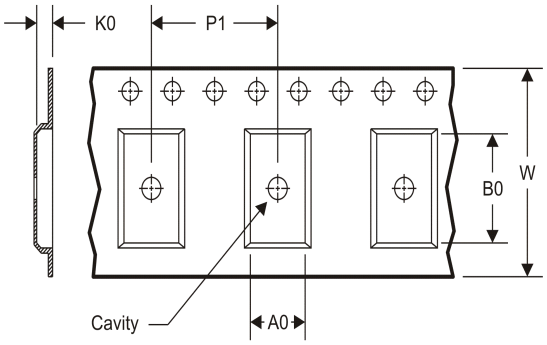
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



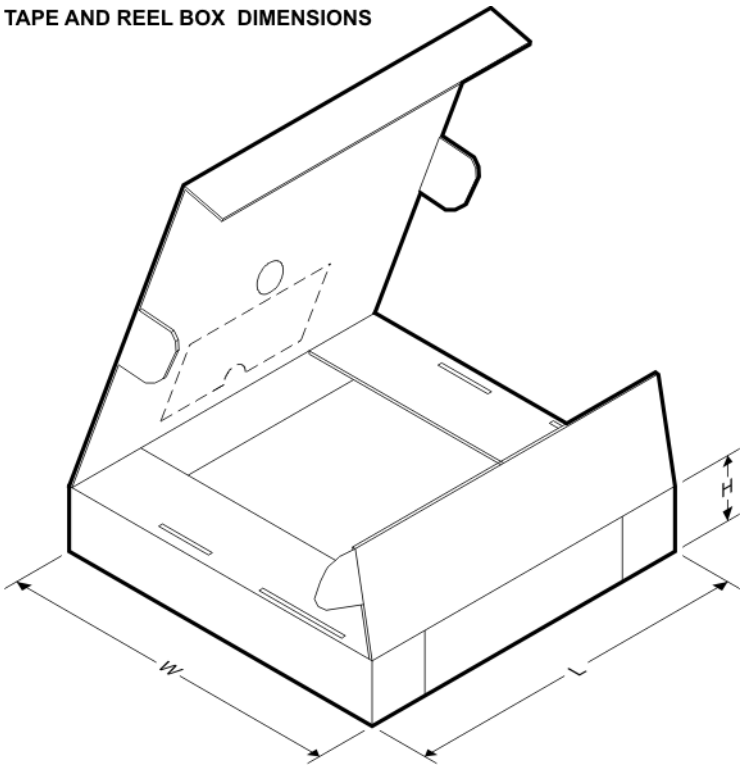
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ76PL102RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ76PL102RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

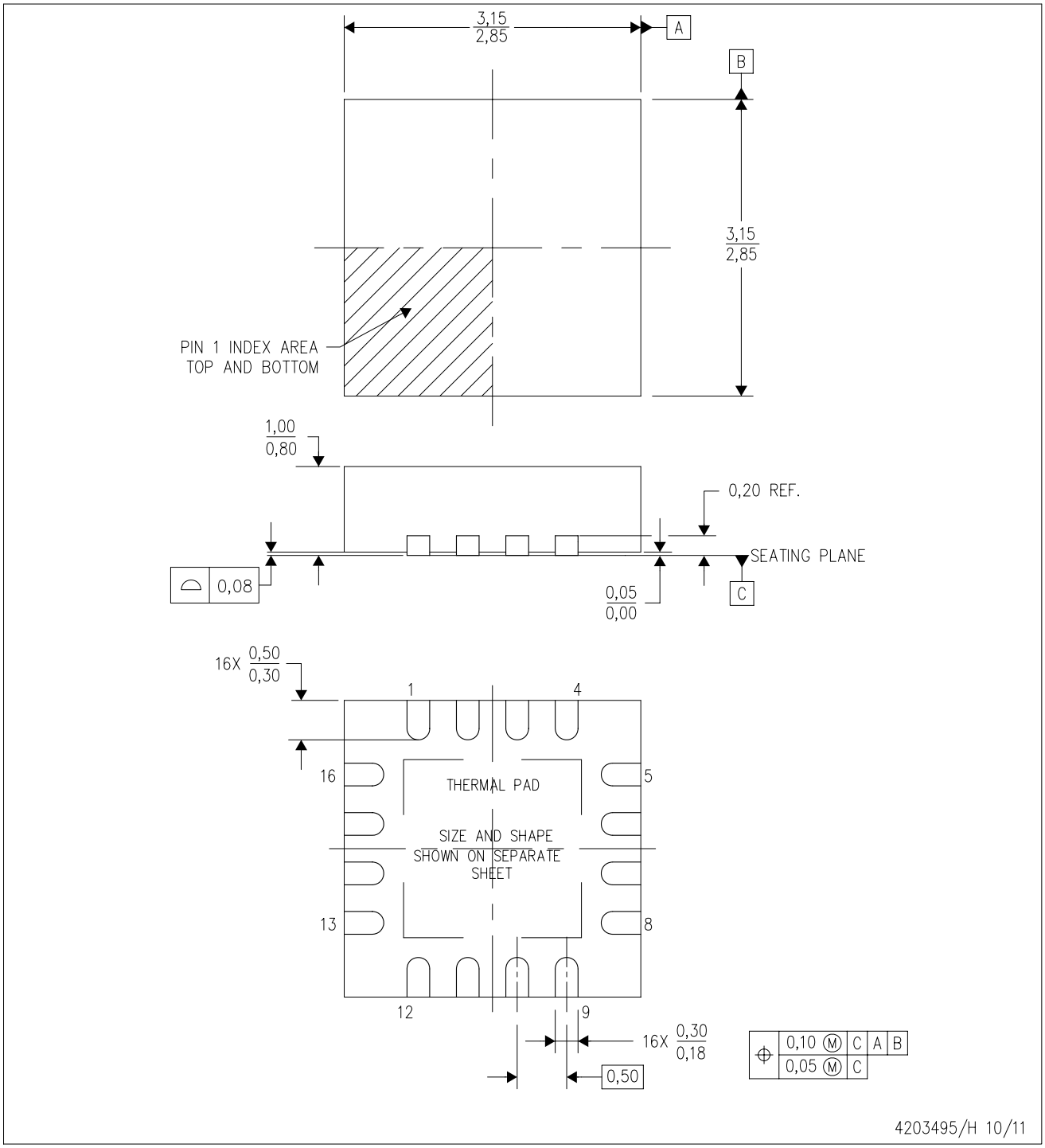
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ76PL102RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ76PL102RGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

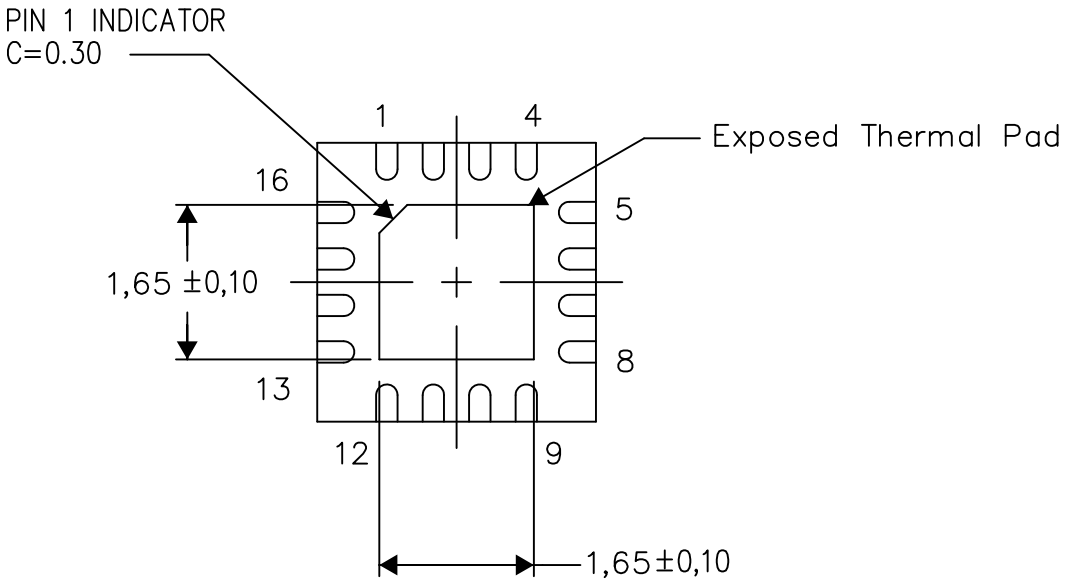
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



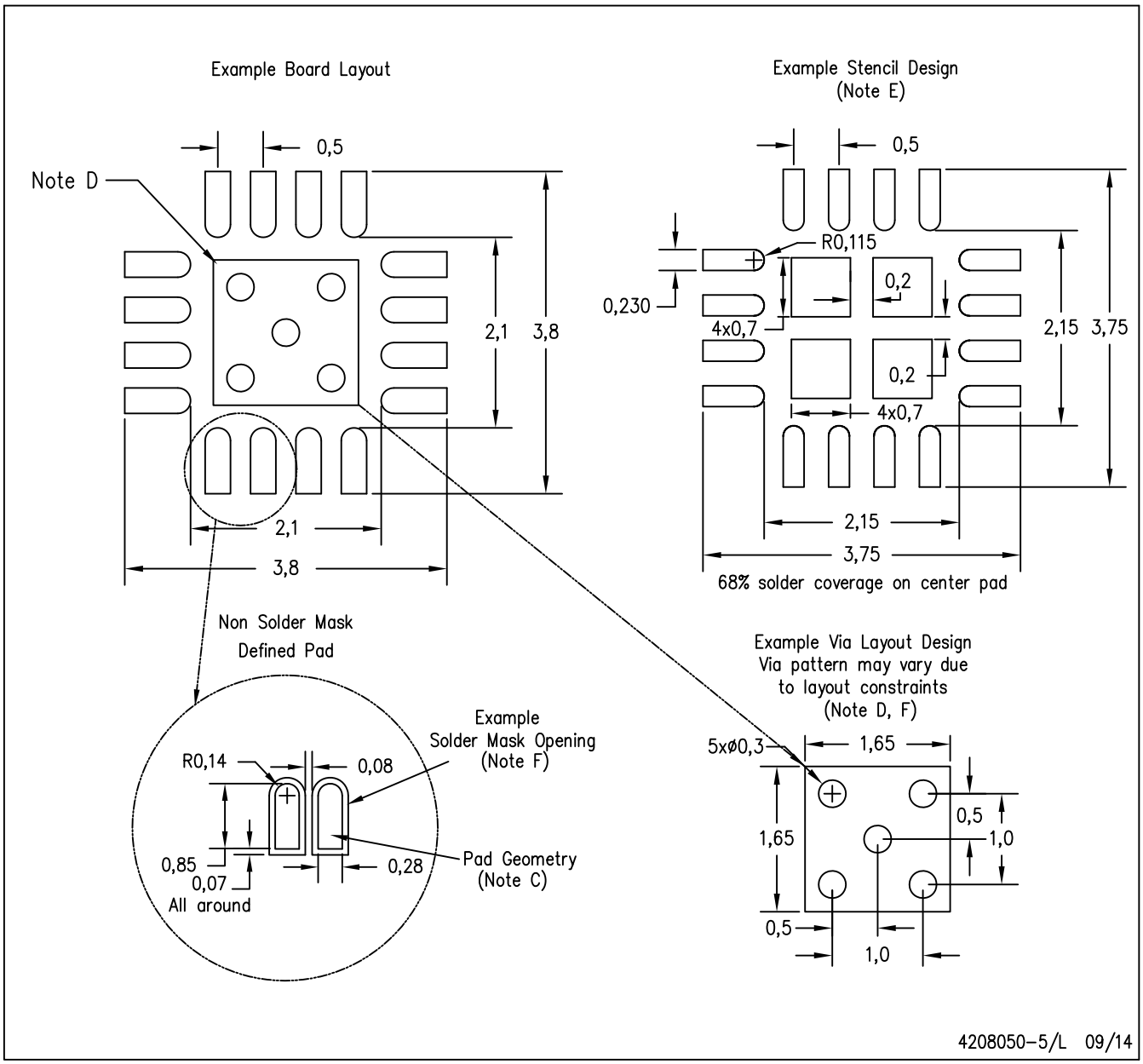
Bottom View

Exposed Thermal Pad Dimensions

4206349–7/W 10/14

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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