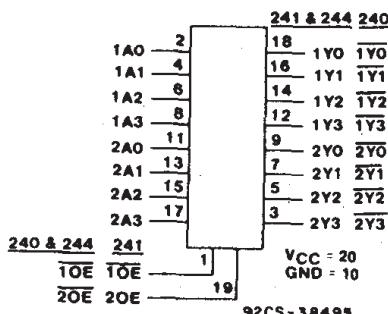


# CD54/74AC240/241/244

## CD54/74ACT240/241/244



Data sheet acquired from Harris Semiconductor  
SCHS287B - Revised January 2004



### FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The RCA CD54/74AC240, CD54/74AC241, and CD54/74AC244 and the CD54/74ACT240, CD54/74ACT241, and CD54/74ACT244 3-state octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT240 and CD54/74AC/ACT244 have active-LOW output enables (TOE, 2OE). The CD54/74AC/ACT241 has one active-LOW (1OE) and one active-HIGH (2OE) output enable.

The CD74AC240 and CD74ACT240 are supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M and M96 suffixes). The CD74AC241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and the CD74ACT241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M96 suffix). The CD74AC244 and CD74ACT244 are supplied in 20-lead dual-in-line plastic packages (E suffix), 20-lead small-outline packages (M and M96 suffixes), and 20-lead shrink small-outline packages (SM96 suffix). These package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC240 and CD54AC244 and the CD54ACT240, CD54ACT241, and CD54ACT244 are supplied in 20-lead hermetic dual-in-line ceramic packages (F3A suffix) and are operable over the -55 to +125°C temperature range.

### TRUTH TABLES

INPUTS		OUTPUT	
10E, 20E	A	Y	
L	L	H	
L	H	L	
H	X	Z	

(AC/ACT240)

INPUTS		OUTPUT	
10E, 20E	A	Y	
L	L	L	
L	H	H	
H	X	X	

(AC/ACT244)

INPUTS		OUTPUT		INPUTS		OUTPUT	
10E	1A	1Y	20E	2A	2Y		
L	L	L	L	X	Z		
L	H	H	H	L	L		
H	X	Z	H	H	H		

(AC/ACT241)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = HIGH Impedance

This data sheet is applicable to the CD54/74AC240, CD54ACT240, and CD54/74ACT241. The CD54/74AC241 were not acquired from Harris Semiconductor. See SCHS244 for information on the CD74ACT240, CD74AC244, and CD74ACT244.

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# CD54/74AC240/241/244 CD54/74ACT240/241/244

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ ) .....	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) .....	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) .....	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) .....	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ ) .....	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -40$ to $+85^\circ\text{C}$ (Package Type E) .....	.....	500 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (Package Type M) .....	.....	400 mW
For $T_A = +70$ to $+85^\circ\text{C}$ (Package Type M) .....	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 310 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ): CD54 .....	.....	-55 to $+125^\circ\text{C}$
CD74 .....	.....	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ ) .....	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum. ....	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only. ....	.....	$+300^\circ\text{C}$

\* For up to 4 outputs per device: add  $\pm 25$  mA for each additional output.

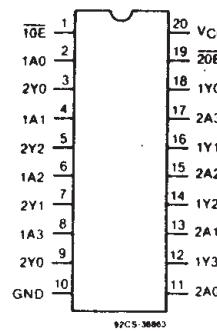
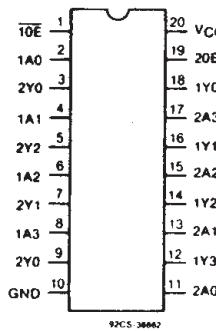
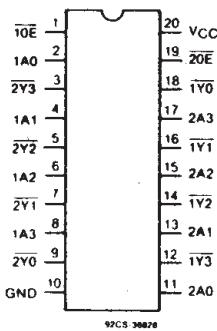
**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$	CD54 CD74	-55 -40 +125 +85	°C
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\* Unless otherwise specified, all voltages are referenced to ground.

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**CD54/74AC, ACT240 TYPES  
TERMINAL ASSIGNMENT**

**CD54/74AC, ACT241 TYPES  
TERMINAL ASSIGNMENT**

**CD54/74AC, ACT244 TYPES  
TERMINAL ASSIGNMENT**

# Technical Data

## CD54/74AC240/241/244 CD54/74ACT240/241/244

### STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>cc</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V <sub>i</sub> (V)	I <sub>o</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>ih</sub>		1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>il</sub>		1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>oh</sub>	V <sub>ih</sub> or V <sub>il</sub> #,*	-0.05	1.5	1.4	—	1.4	—	1.4	V
			-0.05	3	2.9	—	2.9	—	2.9	
			-0.05	4.5	4.4	—	4.4	—	4.4	
			-4	3	2.58	—	2.48	—	2.4	
			-24	4.5	3.94	—	3.8	—	3.7	
			-75	5.5	—	—	3.85	—	—	
			-50	5.5	—	—	—	—	3.85	
Low-Level Output Voltage	V <sub>ol</sub>	V <sub>ih</sub> or V <sub>il</sub> #,*	0.05	1.5	—	0.1	—	0.1	—	V
			0.05	3	—	0.1	—	0.1	—	
			0.05	4.5	—	0.1	—	0.1	—	
			12	3	—	0.36	—	0.44	—	
			24	4.5	—	0.36	—	0.44	—	
			75	5.5	—	—	—	1.65	—	
			50	5.5	—	—	—	—	1.65	
Input Leakage Current	I <sub>i</sub>	V <sub>cc</sub> or GND		5.5	—	±0.1	—	±1	—	±1 μA
3-State Leakage Current	I <sub>oz</sub>	V <sub>ih</sub> or V <sub>il</sub> V <sub>o</sub> = V <sub>cc</sub> or GND		5.5	—	±0.5	—	±5	—	±10 μA
Quiescent Supply Current, MSI	I <sub>cc</sub>	V <sub>cc</sub> or GND	0	5.5	—	8	—	80	—	160 μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC240/241/244

## CD54/74ACT240/241/244

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V <sub>IH</sub>	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #, *	-0.05 -24 -75 -50	4.5 4.5 5.5 5.5	4.4 3.94 — —	— — 3.85 —	4.4 3.8 — —	4.4 3.7 — 3.85	— — — —	V	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #, *	0.05 24 75 50	4.5 4.5 5.5 5.5	— — — —	0.1 0.36 — —	— 0.44 1.65 —	0.1 0.5 — 1.65	— — — —	V	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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## ACT INPUT LOADING TABLES

CD54/74ACT240	
INPUT	UNIT LOADS*
nA0 - A3	1.42
10E	0.83
20E	0.83

CD54/74ACT241	
INPUT	UNIT LOADS*
nA0 - A3	0.5
10E	0.83
20E	1.67

CD54/74ACT244	
INPUT	UNIT LOADS*
nA0 - A3	0.5
10E	0.83
20E	0.83

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

## Technical Data

# CD54/74AC240/241/244 CD54/74ACT240/241/244

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{cc}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
Propagation Delays: Data to Outputs AC240	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 2.6 1.9	82 9.2 6.5	— 2.5 1.8	90 10.1 7.2	ns	
AC241, 244	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3 2.2	93 10.5 7.5	— 2.9 2.1	103 11.5 8.2	ns	
Output Enable Times	$t_{PZL}$ $t_{PZH}$	1.5 3.3 5	— 4.6 3.1	136 16.4 10.9	— 4.5 3	150 18 12	ns	
Output Disable Times	$t_{PLZ}$ $t_{PHZ}$	1.5 3.3 5	— 3.9 3.1	136 13.6 10.9	— 3.8 3	150 15 12	ns	
Power Dissipation Capacitance AC240 AC241, 244	$C_{PD\$}$	— —		65 Typ. 71 Typ.		65 Typ. 71 Typ.	pF	
Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Fig. 1	5			4 Typ. @ 25°C		V	
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5			1 Typ. @ 25°C		V	
Input Capacitance	$C_I$	—	—	10	—	10	pF	
3-State Output Capacitance	$C_O$	—	—	15	—	15	pF	

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{cc}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
Propagation Delays: Data to Outputs ACT240	$t_{PLH}$ $t_{PHL}$	5†	2.3	7.8	2.2	8.6	ns	
ACT241, 244	$t_{PLH}$ $t_{PHL}$	5	2.5	8.7	2.4	9.6	ns	
Output Enable Times	$t_{PZL}$ $t_{PZH}$	5	3.5	12.2	3.4	13.4	ns	
Output Disable Times	$t_{PLZ}$ $t_{PHZ}$	5	3.5	12.2	3.4	13.4	ns	
Power Dissipation Capacitance ACT240 ACT241, 244	$C_{PD\$}$	— —	65 Typ. 71 Typ.		65 Typ. 71 Typ.		pF	
Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Fig. 1	5		4 Typ. @ 25°C			V	
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5		1 Typ. @ 25°C			V	
Input Capacitance	$C_I$	—	—	10	—	10	pF	
3-State Output Capacitance	$C_O$	—	—	15	—	15	pF	

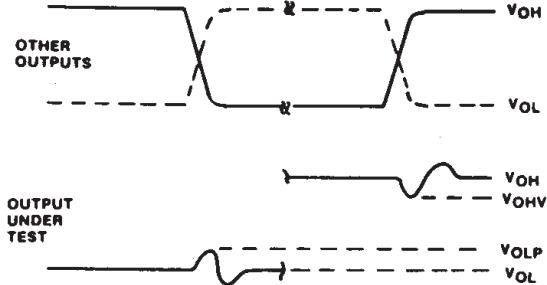
\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

‡ $C_{PD}$  is used to determine the dynamic power consumption, per package.  
For AC series:  $P_D = V_{cc}^2 f_i (C_{PD} + C_L)$   
For ACT series:  $P_D = V_{cc}^2 f_i (C_{PD} + C_L) + V_{cc} \Delta I_{cc}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{cc}$  = supply voltage

# CD54/74AC240/241/244 CD54/74ACT240/241/244

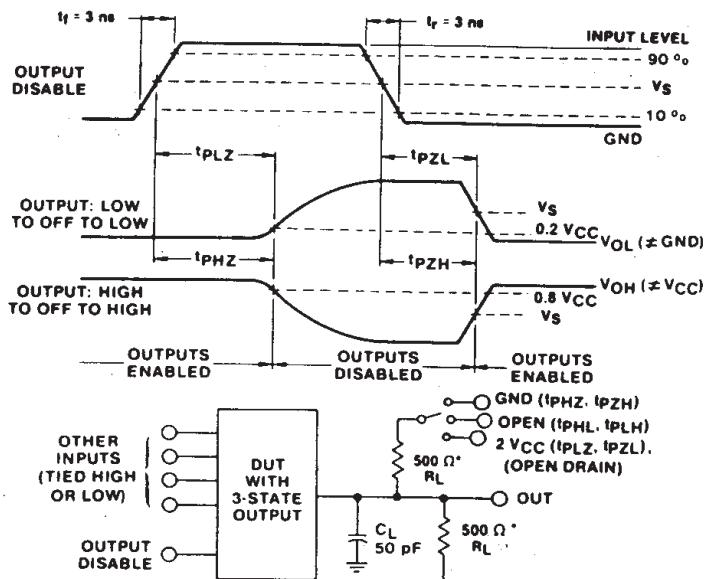
## PARAMETER MEASUREMENT INFORMATION



## NOTES:

1. V<sub>OH</sub> AND V<sub>OL</sub> ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR  $\leq$  1 MHz, t<sub>r</sub> = 3 ns, t<sub>f</sub> = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

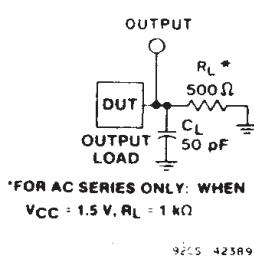
92CS-42406

\*FOR AC SERIES ONLY: WHEN V<sub>CC</sub> = 1.5 V, R<sub>L</sub> = 1 k $\Omega$ 

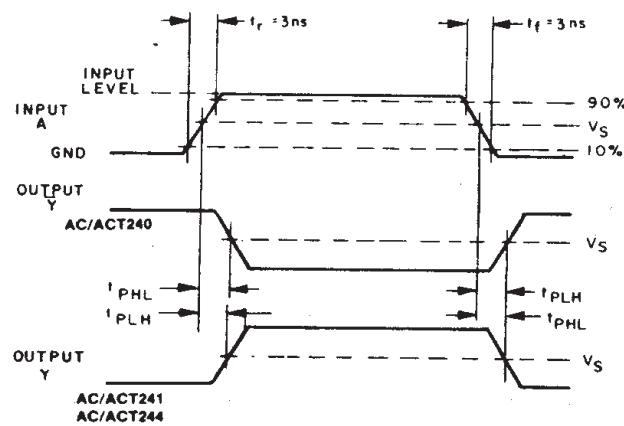
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Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay times and test circuit.

\*FOR AC SERIES ONLY: WHEN V<sub>CC</sub> = 1.5 V, R<sub>L</sub> = 1 k $\Omega$ 

92CS-42389



92CS-42407

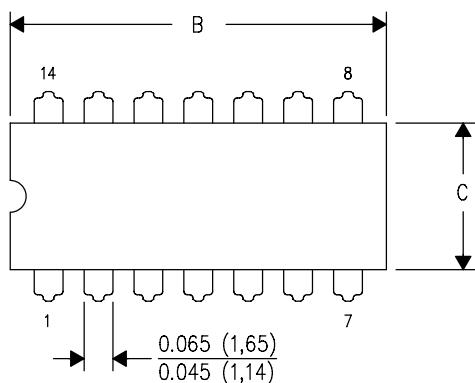
Fig. 3 - Propagation delay times and test circuit.

	CDS4/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

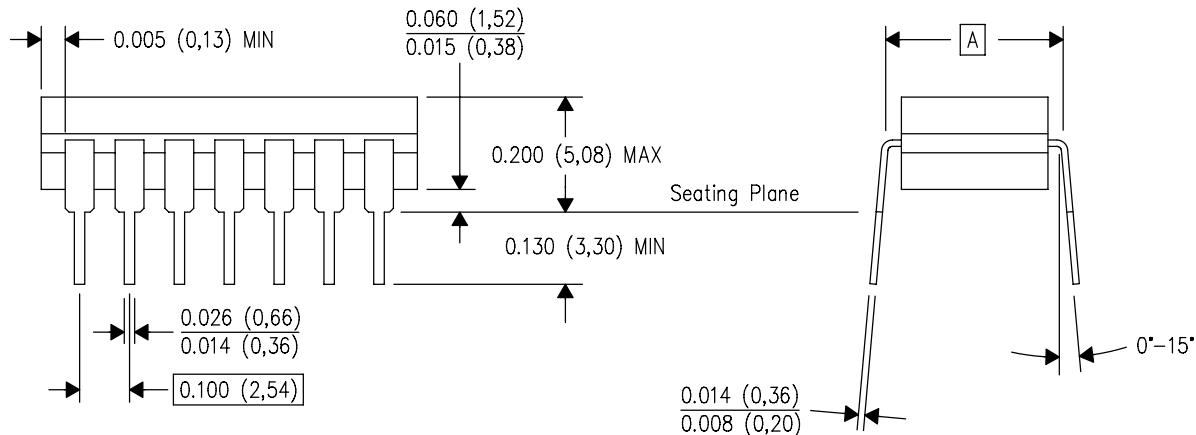
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

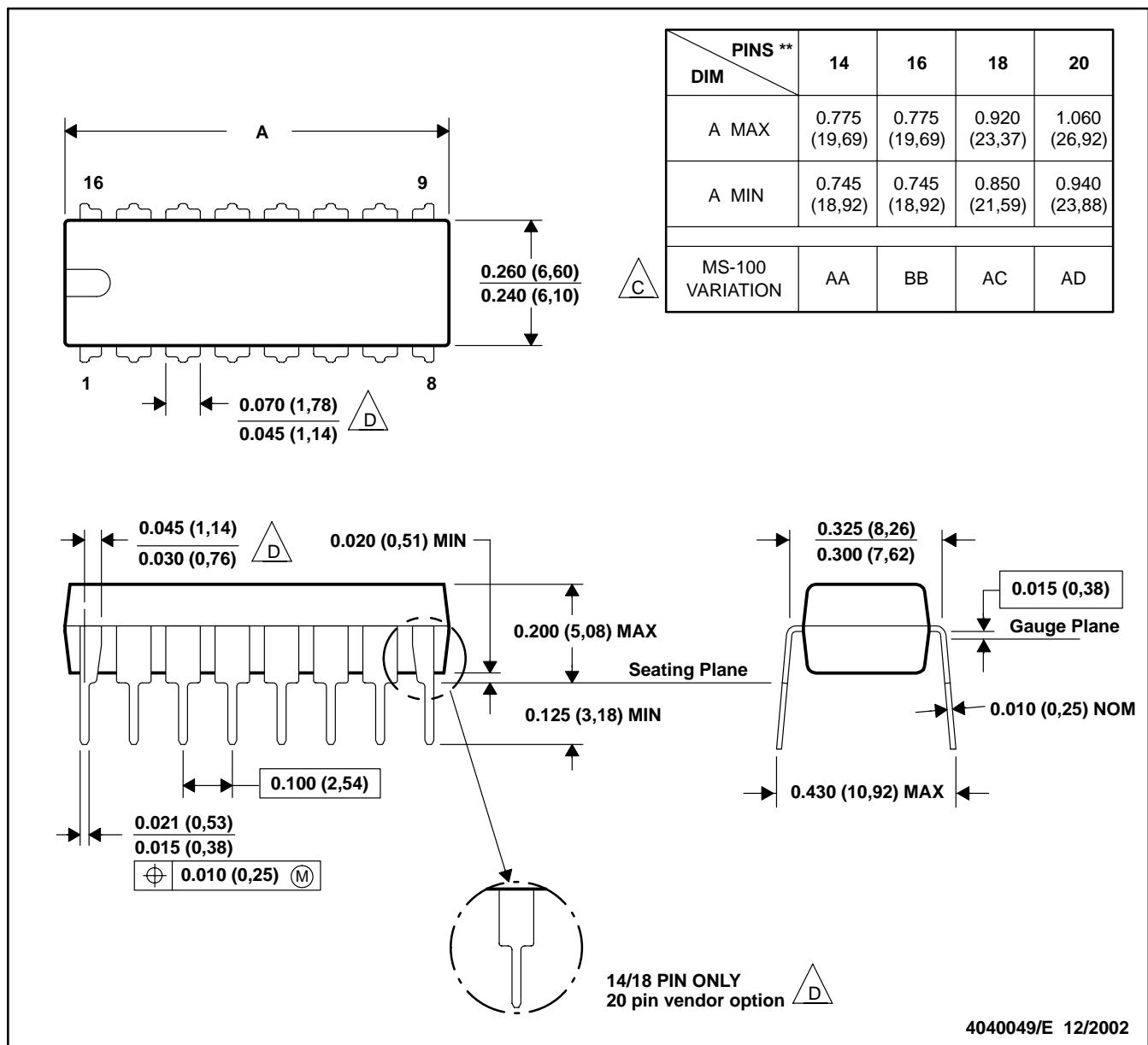
# MECHANICAL

MPDI002C – JANUARY 1995 – REVISED DECEMBER 20002

N (R-PDIP-T\*\*)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

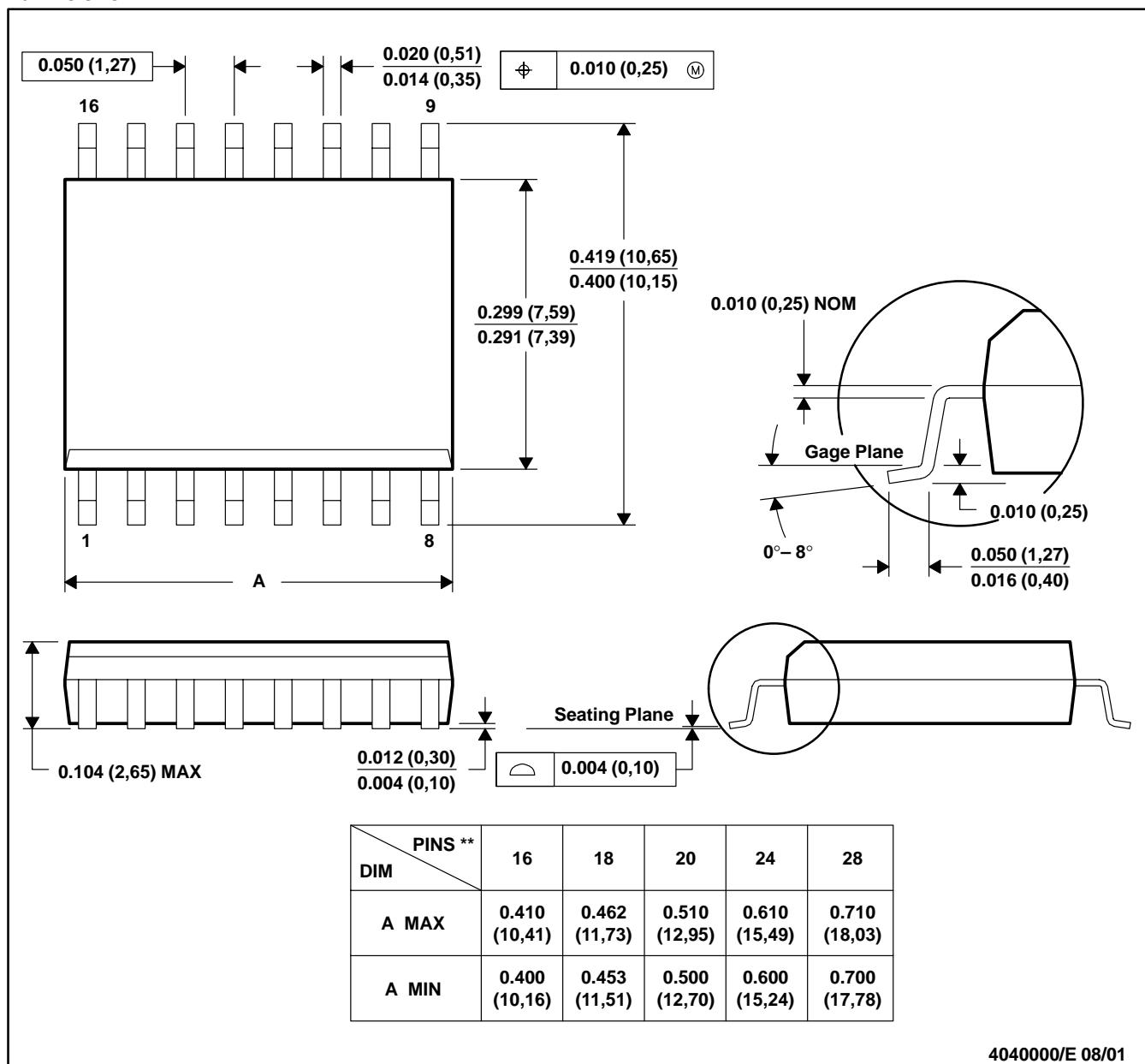
Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



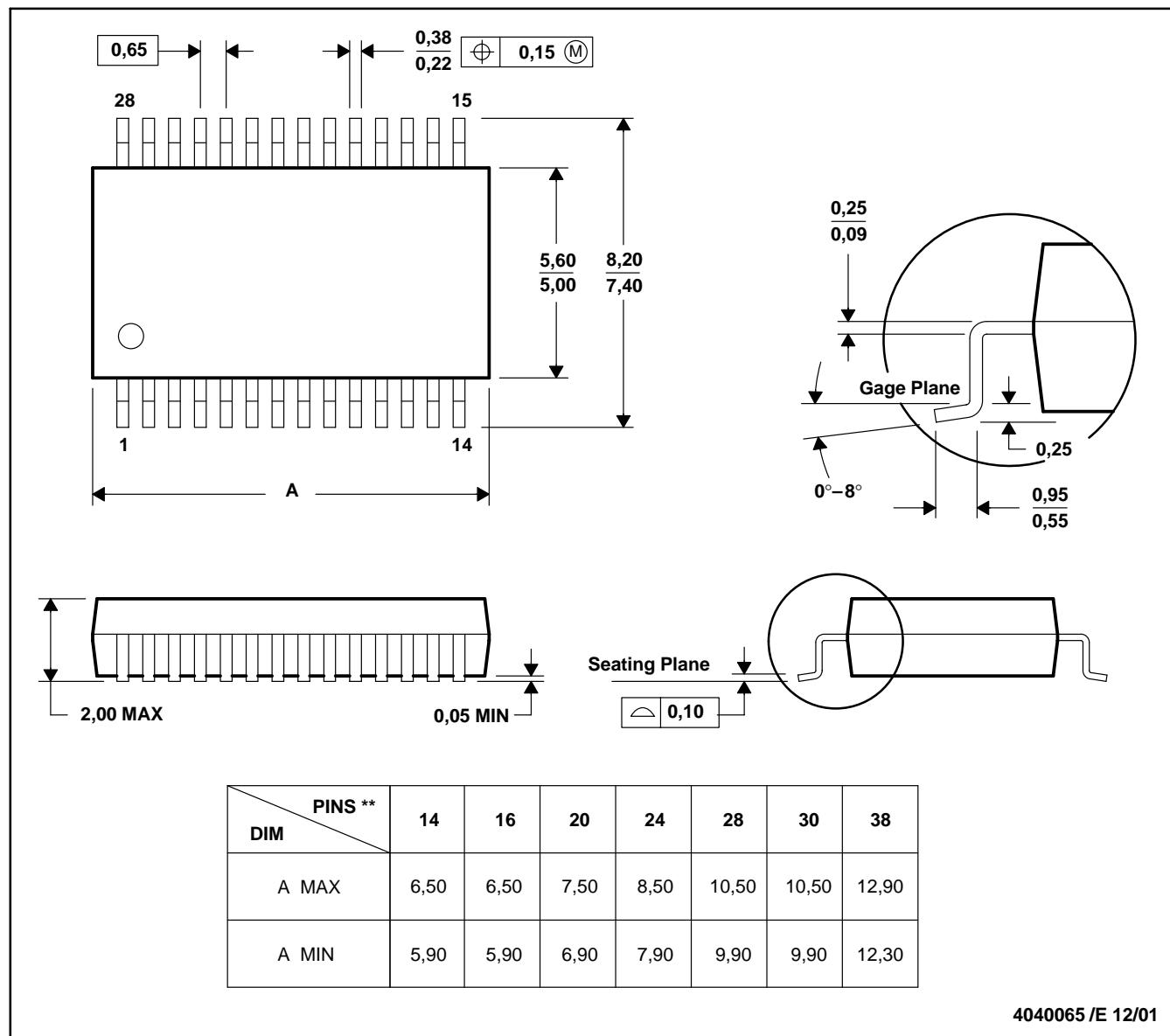
4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).  
 D. Falls within JEDEC MS-013

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150

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