CD74ACT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

GND II 8

SCHS340B - MARCH 2003 - REVISED JUNE 2003

9**∏** 3Y

Inputs Are TTL-Voltage Compatible E, M, OR PW PACKAGE (TOP VIEW) Speed of Bipolar F, AS, and S, With **Significantly Reduced Power Consumption** A/B 16 V_{CC} **Balanced Propagation Delays** 1A [2 15 🛮 🗖 ±24-mA Output Drive Current 1B **∏** 14 | | 4A - Fanout to 15 F Devices 1Y [13 AB 2А Г 12 T 4Y 5 SCR-Latchup-Resistant CMOS Process and 2B [11 **∏** 3A Circuit Design 2Y 🛮 7 10 3B **Exceeds 2-kV ESD Protection Per**

description/ordering information

MIL-STD-883, Method 3015

This quadruple 2-line to 1-line data selector/multiplexer is designed for 4.5-V to 5.5-V V_{CC} operation.

The CD74ACT157 features a common strobe (\overline{G}) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

ORDERING INFORMATION

T _A PACKA		AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – E	Tube	CD74ACT157E	CD74ACT157E
	SOIC - M	Tube	CD74ACT157M	AOT457N
-55°C to 125°C		Tape and reel	CD74ACT157M96	ACT157M
	TCCOD DW	Tube	CD74ACT157PW	1104457
	TSSOP – PW	Tape and reel	CD74ACT157PWR	HM157

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

	INPU	OUTPUT		
G	A/B	Α	Υ	
Н	Χ	Χ	Х	L
L	L	L	X	L
L	L	Н	X	Н
L	Н	Χ	L	L
L	Н	Χ	Н	Н

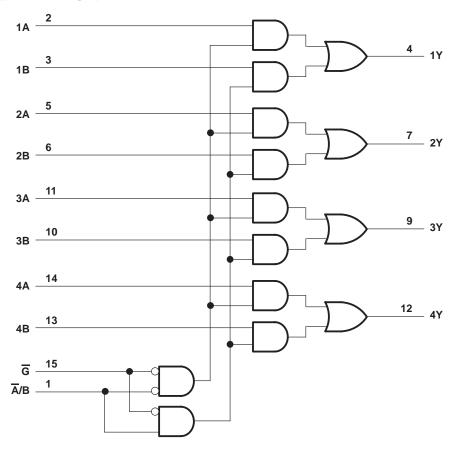


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0 \text{ V or } V_I > V_{CC}$) (s	see Note 1)	±20 mA
Output clamp current, IOK (VO < 0 V or VO > VO	CC) (see Note 1)	±50 mA
Continuous output current, IO (VO > 0 V or VO	< V _{CC})	±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 2):	E package	67°C/W
	M package	73°C/W
	PW package	108°C/W
Storage temperature range, T _{stq}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

		T _A = 2	T _A = 25°C		T _A = 25°C		C to °C	–40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX			
VCC	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V		
VIH	High-level input voltage	2		2		2		V		
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V		
VI	Input voltage	0	VCC	0	VCC	0	VCC	V		
VO	Output voltage	0	VCC	0	VCC	0	VCC	V		
IOH	High-level output current		-24		-24		-24	mA		
loL	Low-level output current		24		24		24	mA		
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	V _{CC}	T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	
	Ve Ver or Ve	I _{OH} = -50 μA	4.5 V	4.4		4.4		4.4		
V		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		V
Voн	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
	V VV	Ι _Ο L = 50 μΑ	4.5 V		0.1		0.1		0.1	
V		$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44	.,
VoL	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				1.65			V
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65	
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND,	I _O = 0	5.5 V		8		160		80	μΑ
Δl _{CC} ‡	$V_{I} = V_{CC} - 2.1 \text{ V}$		4.5 V to 5.5 V		2.4		3		2.8	mA
C _i					10		10		10	pF

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C. ‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD
A or B	0.37
G	0.83
Ā/B	1.33

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).



CD74ACT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	–55° 125		-40°0 85°	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
^t PLH	A - :: B	A	2.4	9.5	2.5	8.6	
^t PHL	A or B	Any Y	2.4	9.5	2.5	8.6	ns
^t PLH	Ā/B	A	3.6	14.5	3.8	13.2	
t _{PHL}	A/B	Any Y	3.6	14.5	3.8	13.2	ns
^t PLH	G	Any V	3.4	13.5	3.6	12.3	20
tPHL	G	Any Y	3.4	13.5	3.6	12.3	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

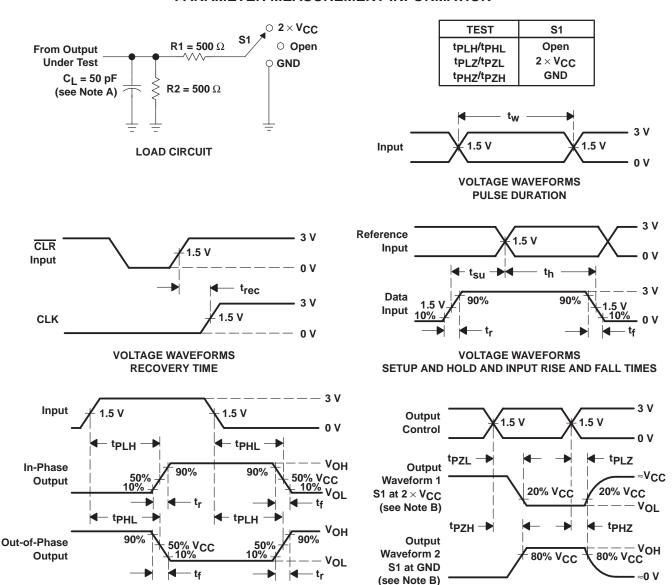
	PARAMETER	TYP	UNIT
C _{pd}	Power dissipation capacitance	156	pF



VOLTAGE WAVEFORMS

OUTPUT ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 3 \ ns$, $t_f = 3 \ ns$. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tpzL and tpzH are the same as ten.
- H. tpLZ and tpHZ are the same as t_{dis}.
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74ACT157E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT157EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT157M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT157PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

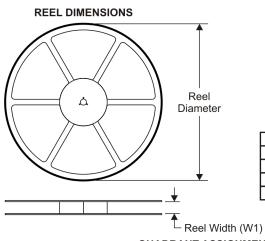
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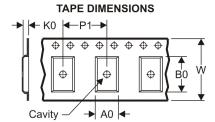
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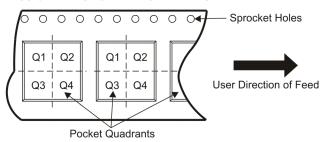
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

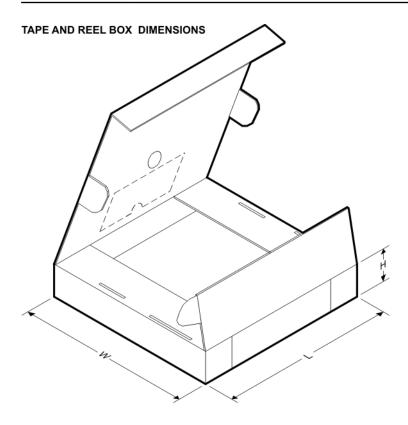
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
Ī	CD74ACT157M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
I	CD74ACT157PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT157M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74ACT157PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

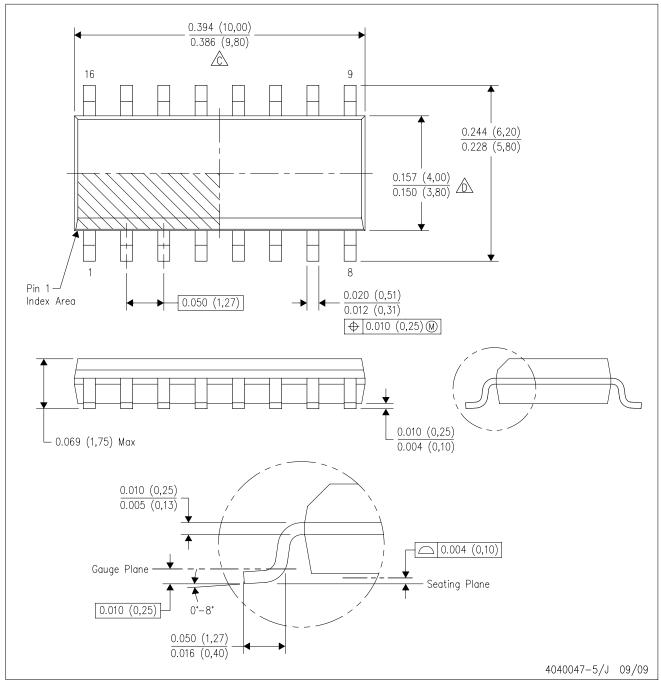
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

D (R-PDS0-G16)

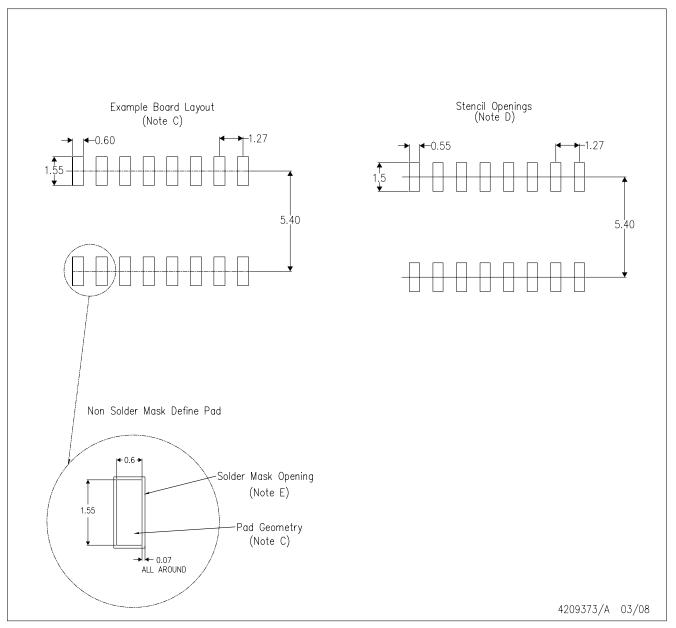
PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



D(R-PDSO-G16)



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OPTION ADDENDUM

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CD74ACT157PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
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TBD: The Pb-Free/Green conversion plan has not been defined.

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PACKAGE OPTION ADDENDUM

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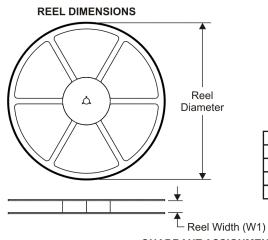
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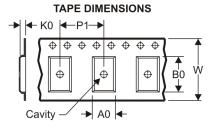
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





_		
	A0	Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

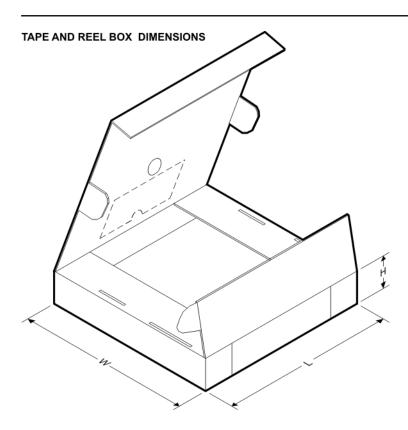
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT157M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT157M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74ACT157PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE

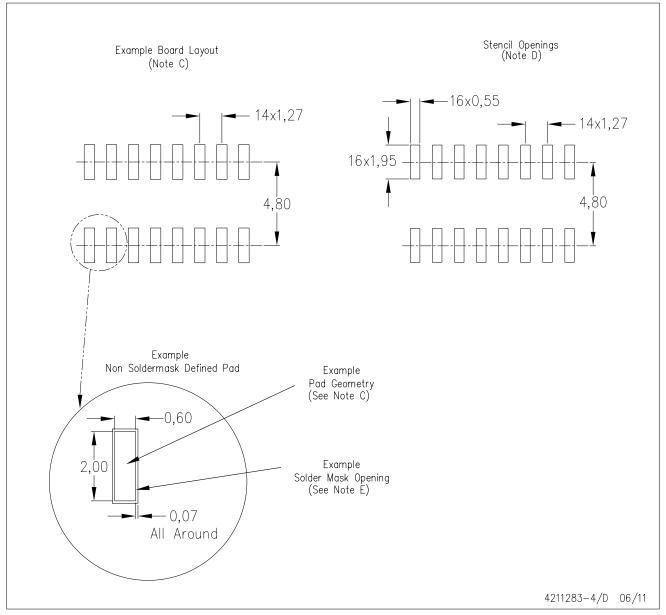


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

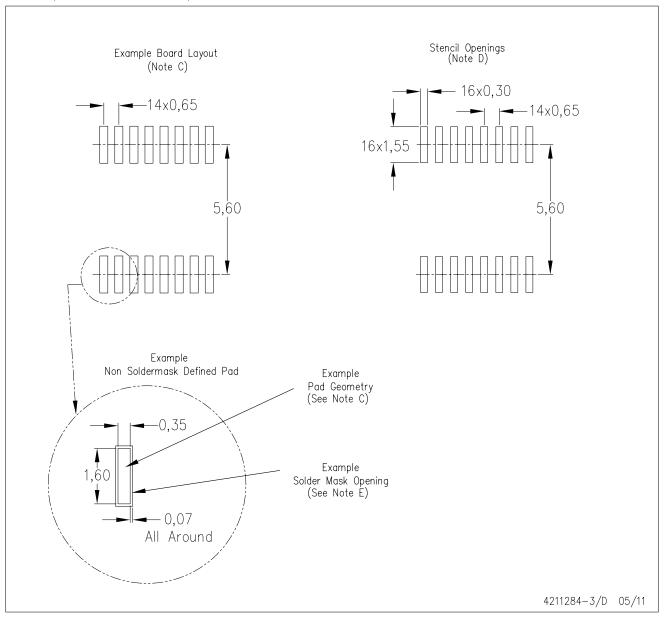


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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