LOW-VOLTAGE 1:10 LVPECL WITH SELECTABLE INPUT CLOCK DRIVER

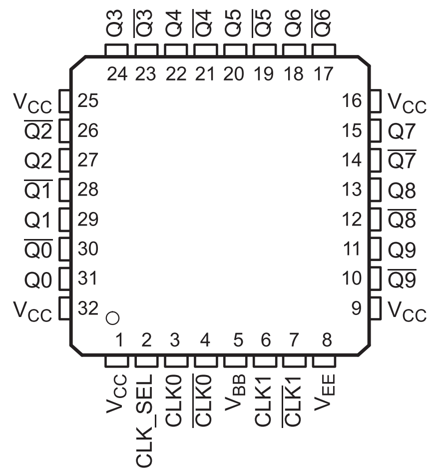
FEATURES

- **Distributes One Differential Clock Input Pair LVPECL to 10 Differential LVPECL**
- **Fully Compatible With LVECL/LVPECL**
- **Supports a Wide Supply Voltage Range From 2.375 V to 3.8 V**
- **Selectable Clock Input Through CLK_SEL**
- **Low-Output Skew (Typ 15 ps) for Clock-Distribution Applications**
  - **Additive Jitter Less Than 1 ps**
  - **Propagation Delay Less Than 350 ps**
  - **Open Input Default State**
  - **LVDS, CML, SSTL input compatible**
- **V_{BB} Reference Voltage Output for Single-Ended Clocking**
- **Available in a 32-Pin LQFP and QFN Package**
- **Frequency Range From DC to 3.5 GHz**
- **Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111**

APPLICATIONS

- **Designed for Driving 50 Ω Transmission Lines**
- **High Performance Clock Distribution**

LQFP AND QFN PACKAGE (TOP VIEW)



DESCRIPTION

The CDCLVP111 clock driver distributes one differential clock pair of LVPECL input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP111 can accept two clock sources into an input multiplexer. The CDCLVP111 is specifically designed for driving 50-Ω transmission lines. When an output pin is not used, leaving it open is recommended to reduce power consumption. If only one of the output pins from a differential pair is used, the other output pin must be identically terminated to 50 Ω.

The V_{BB} reference voltage output is used if single-ended input operation is required. In this case, the V_{BB} pin should be connected to $\overline{CLK0}$ and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

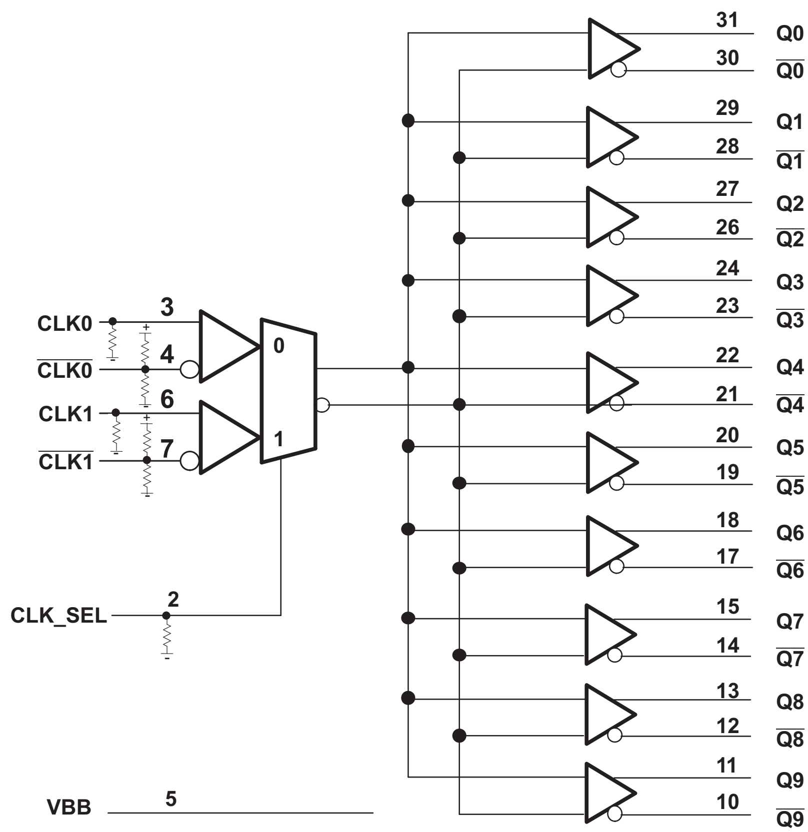
The CDCLVP111 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, $\overline{CLK0}$
1	CLK1, $\overline{CLK1}$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION



PIN FUNCTIONS(1)

PIN		DESCRIPTION
NAME	NO.	
CLK_SEL	2	Clock select. Used to select between CLK0 and CLK1 input pairs. LVTTL/LVCMOS functionality compatible.
CLK0, $\overline{CLK0}$	3, 4	Differential LVECL/LVPECL input pair
CLK1, $\overline{CLK1}$	6, 7	
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
$\overline{Q}$[9:0]	10, 12, 14, 17, 19, 21,23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{CLKn}$.
V_{BB}	5	Reference voltage output for single-ended input operation
V_{CC}	1, 9, 16, 25, 32	Supply voltage
V_{EE}	8	Device ground or negative supply voltage in ECL mode

(1) The PowerPAD™ of the QFN32 package is thermally connected to the die to improve the heat transfer out of the package. This pad is connected to V_{EE}. CLKn, CLK_SEL pull down resistor = 75 kΩ; $\overline{CLKn}$ pull up resistor = 37.5 kΩ; $\overline{CLKn}$ pull down resistor = 50 kΩ.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_{CC}	Supply voltage (Relative to V_{EE})	–0.3 to 4.6	V
V_I	Input voltage	–0.3 to V_{CC} + 0.5	V
V_O	Output voltage	–0.3 to V_{CC} + 0.5	V
I_{IN}	Input current	±20	mA
V_{EE}	Negative supply voltage (Relative to V_{CC})	–4.6 to 0.3	V
I_{BB}	Sink/source current	–1 to 1	mA
I_O	DC output current	–50	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Maximum operating junction temperature	125	°C

(1) Stresses beyond those listed under "absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (relative to V_{EE})	2.375	2.5/3.3	3.8	V
T_A	Operating free-air temperature	–40		85	°C/W
T_J	Operating junction temperature			110	°C

PACKAGE THERMAL IMPEDANCE, VF (LQFP)

		TEST CONDITION	VALUE	UNIT
θ_{JA}	Thermal resistance junction to ambient(1)	0 LFM	74	°C/W
		150 LFM	66	°C/W
		250 LFM	64	°C/W
		500 LFM	61	°C/W
θ_{JC}	Thermal resistance junction to case		39	°C/W

(1) According to JESD 51-7 standard.

PACKAGE THERMAL IMPEDANCE, RHB (QFN)

		TEST CONDITION	VALUE	UNIT
θ_{JA}	Thermal resistance junction to ambient(1)	0 LFM	49	°C/W
		150 LFM	37	°C/W
		250 LFM	36	°C/W
		500 LFM	32	°C/W
θ_{JC}	Thermal resistance junction to case		19	°C/W

(1) According to JESD 51-7 standard.

LVECL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85°C	40		85	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} – 2 V	–40°C			354	mA
			25°C			380	
			85°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors, V_{IH} = V_{CC}, V_{IL} = V_{CC} - 2 V	–40°C, 25°C, 85°C	–150		150	µA

LVECL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply: V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{BB}	Internally generated bias voltage	For V_{EE} = –3 to –3.8 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.45	–1.3	–1.15	V
		V_{EE} = –2.375 to –2.75 V, I_{BB} = –0.2 mA	-40°C, 25°C, 85°C	–1.4	–1.25	–1.1	
V_{IH}	High-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	–1.165		–0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	–1.81		–1.475	V
V_{ID}	Input amplitude (CLKn, $\overline{CLKn}$)	Difference of input $\lvert V_{IH} - V_{IL} \rvert$, See [(1)]	–40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, $\overline{CLKn}$)	DC offset relative to V_{EE}	–40°C, 25°C, 85°C	V_{EE} + 1		–0.3	V
V_{OH}	High-level output voltage	I_{OH} = –21 mA	–40°C	–1.26		–0.85	V
			25°C	–1.2		–0.85	
			85°C	–1.15		–0.85	
V_{OL}	Low-level output voltage	I_{OL} = –5 mA	–40°C	–1.85		–1.5	V
			25°C	–1.85		–1.45	
			85°C	–1.85		–1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} –2 V, See Figure 3	–40°C, 25°C, 85°C	600			mV

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

LVPECL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	-40°C, 25°C, 85°C	40		85	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} - 2 V	-40°C			354	mA
			25°C			380	
			85°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors V_{IH}=V_{CC}, V_{IL}= V_{CC}–2V	-40°C, 25°C, 85°C	–150		150	μA
V_{BB}	Internally generated bias voltage	V_{CC} = 3 to 3.8 V, I_{BB}= –0.2 mA	-40°C, 25°C, 85°C	V_{CC} – 1.45	V_{CC} – 1.3	V_{CC} – 1.15	V
		V_{CC} = 2.375 to 2.75 V, I_{BB} = –0.2 mA	-40°C, 25°C, 85°C	V_{CC} – 1.4	V_{CC} – 1.25	V_{CC} – 1.1	
V_{IH}	High-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	V_{CC} – 1.165		V_{CC} – 0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	V_{CC} – 1.81		V_{CC} – 1.475	V
V_{ID}	Input amplitude (CLKn, $\overline{CLKn}$)	Difference of input $\lvert V_{IH} - V_{IL} \rvert$, see [(1)]	-40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, $\overline{CLKn}$)	DC offset relative to V_{EE}	-40°C, 25°C, 85°C	1		V_{CC} – 0.3	V
V_{OH}	High-level output voltage	I_{OH} = -21 mA	-40°C	V_{CC} – 1.26		V_{CC} – 0.85	V
			25°C	V_{CC} – 1.2		V_{CC} – 0.85	
			85°C	V_{CC} – 1.15		V_{CC} – 0.85	

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

LVPECL DC ELECTRICAL CHARACTERISTICS (continued)

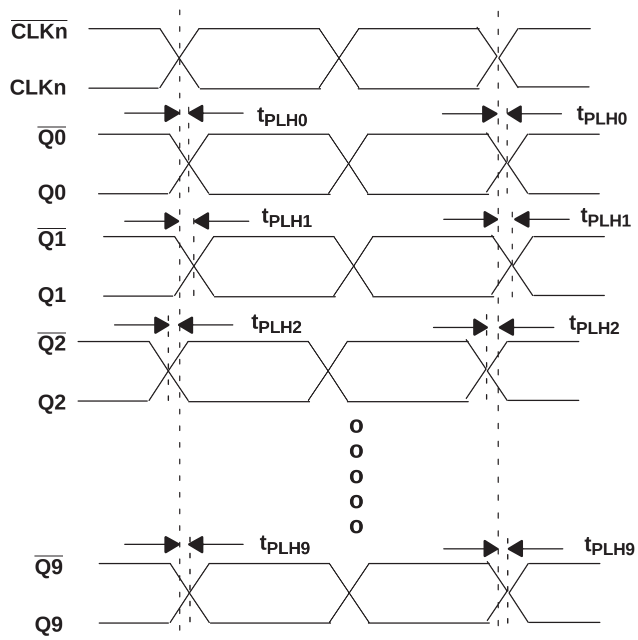
Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = -5 mA	-40°C	V_{CC} – 1.85		V_{CC} – 1.5	V
			25°C	V_{CC} – 1.85		V_{CC} – 1.45	
			85°C	V_{CC} – 1.85		V_{CC} – 1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} - 2 V, See Figure 3	-40°C, 25°C, 85°C	600			mV

AC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V or LVECL/LVPECL input V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Differential propagation delay CLKn, $\overline{CLKn}$ to all Q0, $\overline{Q0}$… Q9, $\overline{Q9}$	See [D]	200		350	ps
$t_{sk(o)}$	Output-to-output skew	See [A], [D] and Figure 1		15	30	ps
$t_{sk(pp)}$	Part-to-part skew	See [B], [D] and Figure 1			70	ps
t_{aj}	Additive phase jitter	Integration bandwidth of 20 kHz to 20 MHz, fout = 125 MHz at 25°C[C]		0.04	< 0.8	ps
$f_{(max)}$	Maximum frequency	Functional up to 3.5 GHz, see Figure 3			3500	MHz
t_r/t_f	Output rise and fall time (20%, 80%)	See [D]	90		200	ps



A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9).

B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) across multiple devices or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9) across multiple devices.

C. Typical value measured at ambient when clock input is 155.52MHz for an integration bandwidth of 20kHz to 5MHz.

D. Input conditions: V_{CM} = 1 V, V_{ID} = 0.5 V and F_{IN} = 1GHz.

Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

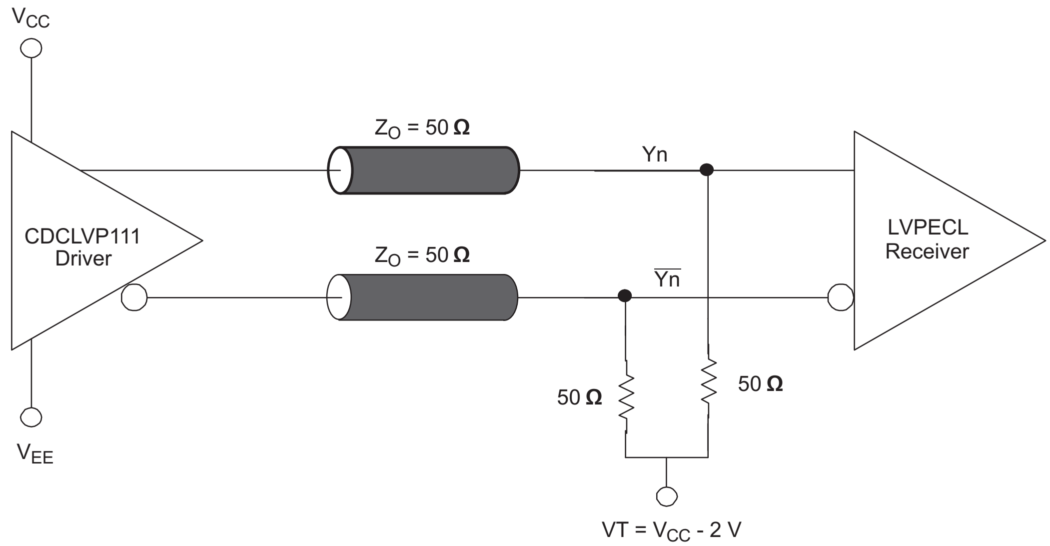


Figure 2. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number SCAA056)

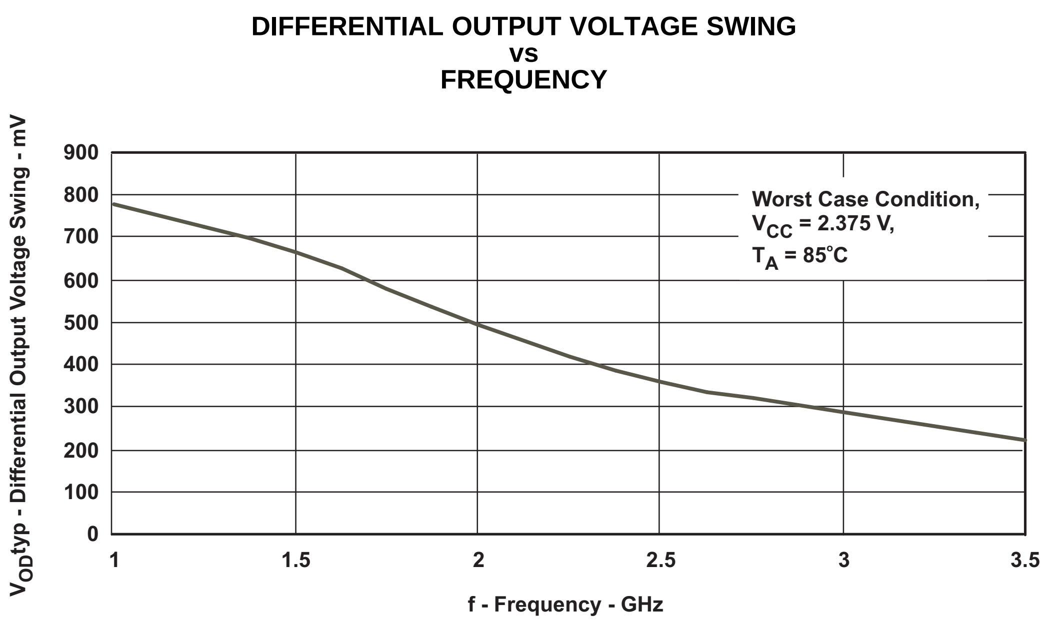


Figure 3. LVPECL Input Using CLK0 Pair, V_{CM} = 1 V, V_{ID} = 0.5 V

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CDCLVP111RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCLVP111RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCLVP111VF	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCLVP111VFR	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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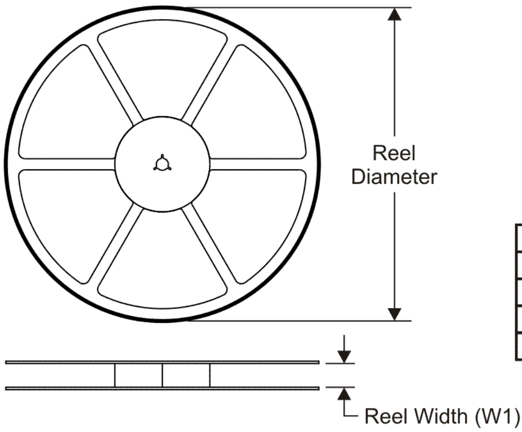
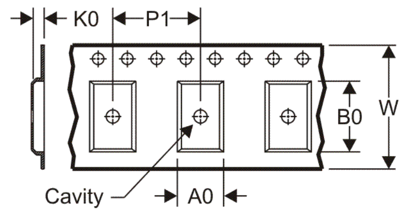
TAPE AND REEL INFORMATION

REEL DIMENSIONS

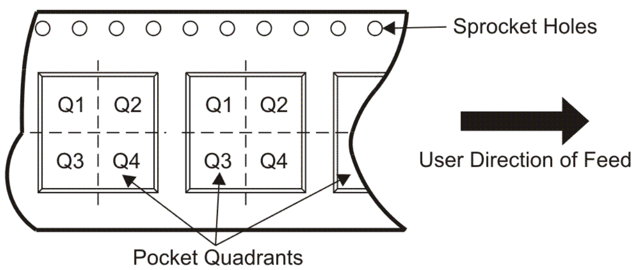


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

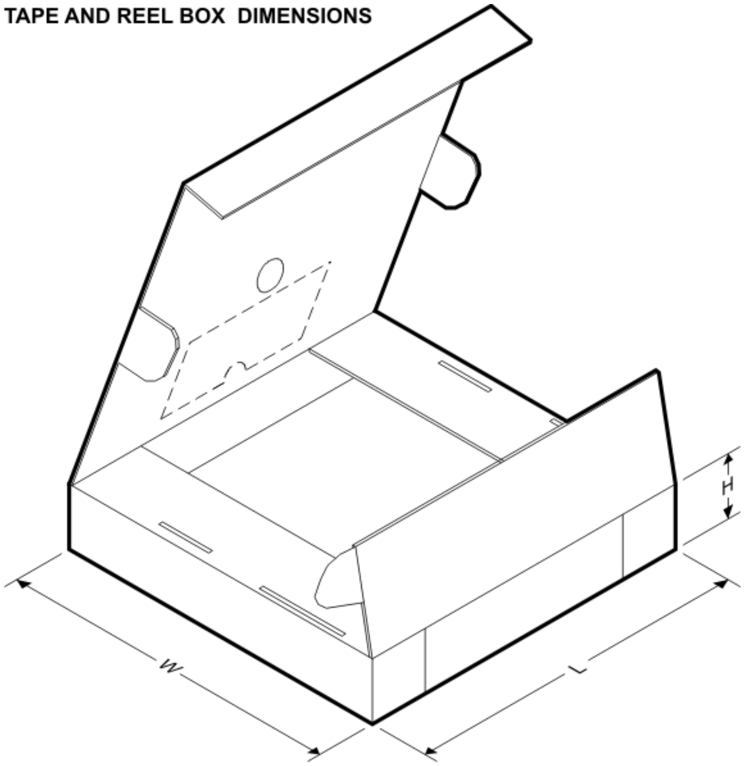
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP111RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVP111RHBT	QFN	RHB	32	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVP111VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

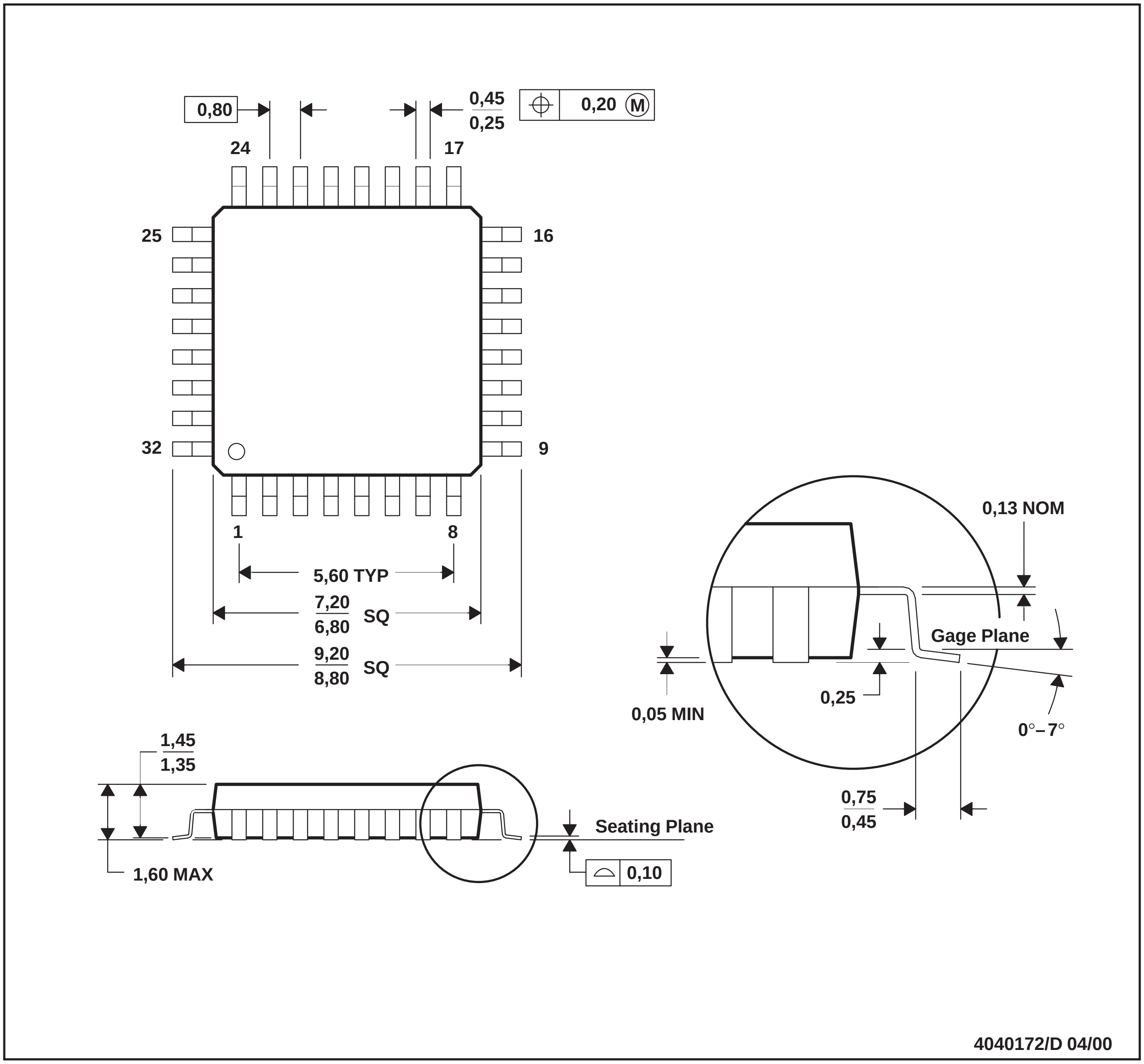
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

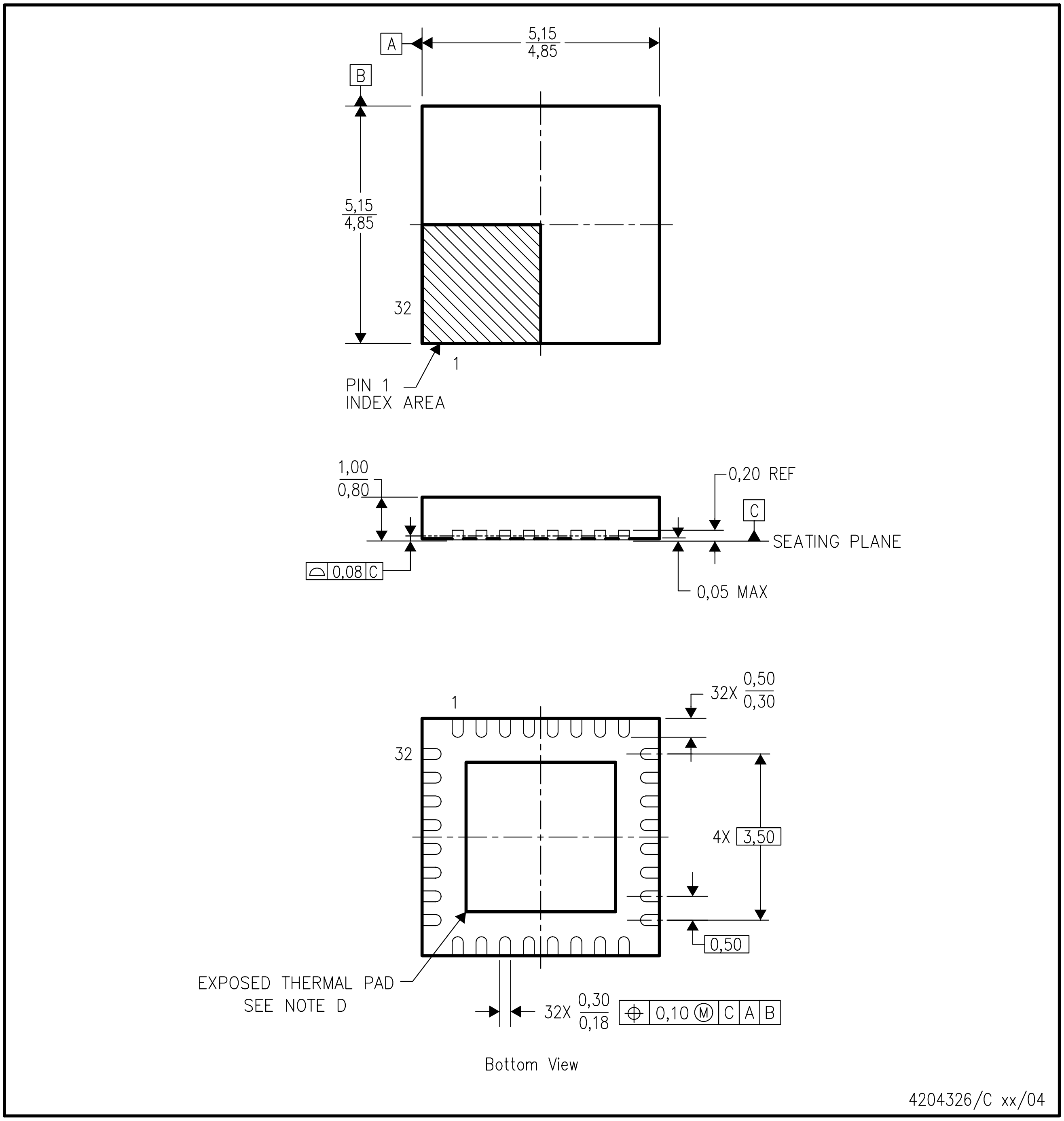
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP111RHBR	QFN	RHB	32	3000	340.5	333.0	20.6
CDCLVP111RHBT	QFN	RHB	32	250	340.5	333.0	20.6
CDCLVP111VFR	LQFP	VF	32	1000	333.2	345.9	28.6

VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



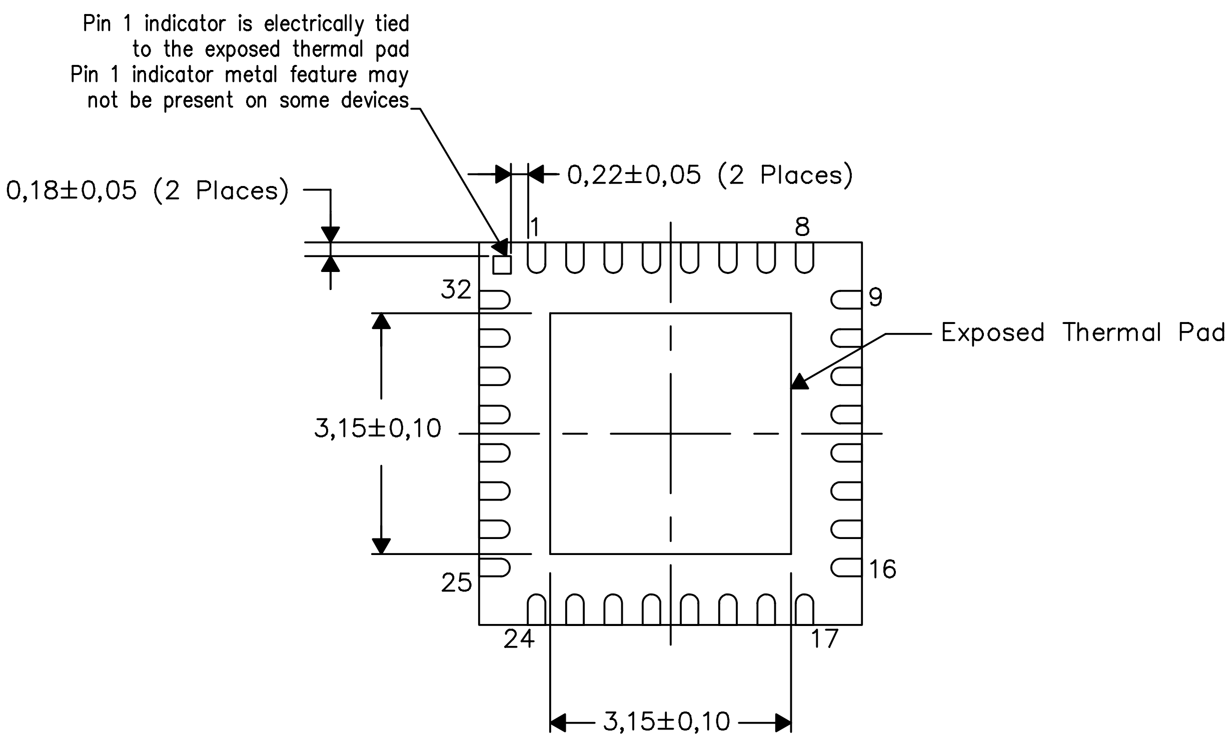
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

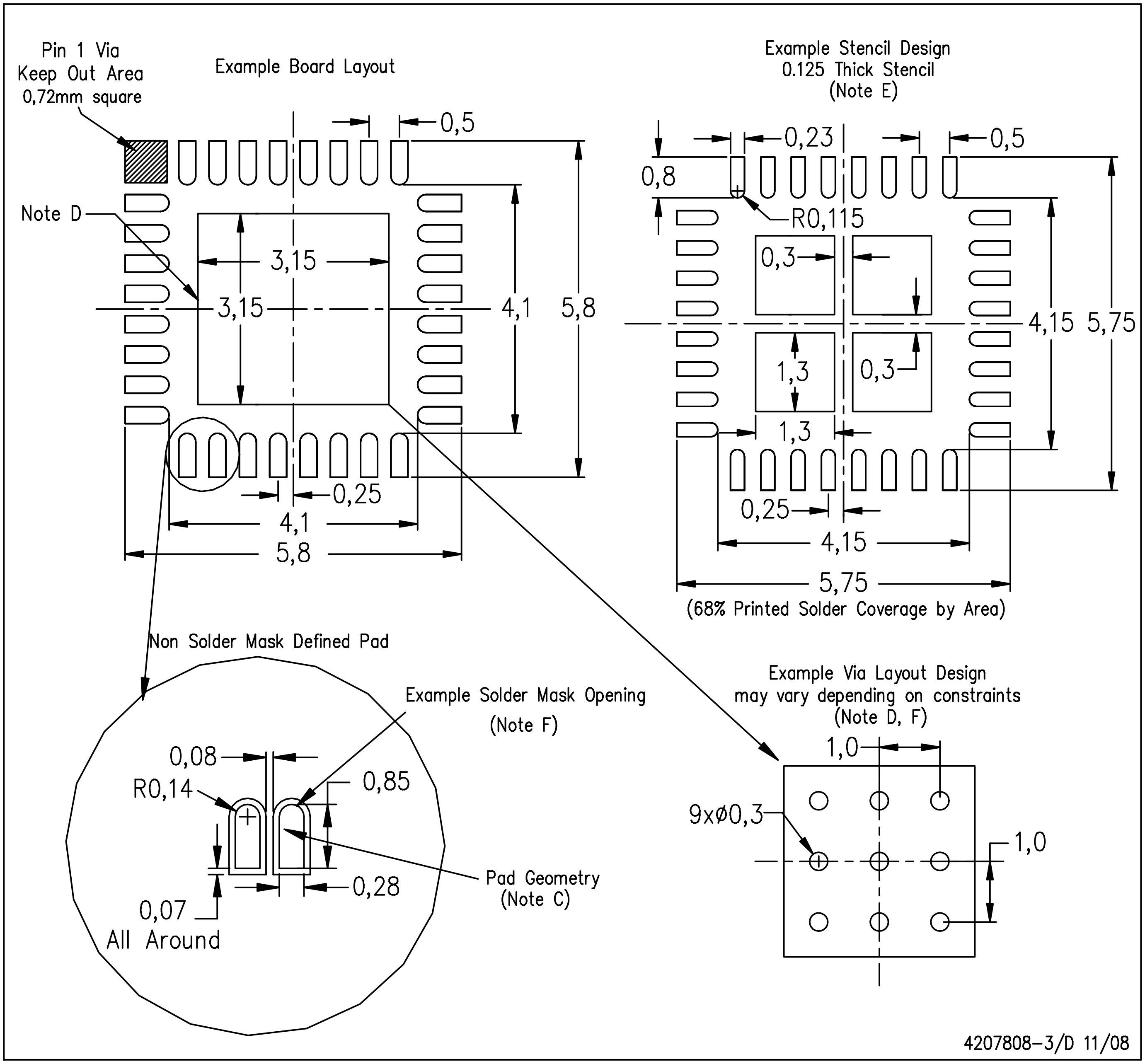


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S-PQFP-N32)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Power Mgmt	power.ti.com	Security	www.ti.com/security
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