

User's Guide SLAU299-November 2009

# SC70 DAC EVM

This document describes the setup and operation of the SC70 DAC Evaluation Module (EVM). It also discusses the DAC eXerciser Program, a software tool used with the SC70 DAC EVM. Included are the EVM schematic, bill of materials, and board layout.

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#### 1 **EVM Overview**

TEXAS INSTRUMENTS

### 1.1 Features

- Full-featured evaluation board for a variety of single-channel, 6-pin SC70 DAC, 6- to 14-bit, serial input, digital-to-analog converters
- Onboard reference and buffer circuits
- High-speed serial interface
- Modular design for use with a variety of DSP and SC70 DAC controller interface boards

# 1.2 Introduction

The SC70 DAC Evaluation Module is an evaluation board containing all the necessary components to evaluate the 6-pin, SC70 series of high-performance, digital-to-analog converters from Texas Instruments. The EVM is designed so that a single printed-circuit board (PCB) supports the entire family of high-speed, 12- and 16-bit serial DACs.

The modular EVM form factor allows for direct evaluation of the DAC's performance and operating characteristics. This EVM is compatible with the 5-6K Interface Board (SLAU104) from Texas Instruments as well as the HPA-MCU Interface Board (SLAU106). As part of a SC70 DACEVM-PDK kit, this EVM is supported on the DXP Platform using the modular motherboard MMB0.

# 2 Analog Interface

For maximum flexibility, the SC70 DAC evaluation module (EVM) is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J2 (Table 1). This header/socket provides access to the analog input pins of the ADC. Consult Samtec at <a href="http://www.samtec.com">www.samtec.com</a>, or call 1-800-SAMTEC-9 for a variety of mating connector options.

### Features:

- Full-featured evaluation board for a variety of single-channel, 6-pin SC70 DAC, 6- to 14-bit, serial input, digital-to-analog converters
- Onboard reference and buffer circuits
- High-speed serial interface
- Modular design for use with a variety of DSP and SC70 DAC controller interface boards

Pin Number	Signal	Description
J2.2	DAC OUT_A12	Single DAC out option via JP3
J2.4	Unused	
J2.6	Unused	
J2.8	DAC OUT_A2	Single DAC out option via JP3
J2.10	Unused	
J2.12	Unused	
J2.14	Unused	
J2.16	Unused	
J2.18	REF(-)	Unused
J2.20	REF(+)	External reference source input (2.5 V nominal, 2.525 V maximum)
J2.15	Unused	
J2.1–J2.19 (odd)	AGND	Analog ground connections (except J2.15)

### Table 1. Analog Interface



# 3 Digital Interface

The SC70 DAC EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J1. This header/socket provides access to the digital control and serial data pins of the SC70 DAC EVM. Consult Samtec at <u>www.samtec.com</u> or 1-800-SAMTEC-9 for a variety of mating connector options.

Pin Number	Signal	Description
J1.1	CS	Active-low input to SYNC enables data transfer – jumper configurable (see schematic) via JP1
J1.3	SCLK	Serial clock
J1.5	SCLK(R)	Serial clock return (for DSP host systems)
J1.7	FS	Frame synchronization for DSP host systems – default SYNC input through JP1 (see schematic)
J1.9	FS(R)	Frame synchronization return (for DSP host systems)
J1.11	DX	Serial data input
J1.13	DR	Serial data return (for DSP host systems)
J1.4		
J1.10	GND	System (EVM) ground
J1.18		

# **Table 2. Digital Control**

# 4 **Power Supplies**

The SC70 DAC EVM board requires a single, +5-VDC power supply for proper operation. This 5-V supply powers the voltage reference (U2) and the external reference buffer (U3). When used in combination with one of the DAP interface boards, J3 provides connection to the common power bus described in document <u>SLAA185</u>. Table 3 shows the pinout of J3.

# Table 3. J3 Power Input

Signal	Pin Nu	ımber	Signal
Unused	1	2	Unused
+5VA	3	4	Unused
GND	5	6	GND
Unused	7	8	Unused
Unused	9	10	Unused

When power is supplied to J3, JP2 allows for one of two different DC voltages to be applied to the DAC installed on the EVM. Review the schematic and PCB silkscreen for details.

# 4.1 DAC Power

JP2 allows the user to select the power supply used by the DAC installed in position U1 on the EVM. The series of DACs supported on this EVM use a single input as both power and reference voltages. When JP2 is in the default factory position (shunt on pins 1-2), power to the DAC comes from a precision 4.096-V reference. When the shunt on JP2 is moved to pins 2-3, the user may apply an external power/reference source to the DAC via J2 pin 20.

Digital Interface



EVM Operation

### 4.2 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied directly to J3 pin 3 referenced to pin 5. Optimal performance of the EVM requires a clean, well-regulated power source.

### CAUTION

The DACs that are compatible with this EVM have a variety of power supply requirements. Check the appropriate data sheets, and verify all power supplies are within the safe operating limits of the converter before applying power to the EVM.

# 5 EVM Operation

# 5.1 Analog Output

The analog output from the EVM is applied directly to J2 (top or bottom side) via jumper JP3. The default condition of the jumper has a shunt placed between pins 1-2, which applies the analog output to J2 pin 2. Moving the shunt on JP3 to cover pins 2-3 applies the analog output to J2 pin 10.

# 5.2 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The SC70 DAC EVM can also be connected directly to a DSP or microcontroller capable of supplying the necessary serial control inputs. Visit the product folder for the EVM or the installed device for a current list of compatible interface and/or accessory boards.

# 5.3 SYNC

Jumper JP1 is provided to allow the source selection of the signal applied to the SYNC input of the DAC installed on the EVM. The factory default condition for the EVM is to place a shunt jumper between pins 1-2 of JP1. This allows the Frame Sync (FS) signal from DSP host systems to be used as the SYNC input to the DAC. This signal originates from J1.7. When the shunt on JP1 is moved to pins 2-3, a GPIO input applied via J1.1 can be used to control the SYNC input to the DAC. This feature allows the possibility of sharing the SPI bus with up to two SC70 DAC EVMs by stacking the boards together.

### 5.4 Default Jumper Locations

Table 4 provides a list of jumpers found on the EVM and their factory default conditions.

Jumper	Shunt Position	Jumper Description
JP1	Pins 1-2	Controls SYNC (default is J1.7)
JP2	Pins 1-2	Controls DAC power/reference (default is U2, 4.096 V)
JP3	Pins 1-2	Controls analog output voltage (default is J2.2)

# Table 4. EVM Default Jumper Settings

# 6 Using the SC70 DAC EVM With DXP

The SC70 DAC EVM is compatible with the DAC eXerciser Program (DXP) from Texas Instruments. DXP is a tool that can generate the necessary control signals required to output various signals and waveforms from the device installed on the SC70 DAC EVM. The SC70 DAC EVM-PDK kit combines one of the DAC8411, DAC8311, DAC7311, DAC6311, or the DAC5311 EVM boards with the DSP-based modular motherboard MMB0. The kit includes the DXP software for evaluation using any available USB port on a Windows<sup>™</sup> XP-based computer.



DXP is a program for controlling the digital input signals such as the clock, SYNC, and SDI. Wave tables are built into the DSP software to allow Sine, Ramp, Triangle, and Square wave signals to be generated by the SC70 DAC. Straight DC outputs can also be obtained.

The SC70 DAC EVM-PDK is controlled by loading a DAC EVM configuration into the MMB0. For complete information about installing and configuring DXP, see the *DXP User's Guide*, available for download from the TI Web site. This section covers the specific operation of the SC70 DAC EVM-PDK.

# 6.1 Hardware

The hardware consists of two main components: the first is the SC70 DAC EVM itself and the other is a modular motherboard called the MMB0. The MMB0 board houses a TMS320VC5507 DSP which controls the serial interface to the device loaded on the EVM board.

The hardware needs to be configured such that the SC70 DAC EVM is plugged onto the MMB0 aligning female connectors P1, P2, and P3 (bottom side of the SC70 DAC EVM) with male connectors J4, J7, and J5 on the MMB0.

### CAUTION

Exercise caution when assembling the SC70 DAC EVM and MMB0 boards as it is possible to misalign the connectors.

Do not connect the MMB0 to your PC before installing the DXP software as described in the DXP User's Guide. Installing the software ensures that the necessary drivers are properly loaded to run the hardware.



Figure 1. MMB0 With SC70 DACEVM Installed (NEEDS REPLACING)



# 6.2 MMB0 Power Supplies

Several power connections are required for the hardware to work properly. For the MMB0, the supplied 6-V AC/DC converter is all that is necessary. Ensure that J12 on the MMB0 board is closed before connecting the AC/DC adapter to the DC In connector of the MMB0. This supply provides all power to the digital portion of the SC70 DAC EVM as well as all necessary power for the DSP. Clean, well-regulated analog power for the SC70 DAC EVM must be supplied externally via J14 – a 6-position screw terminal mounted in the lower left corner of the MMB0 board.

# CAUTION

When using external power supplies applied to J14 on the MMB0, ensure that all shorting blocks from J13 are completely removed. Permanent damage to the MMB0 may occur otherwise.

From left to right, the J14 screw terminal connections are –VA, +VA, +5VA, -5VA, +5VD, and GND. The SC70 DAC board has power requirements as described in Section 4. The analog +5VA may be applied directly to the screw terminals at J14 on the MMB0 (referenced to the GND terminal).

For convenience to the SC70 DAC EVM user, the +5VA required for the analog power to the EVM may be provided through the MMB0. This can be accomplished by placing a shunt jumper on J13B (+5 to +5VA), which connects the digital 5-V supply to the analog supply input. Due to switching noise, overall performance of the device installed on the EVM may be compromised.

# 6.3 Software – Running DXP

Install DXP on a laptop or personal computer running Windows XP as per the detailed instruction in the DXP User's Guide (<u>SBAU146</u>). Run the DXP program by clicking on the DXP icon on your desktop, or by browsing to your installation directory.

Before you can generate signals with DXP, a DAC EVM configuration file must be loaded. To load a configuration file, select the desired DAC from the configuration list under the DAC menu. Choose the DAC configuration file for the device installed on the EVM as shown in Figure 2.



- DXP		_ <u> </u>
Eile DAC Help		
DAC9881	Connerte	
DAC8881		
DAC6832		Connected
DAC8581	Run DAC	
DAC8560		
DAC8411		
Rescan For Devices Ctrl+R		
Signal Type Sine	Simulate	
Data Format Two's Complement	$\nabla$	
Frequency		
0.01 1 100	1.000kHz	
Attenuation	- ~	
-70 -65 -60 -55 -50 -45 -40 -3	5 -30 -25 -20 -15 -10 -5 0	
	Offset Units	
Phase Offset Volt	s 2.500000V Volts 🗸	
Offset Code	s 0x000	
DAC Output Update Options		
Source Frame Sync	Update Rate 200,000kSP5	
L		

Figure 2. Loading a SC70 DAC EVM Configuration

The DXP software defaults to output a 1-kHz sine wave from the DAC; other waveform options include Square, Saw tooth, Triangle, and DC output options as described in the DXP User's Guide. The frequency and amplitude of the output waveform is controlled by sliders on the DXP interface. The DAC update rate can also be modified as shown in Figure 3.



Eile DAC Help	
DAC eXerciser Program Readys	select a device from "DAC" menu
DAC9881	
Digital Waveform Generation	GPIO-controlled DAC Functions
Signal Type Sine 🗸 Simulate	Reset INACTIVE
Data Format Straight Binary 🗸	Power-down INACTIVE
Frequency 0.01 1 100 10000 500000	
Attenuation	
Phase     Offset Volts     2.500000V     Offset Units       0     Offset Codes     0x20000	
DAC Output Update Options	
Source Frame Sync  Update Rate 1.000MSPS	

Figure 3. SC70 DAC EVM – Frequency/Amplitude and Update Rate Adjustments

# 6.4 DAC Output Update Options

The DXP software also allows the user to choose several DAC output update options. These are shown in Figure 4.

-DAC C	Output Update Options			
Source	✓ Frame Sync Latch Pin with DSP Timer	Update Rate	1.000MSPS	
	Latch Pin with External Source			

Figure 4. DAC Output Update Options

Details on these options are shown in Table 5.

# **Table 5. Output Update Features**

Options	Detailed Description
Frame Sync	The DXP software defaults to Frame Sync update mode. In this mode, the SYNC input of the DAC loaded on the EVM is controlled by the Frame Sync output of the MMB0. JP1 on the SC70 DAC EVM must be shorted pins 1-2 to use this option.
Latch with DSP Timer	N/A
Latch with External Timer	N/A
Update Rate	User Input – enter the desired DAC update rate, 1MSPS is the default

# 7 Bill of Materials and EVM Schematic

The following table contains a complete bill of materials for the SC70 DAC EVM. The schematic diagram is also provided for reference.

# 7.1 Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1, C2	0.1 µF, 0603, Ceramic, 50V, X7R, 10%	Murata	GRM188R71H104KA93D
C3	0.47 µF, 0603, Ceramic, 25V, X7R, 10%	Murata	GRM188R71E474KA12D
C4, C6	1 µF, 0603, Ceramic, 16V, X5R, 10%	TDK	C1608X5R1C105K
C5	10 µF, 0805, Ceramic, 10V, X5R, 10%	Taiyo Yuden	LMK212BJ106KD-T
C7	10 µF, 0603, Ceramic, 6.3V, X5R, 20%	TDK	C1608X5R0J106M
J1 J2 (Top Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
J3 (Top Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
J1 J2 (Bottom Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
J3 (Bottom Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
JP1, JP2, JP3	3 Pin 0.1inch, Header	Samtec	TSW-103-07-T-S
R1	NI		
R2	10 kΩ, 0603, 1/10W, 1%	Yageo	RC0603FR-0710KL
R3, R4, R8, R9, R10	NI		
R5, R6, R7, R11	0 Ω, 0603, 1/10W, 5%	Yageo	RC0603JR-070RL
R12	1.5 Ω, 0603, 1/10W, 5%	Yageo	RC0603JR-071R5L
TP1	TEST POINT PC MINI 0.040" D RED	Keystone	5000
TP2, TP3	TEST POINT PC MINI 0.040" D BLACK	Keystone	5001
U1	Various – See <sup>(1)</sup>	TI	Various
U2	IC PREC V-REF 4.096V LN 8-SOIC	TI	REF5040AID
U3	IC OPAMP GP R-R 44MHZ SOT23-5	TI	OPA353NA/250

<sup>(1)</sup> The device installed at location U1 is dependent on the EVM ordered. This device is soldered to the board for best performance. U1 may be replaced with any device listed in the EVM Compatible Device Data Sheets table found at the end of this document.

# 7.2 EVM Schematic

The SC70 DAC EVM schematic appears on the last page of this document.



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	DE)/	Revision History	
	REV	ECN Number Ap	proved
	I	I I	
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		INSTRUMENTS	
	Title:	12500 TI Boulevard. Dallas, Texas 7524	3
		SC70-6 DAC EVM	
	DOCUMEN <sup>®</sup>	CONTROL # 6498629	/: A
2.Sch	DATE: 5-	Nov-2009 SIZE: SHEET: 1 O	F: 1
_		6	



# 8 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through the TI Web site at www.ti.com

# **EVM-Compatible Device Data Sheets:**

- 1. DAC5311, DAC6311, DAC7311, 1.8V to 5.5V, 80µA, 8-, 10-, 10-, and 12-Bit, Low-Power, Single-Channel, Digital-to-Analog Converters in SC70 Package (SBAS442)
- 2. DAC8311, 1.8V to 5.5V, 80µA, DAC8411, 14- and 16-Bit, Low-Power, Single-Channel, Digital-to-Analog Converters in SC70 Package (SBAS439)

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### **EVM Warnings and Restrictions**

It is important to operate this EVM within the input voltage range of 0 V to 5 V and the output voltage range of 0 V to 5 V. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are

questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 32° C. The EVM is designed to operate properly with certain components above 32° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Power Mgmt	power.ti.com	Security	www.ti.com/security
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