# STEPPER MOTOR CONTROLLER IC

**Check for Samples: DRV8824**

## FEATURES

- **PWM Microstepping Motor Driver**
  - **Built-In Microstepping Indexer**
  - **Five-Bit Winding Current Control Allows Up to 32 Current Levels**
  - **Low MOSFET On-Resistance**
- **1.6-A Maximum Drive Current at 24 V, 25°C**
- **Built-In 3.3-V Reference Output**
- **8.2-V to 45-V Operating Supply Voltage Range**
- **Thermally Enhanced HTSSOP and QFN Surface Mount Packages**

## APPLICATIONS

- **Automatic Teller Machines**
- **Money Handling Machines**
- **Video Security Cameras**
- **Printers**
- **Scanners**
- **Office Automation Machines**
- **Gaming Machines**
- **Factory Automation**
- **Robotics**

## DESCRIPTION

The DRV8824 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers and a microstepping indexer, and is intended to drive a bipolar stepper motor. The output driver block for each consists of N-channel power MOSFET's configured as full H-bridges to drive the motor windings. The DRV8824 is capable of driving up to 1.6-A of output current (with proper heatsinking, at 24 V and 25°C).

A simple step/direction interface allows easy interfacing to controller circuits. Pins allow configuration of the motor in full-step up to 1/32-step modes. Decay mode is programmable.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout and overtemperature.

The DRV8824 is available in a 28-pin HTSSOP package with PowerPAD™ and in a 28-pin QFN package PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

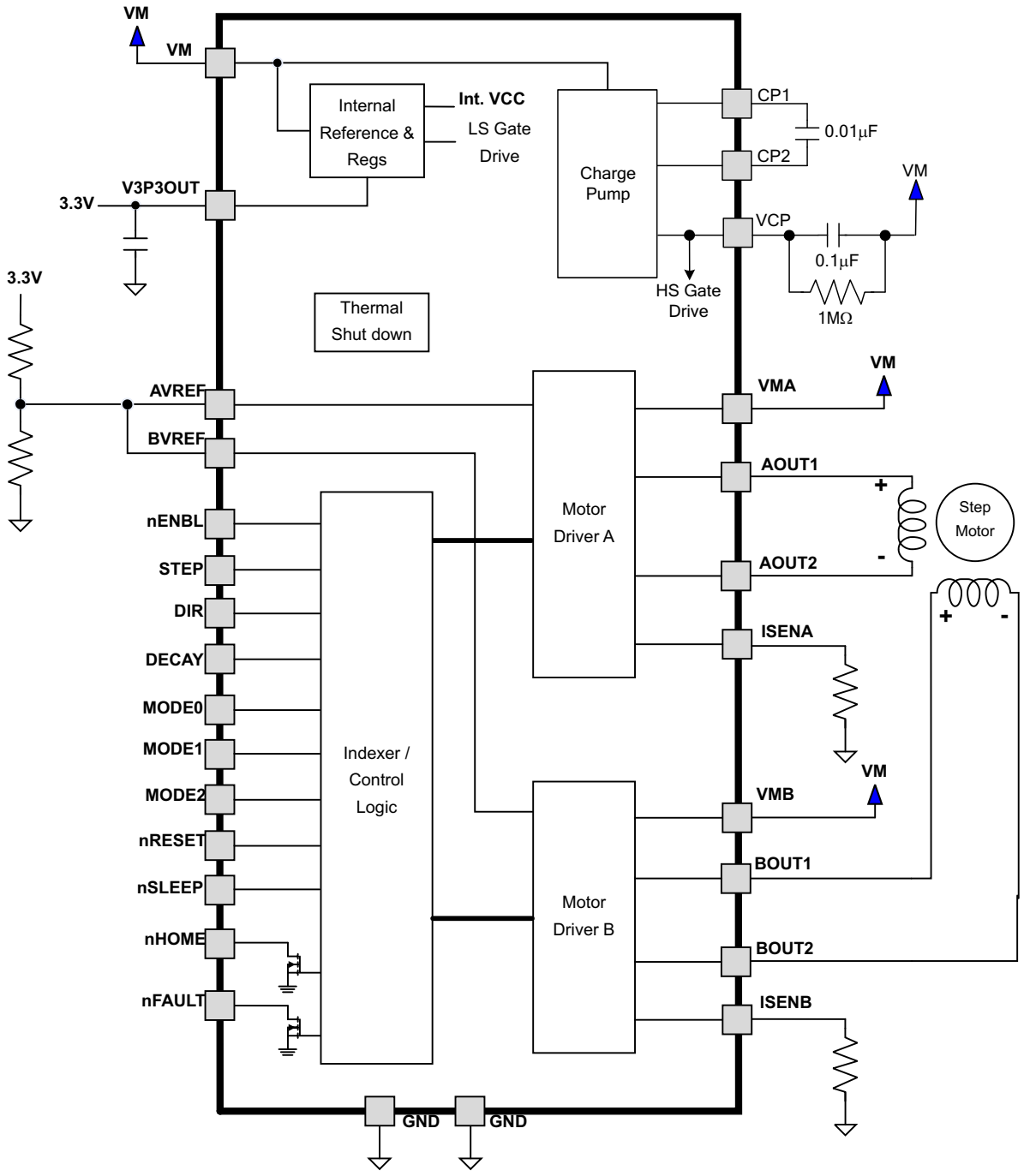
**ORDERING INFORMATION(1)**

| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PowerPAD™ (HTSSOP) - PWP | Reel of 2000 | DRV8824PWPR | DRV8824 |
| | | Tube of 50 | DRV8824PWP | |
| | PowerPAD™ (QFN) - RHD | Reel of 3000 | DRV8824RHDR | |
| | | Reel of 250 | DRV8824RHDT | |

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## DEVICE INFORMATION

### Functional Block Diagram

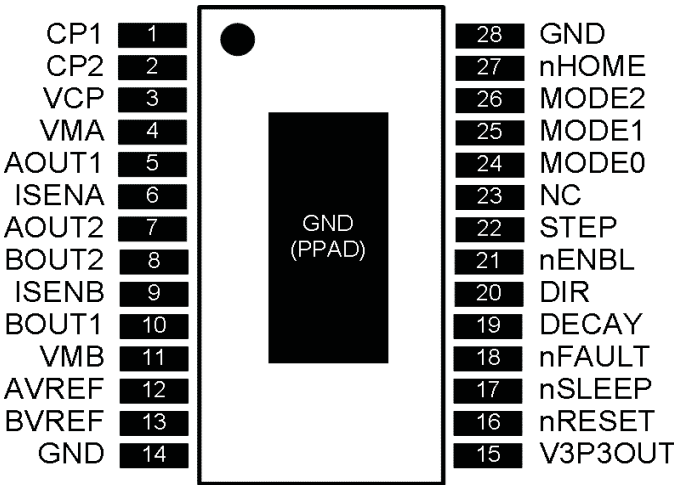


## Table 1. TERMINAL FUNCTIONS

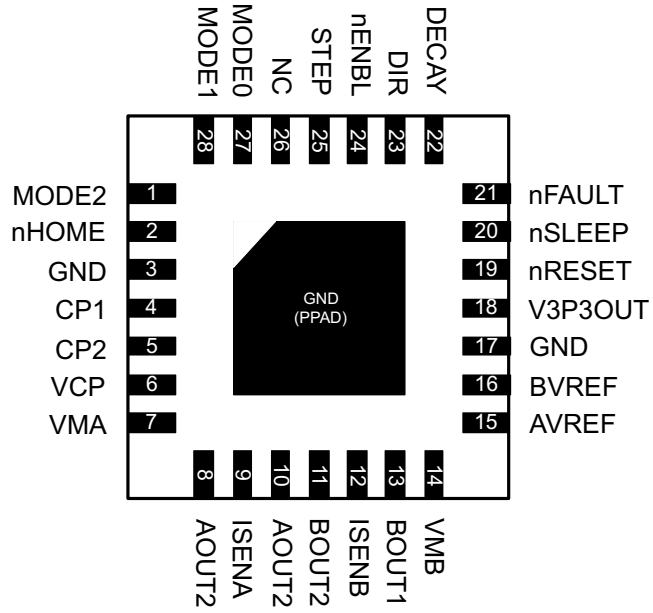
| NAME | PIN | | I/O[1] | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|---|
| | PWP | RHD | | | |
| **POWER AND GROUND** | | | | | |
| GND | 14, 28 | 3, 17 | - | Device ground | |
| VMA | 4 | 7 | - | Bridge A power supply | Connect to motor supply (8.2 V - 45 V). Both pins must be connected to same supply. |
| VMB | 11 | 14 | - | Bridge B power supply | |
| V3P3OUT | 15 | 18 | O | 3.3-V regulator output | Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF. |
| CP1 | 1 | 4 | IO | Charge pump flying capacitor | Connect a 0.01-µF 50-V capacitor between CP1 and CP2. |
| CP2 | 2 | 5 | IO | Charge pump flying capacitor | |
| VCP | 3 | 6 | IO | High-side gate drive voltage | Connect a 0.1-µF 16-V ceramic capacitor and a 1-MΩ resistor to VM. |
| **CONTROL** | | | | | |
| nENBL | 21 | 24 | I | Enable input | Logic high to disable device outputs and indexer operation, logic low to enable. Internal pulldown. |
| nSLEEP | 17 | 20 | I | Sleep mode input | Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown. |
| STEP | 22 | 25 | I | Step input | Rising edge causes the indexer to move one step. Internal pulldown. |
| DIR | 20 | 23 | I | Direction input | Level sets the direction of stepping. Internal pulldown. |
| MODE0 | 24 | 27 | I | Microstep mode 0 | MODE0 - MODE2 set the step mode - full, 1/2, 1/4, 1/8/ 1/16, or 1/32 step. Internal pulldown. |
| MODE1 | 25 | 28 | I | Microstep mode 1 | |
| MODE2 | 26 | 1 | I | Microstep mode 2 | |
| DECAY | 19 | 22 | I | Decay mode | Low = slow decay, open = mixed decay, high = fast decay. Internal pulldown and pullup. |
| nRESET | 16 | 19 | I | Reset input | Active-low reset input initializes the indexer logic and disables the H-bridge outputs. Internal pulldown. |
| AVREF | 12 | 15 | I | Bridge A current set reference input | Reference voltage for winding current set. Normally AVREF and BVREF are connected to the same voltage. Can be connected to V3P3OUT. A 0.01-µF bypass capacitor to GND is recommended. |
| BVREF | 13 | 16 | I | Bridge B current set reference input | |
| NC | 23 | 26 | | No connect | Leave this pin unconnected. |
| **STATUS** | | | | | |
| nHOME | 27 | 2 | OD | Home position | Logic low when at home state of step table |
| nFAULT | 18 | 21 | OD | Fault | Logic low when in fault condition (overtemp, overcurrent) |
| **OUTPUT** | | | | | |
| ISENA | 6 | 9 | IO | Bridge A ground / Isense | Connect to current sense resistor for bridge A. |
| ISENB | 9 | 12 | IO | Bridge B ground / Isense | Connect to current sense resistor for bridge B. |
| AOUT1 | 5 | 8 | O | Bridge A output 1 | Connect to bipolar stepper motor winding A. Positive current is AOUT1 → AOUT2 |
| AOUT2 | 7 | 10 | O | Bridge A output 2 | |
| BOUT1 | 10 | 13 | O | Bridge B output 1 | Connect to bipolar stepper motor winding B. Positive current is BOUT1 → BOUT2 |
| BOUT2 | 8 | 11 | O | Bridge B output 2 | |

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

**PWP PACKAGE**
**(TOP VIEW)**




**RHD PACKAGE**
**(TOP VIEW)**



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| VMx | Power supply voltage range | | –0.3 to 47 | V |
| | Digital pin voltage range | | –0.5 to 7 | V |
| VREF | Input voltage | | –0.3 to 4 | V |
| | ISENSEx pin voltage | | –0.3 to 0.8 | V |
| | Peak motor drive output current, t < 1 µS | | Internally limited | A |
| | Continuous motor drive output current(3) | | 1.6 | A |
| | ESD rating | HBD (human body model) | 2000 | V |
| | | CDM (charged device model) | 500 | |
| | Continuous total power dissipation | | See Thermal Information table | |
| $T_J$ | Operating virtual junction temperature range | | –40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | –60 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

## THERMAL INFORMATION

| THERMAL METRIC | | DRV8824 | | UNITS |
|---|---|---|---|---|
| | | PWP | RHD | |
| | | 28 PINS | 28 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(1) | 38.9 | 35.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(2) | 23.3 | 25.1 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(3) | 21.2 | 8.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(4) | 0.8 | 0.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(5) | 20.9 | 8.2 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(6) | 2.6 | 1.1 | |

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_M$ | Motor power supply voltage range(1) | 8.2 | | 45 | V |
| $V_{REF}$ | VREF input voltage(2) | 1 | | 3.5 | V |
| $I_{V3P3}$ | V3P3OUT load current | | | 1 | mA |

(1) All $V_M$ pins must be connected to the same supply voltage.
(2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range of -40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_{VM}$ | VM operating supply current | $V_M$ = 24 V, $f_{PWM}$ < 50 kHz | | 5 | 8 | mA |
| $I_{VMQ}$ | VM sleep mode supply current | $V_M$ = 24 V | | 10 | 20 | µA |
| $V_{UVLO}$ | VM undervoltage lockout voltage | $V_M$ rising | | 7.8 | 8.2 | V |
| **V3P3OUT REGULATOR** | | | | | | |
| $V_{3P3}$ | V3P3OUT voltage | IOUT = 0 to 1 mA, $V_M$ = 24 V, $T_J$ = 25°C | 3.18 | 3.30 | 3.42 | V |
| | | IOUT = 0 to 1 mA | 3.10 | 3.30 | 3.50 | |
| **LOGIC-LEVEL INPUTS** | | | | | | |
| $V_{IL}$ | Input low voltage | | | 0.6 | 0.7 | V |
| $V_{IH}$ | Input high voltage | | 2 | | 5.25 | V |
| $V_{HYS}$ | Input hysteresis | | | 0.45 | | V |
| $I_{IL}$ | Input low current | VIN = 0 | –20 | | 20 | µA |
| $I_{IH}$ | Input high current | VIN = 3.3 V | | | 100 | µA |
| $R_{PD}$ | Internal pulldown resistance | nENBL, nRESET, DIR, STEP, MODEx | | 100 | | kΩ |
| | | nSLEEP | | 1 | | MΩ |
| **nHOME, nFAULT OUTPUTS (OPEN-DRAIN OUTPUTS)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_O$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output high leakage current | $V_O$ = 3.3 V | | | 1 | µA |
| **DECAY INPUT** | | | | | | |
| $V_{IL}$ | Input low threshold voltage | For slow decay mode | | | 0.8 | V |
| $V_{IH}$ | Input high threshold voltage | For fast decay mode | 2 | | | V |
| $I_{IN}$ | Input current | | –100 | | 100 | µA |
| $R_{PU}$ | Internal pullup resistance | | | 130 | | kΩ |
| $R_{PD}$ | Internal pulldown resistance | | | 80 | | kΩ |
| **H-BRIDGE FETS** | | | | | | |
| $R_{DS(ON)}$ | HS FET on resistance | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 25°C | | 0.63 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 85°C | | 0.76 | 0.90 | |
| $R_{DS(ON)}$ | LS FET on resistance | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 25°C | | 0.65 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 85°C | | 0.78 | 0.90 | |
| $I_{OFF}$ | Off-state leakage current | | –20 | | 20 | µA |
| **MOTOR DRIVER** | | | | | | |
| $f_{PWM}$ | Internal PWM frequency | | | 50 | | kHz |
| $t_{BLANK}$ | Current sense blanking time | | | 3.75 | | µs |
| $t_R$ | Rise time | $V_M$ = 24 V | 100 | | 360 | ns |
| $t_F$ | Fall time | $V_M$ = 24 V | 80 | | 250 | ns |
| $t_{DEAD}$ | Dead time | | | 400 | | ns |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | | 1.8 | | 5 | A |
| $t_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | °C |
| **CURRENT CONTROL** | | | | | | |
| $I_{REF}$ | xVREF input current | xVREF = 3.3 V | –3 | | 3 | µA |
| $V_{TRIP}$ | xISENSE trip voltage | xVREF = 3.3 V, 100% current setting | 635 | 660 | 685 | mV |

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range of -40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\Delta I_{TRIP}$ | Current trip accuracy (relative to programmed value) | xVREF = 3.3 V , 5% current setting | –25 | | 25 | % |
| | | xVREF = 3.3 V , 10% - 34% current setting | –15 | | 15 | |
| | | xVREF = 3.3 V, 38% - 67% current setting | –10 | | 10 | |
| | | xVREF = 3.3 V, 71% - 100% current setting | –5 | | 5 | |
| $A_{ISENSE}$ | Current sense amplifier gain | Reference only | | 5 | | V/V |

## TIMING REQUIREMENTS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $f_{STEP}$ | Step frequency | | 250 | kHz |
| 2 | $t_{WH(STEP)}$ | Pulse duration, STEP high | 1.9 | | µs |
| 3 | $t_{WL(STEP)}$ | Pulse duration, STEP low | 1.9 | | µs |
| 4 | $t_{SU(STEP)}$ | Setup time, command to STEP rising | 200 | | ns |
| 5 | $t_{H(STEP)}$ | Hold time, command to STEP rising | 200 | | ns |
| 6 | $t_{ENBL}$ | Enable time, nENBL active to STEP | 200 | | ns |
| 7 | $t_{WAKE}$ | Wakeup time, nSLEEP inactive to STEP | 1 | | ms |

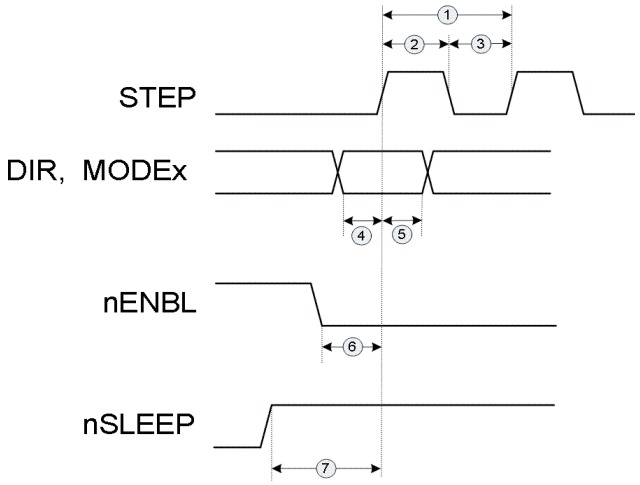



**Figure 1. Timing Diagram**

## FUNCTIONAL DESCRIPTION

### PWM Motor Drivers

The DRV8824 contains two H-bridge motor drivers with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 2.

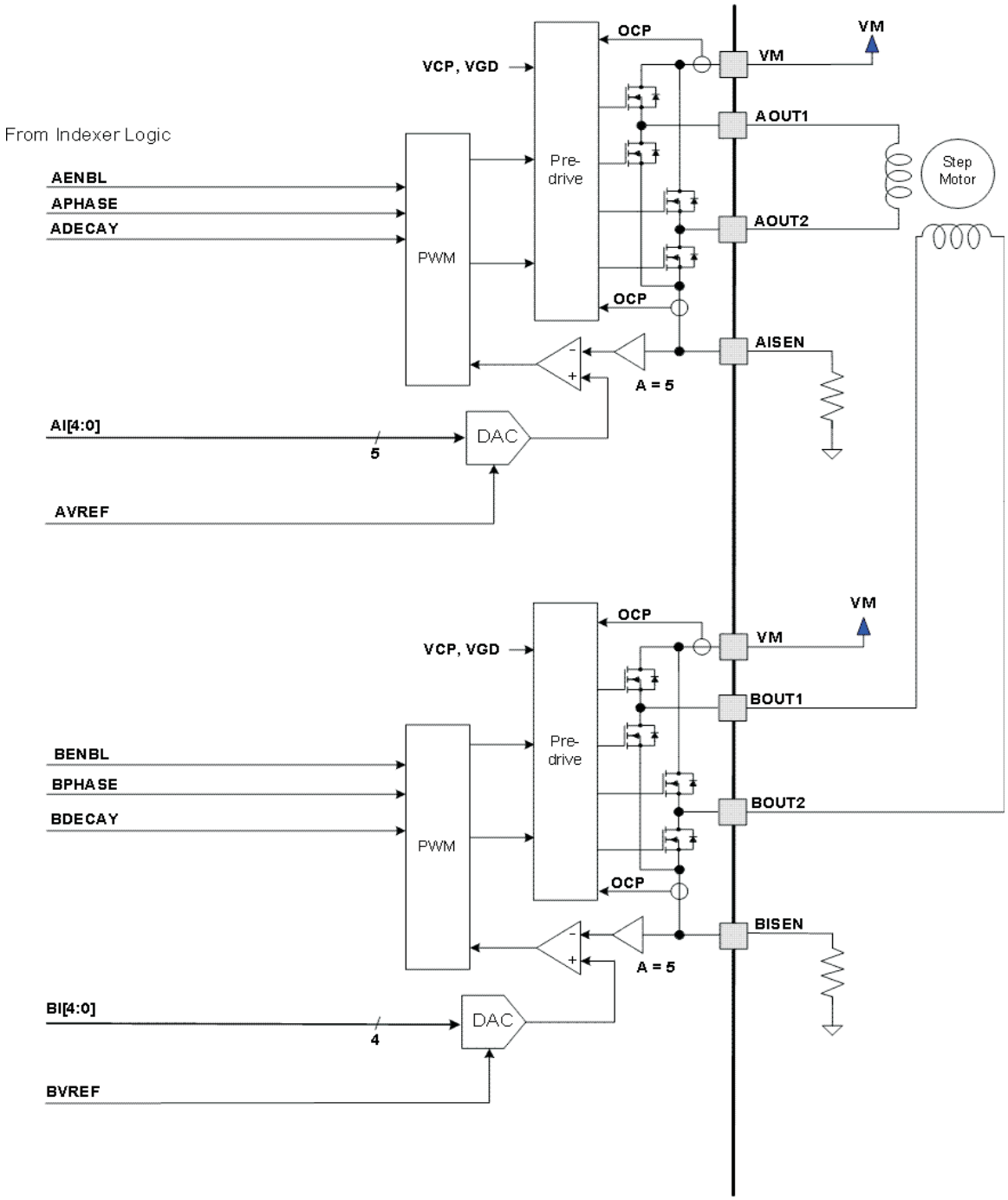



**Figure 2. Motor Control Circuitry**

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

## Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

In stepping motors, current regulation is used to vary the current in the two windings in a semi-sinusoidal fashion to provide smooth motion.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current will be 3.3 V / (5 x 0.5 Ω) = 1.32 A.

The reference voltage is scaled by an internal DAC that allows fractional stepping of a bipolar stepper motor, as described in the microstepping indexer section below.

## Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 3 as case 1. The current flow direction shown indicates positive current flow.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 3 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 3 as case 3.

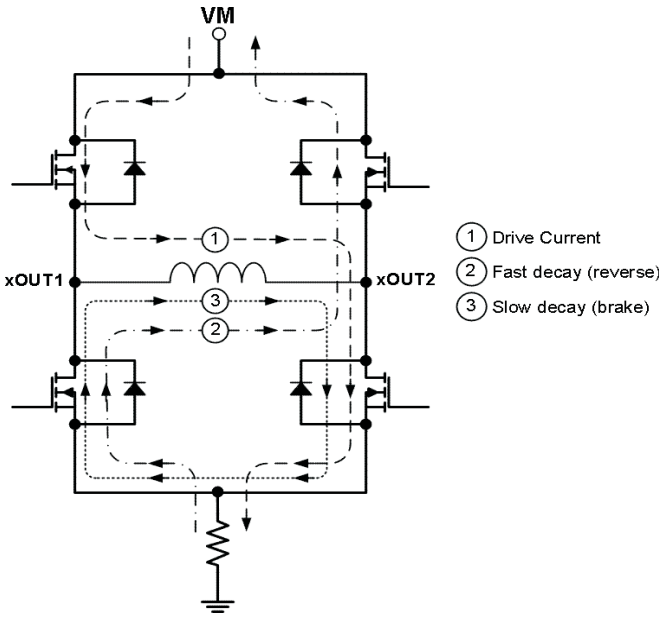



**Figure 3. Decay Mode**

The DRV8824 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period. This occurs only if the current through the winding is decreasing (per the indexer step table); if the current is increasing, then slow decay is used.

## Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

## Microstepping Indexer

Built-in indexer logic in the DRV8824 allows a number of different stepping configurations. The MODE0 - MODE2 pins are used to configure the stepping format as shown in Table 2.

**Table 2. Stepping Format**

| MODE2 | MODE1 | MODE0 | STEP MODE |
|---|---|---|---|
| 0 | 0 | 0 | Full step (2-phase excitation) with 71% current |
| 0 | 0 | 1 | 1/2 step (1-2 phase excitation) |
| 0 | 1 | 0 | 1/4 step (W1-2 phase excitation) |
| 0 | 1 | 1 | 8 microsteps / step |
| 1 | 0 | 0 | 16 microsteps / step |
| 1 | 0 | 1 | 32 microsteps / step |
| 1 | 1 | 0 | 32 microsteps / step |
| 1 | 1 | 1 | 32 microsteps / step |

Table 3 shows the relative current and step directions for different settings of MODEx. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that if the step mode is changed while stepping, the indexer will advance to the next valid state for the new MODEx setting at the rising edge of STEP.

The home state is 45°. This state is entered at power-up or application of nRESET. This is shown in Table 3 by the shaded cells. The logic inputs DIR, STEP, nRESET and MODEx have an internal pulldown resistors of 100 kΩ

**Table 3. Relative Current and Step Directions**

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | | 100% | 0% | 0 |
| 2 | | | | | | 100% | 5% | 3 |
| 3 | 2 | | | | | 100% | 10% | 6 |
| 4 | | | | | | 99% | 15% | 8 |
| 5 | 3 | 2 | | | | 98% | 20% | 11 |
| 6 | | | | | | 97% | 24% | 14 |
| 7 | 4 | | | | | 96% | 29% | 17 |
| 8 | | | | | | 94% | 34% | 20 |
| 9 | 5 | 3 | 2 | | | 92% | 38% | 23 |
| 10 | | | | | | 90% | 43% | 25 |

**Table 3. Relative Current and Step Directions (continued)**

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|---|---|---|---|---|---|---|---|---|
| 11 | 6 | | | | | 88% | 47% | 28 |
| 12 | | | | | | 86% | 51% | 31 |
| 13 | 7 | 4 | | | | 83% | 56% | 34 |
| 14 | | | | | | 80% | 60% | 37 |
| 15 | 8 | | | | | 77% | 63% | 39 |
| 16 | | | | | | 74% | 67% | 42 |
| 17 | 9 | 5 | 3 | 2 | 1 | 71% | 71% | 45 |
| 18 | | | | | | 67% | 74% | 48 |
| 19 | 10 | | | | | 63% | 77% | 51 |
| 20 | | | | | | 60% | 80% | 53 |
| 21 | 11 | 6 | | | | 56% | 83% | 56 |
| 22 | | | | | | 51% | 86% | 59 |
| 23 | 12 | | | | | 47% | 88% | 62 |
| 24 | | | | | | 43% | 90% | 65 |
| 25 | 13 | 7 | 4 | | | 38% | 92% | 68 |
| 26 | | | | | | 34% | 94% | 70 |
| 27 | 14 | | | | | 29% | 96% | 73 |
| 28 | | | | | | 24% | 97% | 76 |
| 29 | 15 | 8 | | | | 20% | 98% | 79 |
| 30 | | | | | | 15% | 99% | 82 |
| 31 | 16 | | | | | 10% | 100% | 84 |
| 32 | | | | | | 5% | 100% | 87 |
| 33 | 17 | 9 | 5 | 3 | | 0% | 100% | 90 |
| 34 | | | | | | –5% | 100% | 93 |
| 35 | 18 | | | | | –10% | 100% | 96 |
| 36 | | | | | | –15% | 99% | 98 |
| 37 | 19 | 10 | | | | –20% | 98% | 101 |
| 38 | | | | | | –24% | 97% | 104 |
| 39 | 20 | | | | | –29% | 96% | 107 |
| 40 | | | | | | –34% | 94% | 110 |
| 41 | 21 | 11 | 6 | | | –38% | 92% | 113 |
| 42 | | | | | | –43% | 90% | 115 |
| 43 | 22 | | | | | –47% | 88% | 118 |
| 44 | | | | | | –51% | 86% | 121 |
| 45 | 23 | 12 | | | | –56% | 83% | 124 |
| 46 | | | | | | –60% | 80% | 127 |
| 47 | 24 | | | | | –63% | 77% | 129 |
| 48 | | | | | | –67% | 74% | 132 |
| 49 | 25 | 13 | 7 | 4 | 2 | –71% | 71% | 135 |
| 50 | | | | | | –74% | 67% | 138 |
| 51 | 26 | | | | | –77% | 63% | 141 |
| 52 | | | | | | –80% | 60% | 143 |
| 53 | 27 | 14 | | | | –83% | 56% | 146 |
| 54 | | | | | | –86% | 51% | 149 |
| 55 | 28 | | | | | –88% | 47% | 152 |
| 56 | | | | | | –90% | 43% | 155 |

**Table 3. Relative Current and Step Directions (continued)**

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|---|---|---|---|---|---|---|---|---|
| 57 | 29 | 15 | 8 | | | –92% | 38% | 158 |
| 58 | | | | | | –94% | 34% | 160 |
| 59 | 30 | | | | | –96% | 29% | 163 |
| 60 | | | | | | –97% | 24% | 166 |
| 61 | 31 | 16 | | | | –98% | 20% | 169 |
| 62 | | | | | | –99% | 15% | 172 |
| 63 | 32 | | | | | –100% | 10% | 174 |
| 64 | | | | | | –100% | 5% | 177 |
| 65 | 33 | 17 | 9 | 5 | | –100% | 0% | 180 |
| 66 | | | | | | –100% | –5% | 183 |
| 67 | 34 | | | | | –100% | –10% | 186 |
| 68 | | | | | | –99% | –15% | 188 |
| 69 | 35 | 18 | | | | –98% | –20% | 191 |
| 70 | | | | | | –97% | –24% | 194 |
| 71 | 36 | | | | | –96% | –29% | 197 |
| 72 | | | | | | –94% | –34% | 200 |
| 73 | 37 | 19 | 10 | | | –92% | –38% | 203 |
| 74 | | | | | | –90% | –43% | 205 |
| 75 | 38 | | | | | –88% | –47% | 208 |
| 76 | | | | | | –86% | –51% | 211 |
| 77 | 39 | 20 | | | | –83% | –56% | 214 |
| 78 | | | | | | –80% | –60% | 217 |
| 79 | 40 | | | | | –77% | –63% | 219 |
| 80 | | | | | | –74% | –67% | 222 |
| 81 | 41 | 21 | 11 | 6 | 3 | –71% | –71% | 225 |
| 82 | | | | | | –67% | –74% | 228 |
| 83 | 42 | | | | | –63% | –77% | 231 |
| 84 | | | | | | –60% | –80% | 233 |
| 85 | 43 | 22 | | | | –56% | –83% | 236 |
| 86 | | | | | | –51% | –86% | 239 |
| 87 | 44 | | | | | –47% | –88% | 242 |
| 88 | | | | | | –43% | –90% | 245 |
| 89 | 45 | 23 | 12 | | | –38% | –92% | 248 |
| 90 | | | | | | –34% | –94% | 250 |
| 91 | 46 | | | | | –29% | –96% | 253 |
| 92 | | | | | | –24% | –97% | 256 |
| 93 | 47 | 24 | | | | –20% | –98% | 259 |
| 94 | | | | | | –15% | –99% | 262 |
| 95 | 48 | | | | | –10% | –100% | 264 |
| 96 | | | | | | –5% | –100% | 267 |
| 97 | 49 | 25 | 13 | 7 | | 0% | –100% | 270 |
| 98 | | | | | | 5% | –100% | 273 |
| 99 | 50 | | | | | 10% | –100% | 276 |
| 100 | | | | | | 15% | –99% | 278 |
| 101 | 51 | 26 | | | | 20% | –98% | 281 |
| 102 | | | | | | 24% | –97% | 284 |

**Table 3. Relative Current and Step Directions (continued)**

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|---|---|---|---|---|---|---|---|---|
| 103 | 52 | | | | | 29% | –96% | 287 |
| 104 | | | | | | 34% | –94% | 290 |
| 105 | 53 | 27 | 14 | | | 38% | –92% | 293 |
| 106 | | | | | | 43% | –90% | 295 |
| 107 | 54 | | | | | 47% | –88% | 298 |
| 108 | | | | | | 51% | –86% | 301 |
| 109 | 55 | 28 | | | | 56% | –83% | 304 |
| 110 | | | | | | 60% | –80% | 307 |
| 111 | 56 | | | | | 63% | –77% | 309 |
| 112 | | | | | | 67% | –74% | 312 |
| 113 | 57 | 29 | 15 | 8 | 4 | 71% | –71% | 315 |
| 114 | | | | | | 74% | –67% | 318 |
| 115 | 58 | | | | | 77% | –63% | 321 |
| 116 | | | | | | 80% | –60% | 323 |
| 117 | 59 | 30 | | | | 83% | –56% | 326 |
| 118 | | | | | | 86% | –51% | 329 |
| 119 | 60 | | | | | 88% | –47% | 332 |
| 120 | | | | | | 90% | –43% | 335 |
| 121 | 61 | 31 | 16 | | | 92% | –38% | 338 |
| 122 | | | | | | 94% | –34% | 340 |
| 123 | 62 | | | | | 96% | –29% | 343 |
| 124 | | | | | | 97% | –24% | 346 |
| 125 | 63 | 32 | | | | 98% | –20% | 349 |
| 126 | | | | | | 99% | –15% | 352 |
| 127 | 64 | | | | | 100% | –10% | 354 |
| 128 | | | | | | 100% | –5% | 357 |

## nRESET, nENBLE and nSLEEP Operation

The nRESET pin, when driven active low, resets internal logic, and resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while nRESET is active.

The nENBL pin is used to control the output drivers and enable/disable operation of the indexer. When nENBL is low, the output H-bridges are enabled, and rising edges on the STEP pin are recognized. When nENBL is high, the H-bridges are disabled, the outputs are in a high-impedance state, and the STEP input is ignored.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before applying a STEP input, to allow the internal circuitry to stabilize.

The nRESET and nENABLE pins have internal pulldown resistors of 100 kΩ. The nSLEEP pin has an internal pulldown resistor of 1 MΩ.

## Protection Circuits

The DRV8824 is fully protected against undervoltage, overcurrent and overtemperature events.

### Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the $I_{SENSE}$ resistor value or VREF voltage.

### Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

### Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when $V_M$ rises above the UVLO threshold.

## THERMAL INFORMATION

### Thermal Protection

The DRV8824 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### Power Dissipation

Power dissipation in the DRV8824 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 2.

$$P_{TOT} = 4 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (2)$$

where $P_{TOT}$ is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. It can be seen that the heatsink effectiveness increases rapidly to about 20 $cm^2$, then levels off somewhat for larger areas.

## REVISION HISTORY

| Changes from Revision G (August 2013) to Revision H | Page |
|---|---|
| • Changed in ELECTRICAL CHARACTERISTICS table, section DECAY INPUT 3rd row | 6 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8824PWP | ACTIVE | HTSSOP | PWP | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | DRV8824 | Samples |
| DRV8824PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | DRV8824 | Samples |
| DRV8824RHDR | ACTIVE | VQFN | RHD | 28 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV8824 | Samples |
| DRV8824RHDT | ACTIVE | VQFN | RHD | 28 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV8824 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

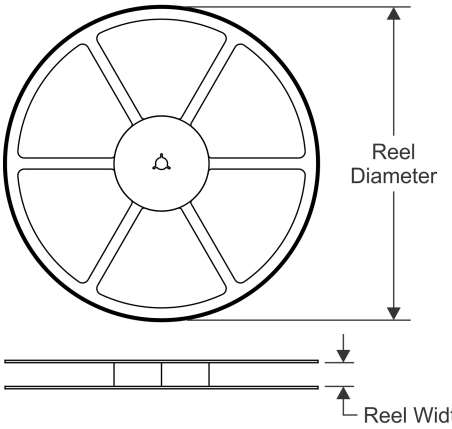
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

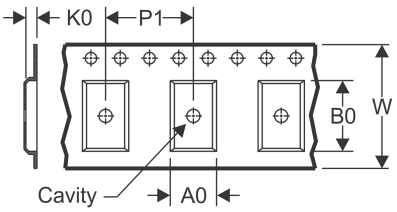
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

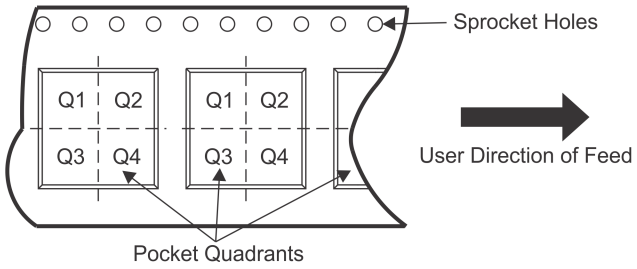



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

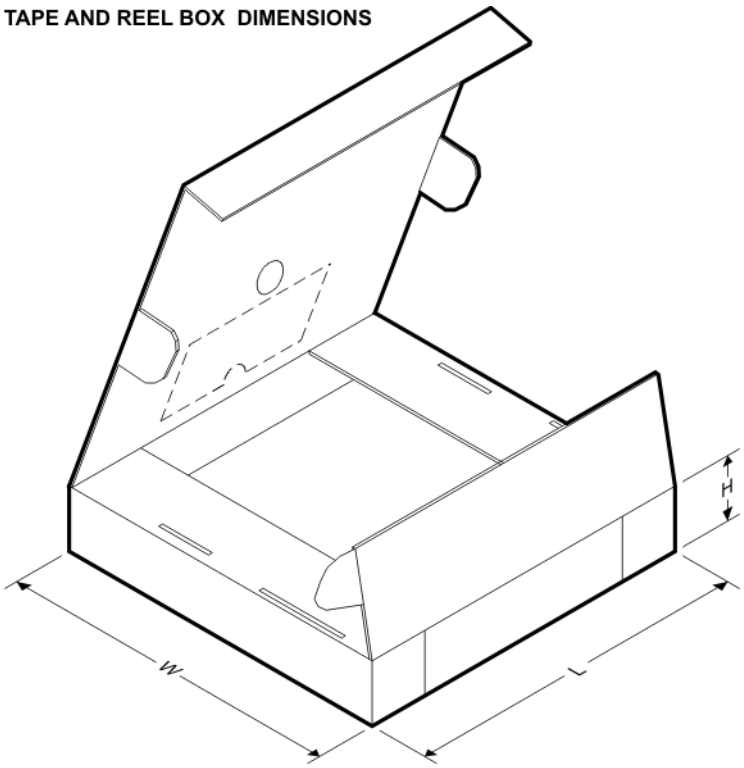
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8824PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| DRV8824RHDR | VQFN | RHD | 28 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| DRV8824RHDT | VQFN | RHD | 28 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

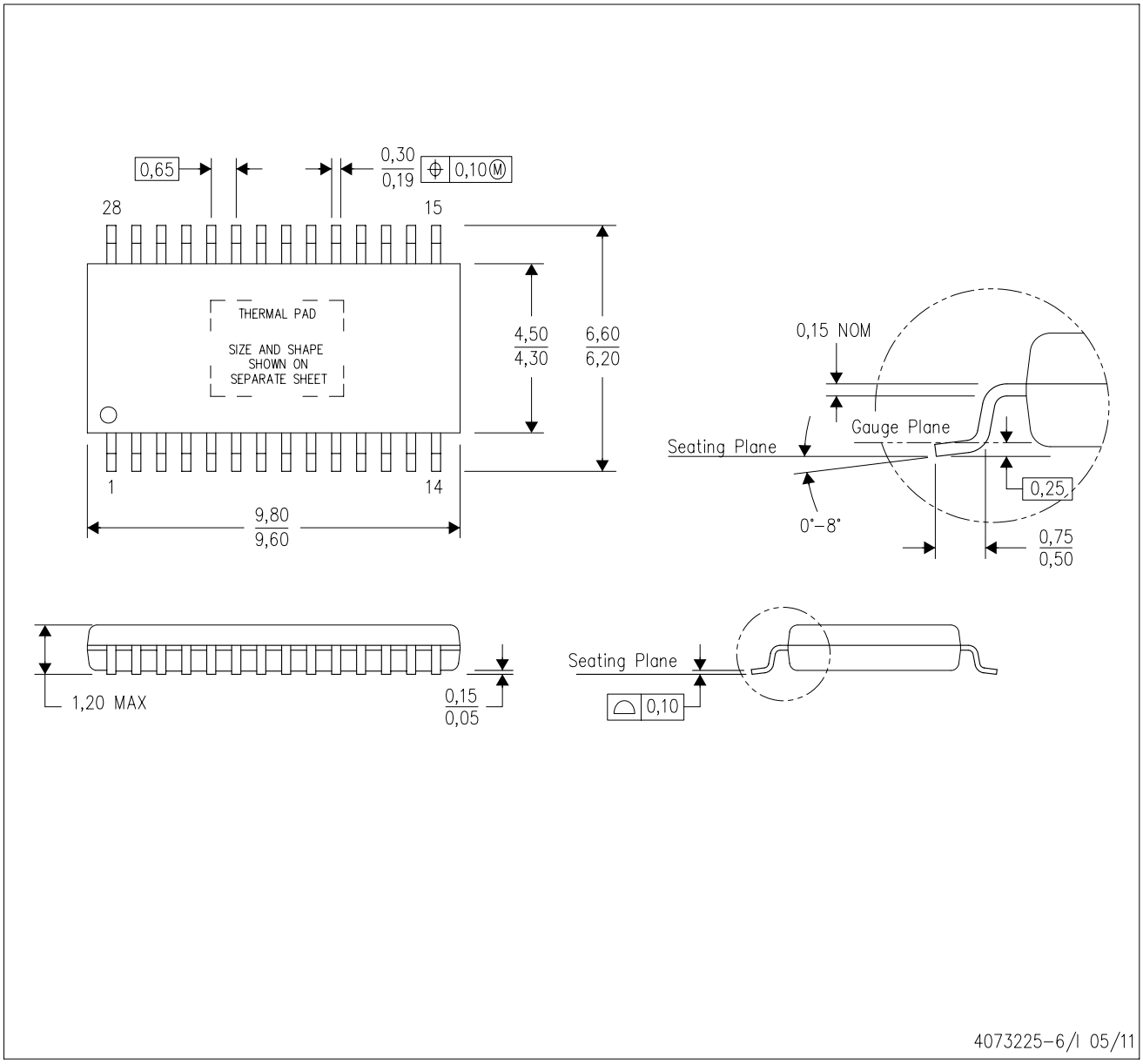
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8824PWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| DRV8824RHDR | VQFN | RHD | 28 | 3000 | 367.0 | 367.0 | 35.0 |
| DRV8824RHDT | VQFN | RHD | 28 | 250 | 552.0 | 154.0 | 36.0 |

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

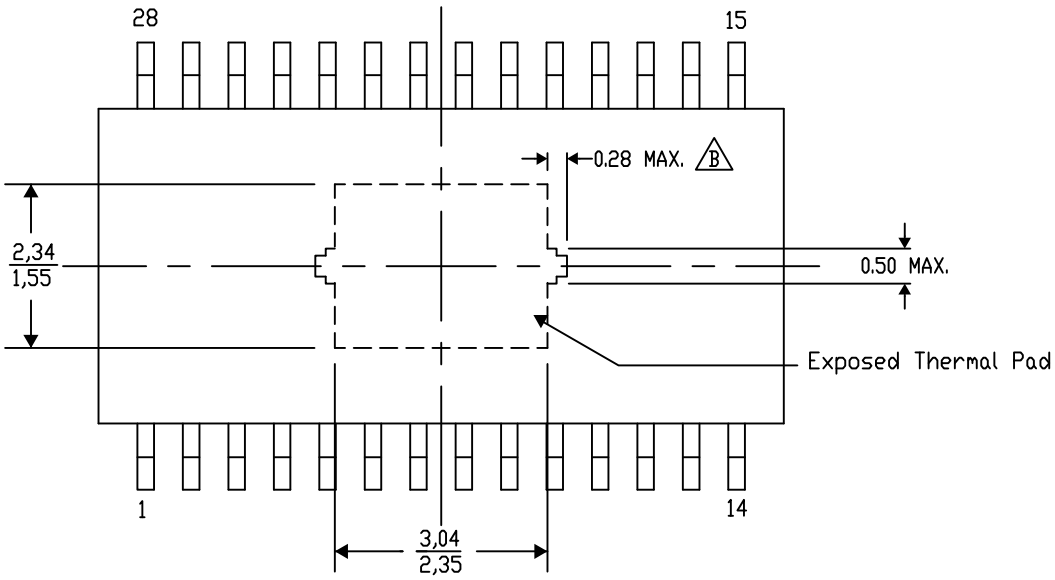
# PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

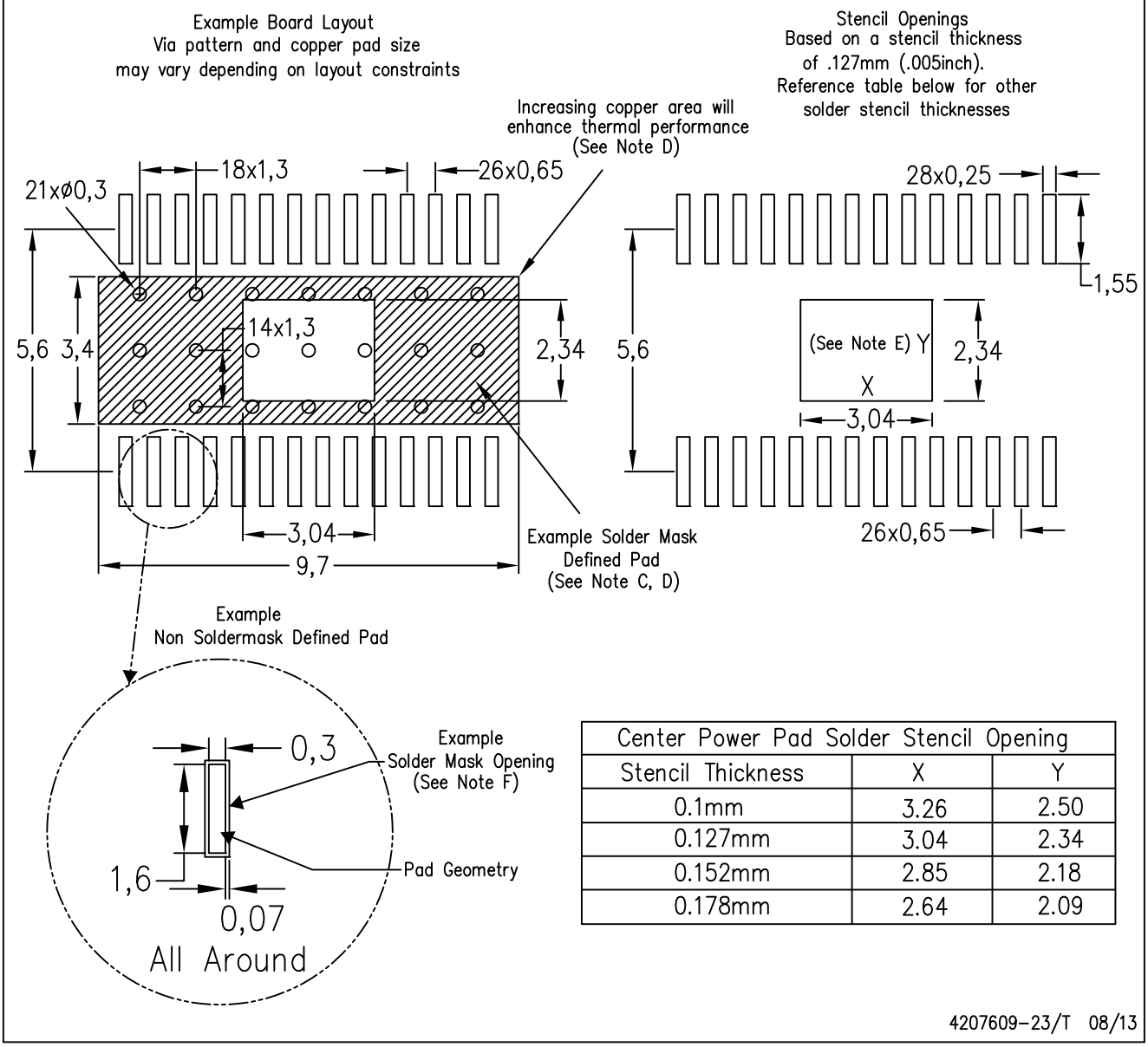
4206332–39/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

# PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE

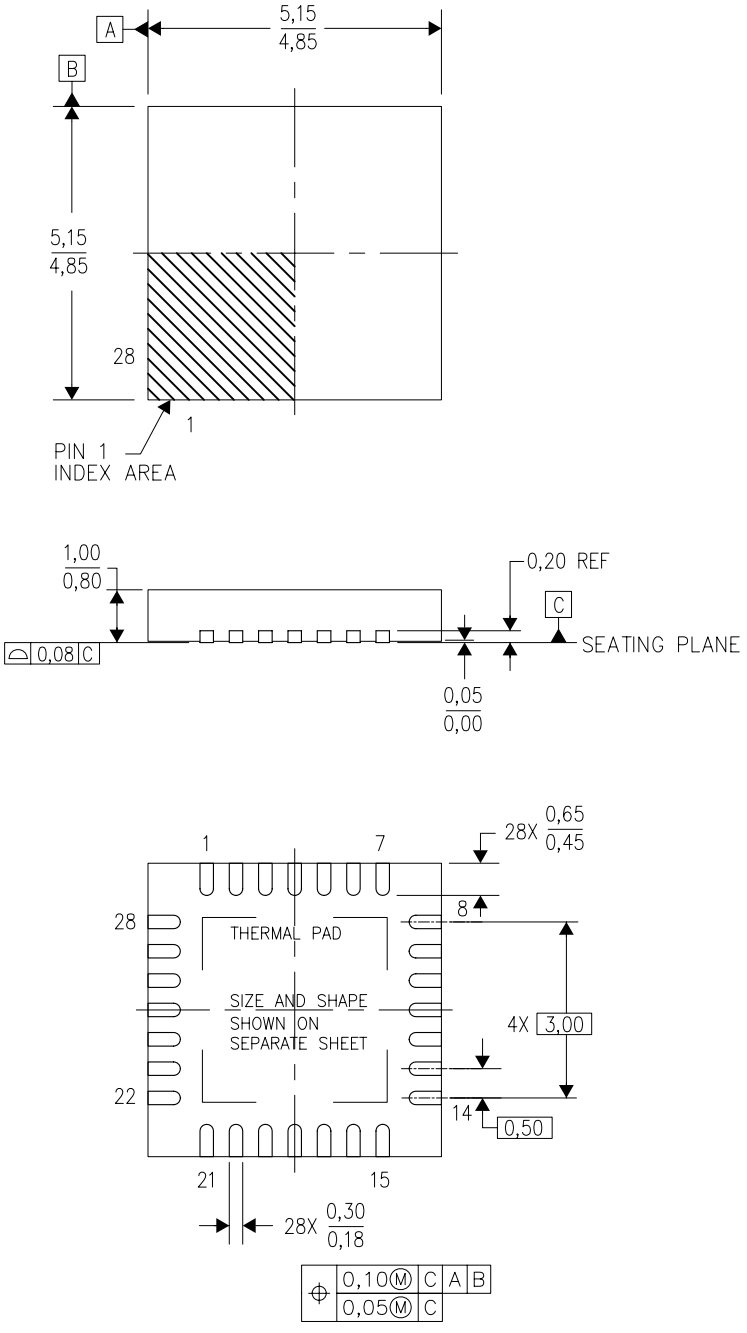



| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.26 | 2.50 |
| 0.127mm | 3.04 | 2.34 |
| 0.152mm | 2.85 | 2.18 |
| 0.178mm | 2.64 | 2.09 |

4207609–23/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD




4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

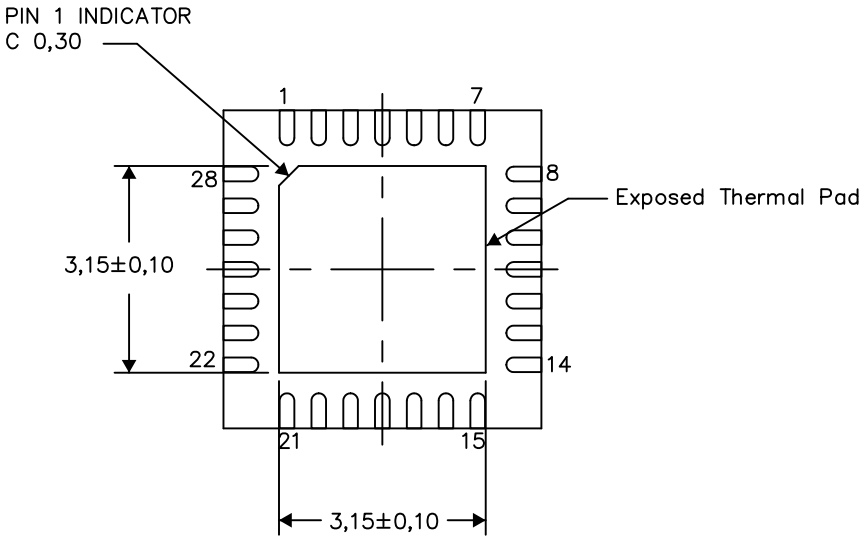
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



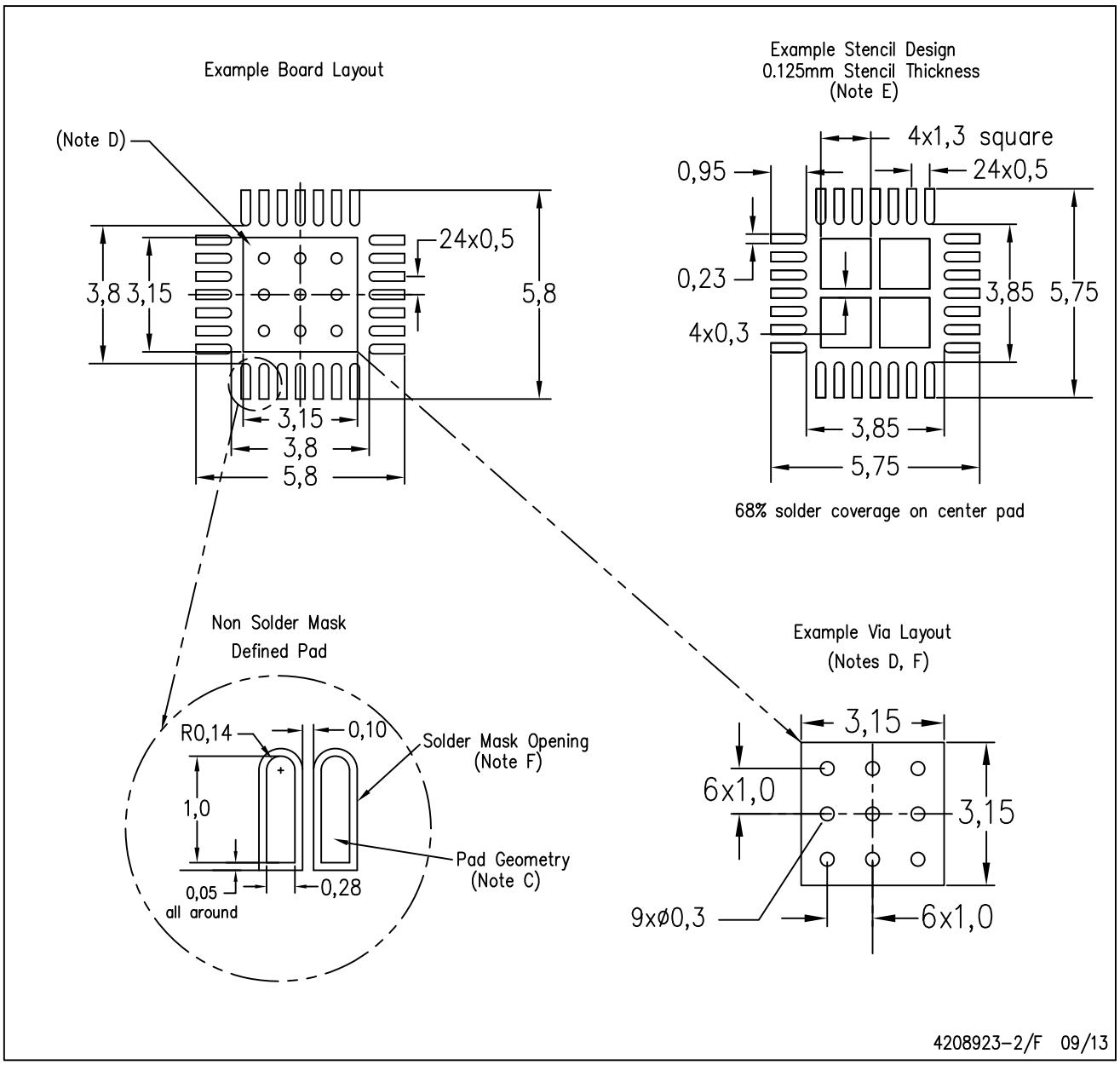

Bottom View

Exposed Thermal Pad Dimensions

4206358–2/J 09/13

NOTE: All linear dimensions are in millimeters

# RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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