

# LM4935

*LM4935 Audio Sub-System with Dual-Mode Stereo Headphone & Mono High Efficiency Loudspeaker Amplifiers and Multi-Purpose ADC*



Literature Number: SNAS296D

## LM4935 Boomer® Audio Power Amplifier Series

# Audio Sub-System with Dual-Mode Stereo Headphone & Mono High Efficiency Loudspeaker Amplifiers and Multi-Purpose ADC

## 1.0 General Description

The LM4935 is an integrated audio subsystem that supports both analog and digital audio functions. The LM4935 includes a high quality stereo DAC, a mono ADC, a multi-purpose SAR ADC, a stereo headphone amplifier, which supports output cap-less (OCL) or AC-coupled (SE) modes of operation, a mono earpiece amplifier and a mono high efficiency loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices.

The LM4935 features a bi-directional I<sup>2</sup>S serial interface for full range audio and an I<sup>2</sup>C or SPI compatible interface for control. The stereo DAC path features an SNR of 88 dB with an 18-bit 48 kHz input. In SE mode the headphone amplifier delivers at least 33 mW<sub>RMS</sub> to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when A<sub>VDD</sub> = 3.3V. The mono earpiece amplifier delivers at least 115 mW<sub>RMS</sub> to a 32Ω bridged-tied load with less than 1% distortion (THD+N) when A<sub>VDD</sub> = 3.3V. The mono speaker amplifier delivers up to 600 mW into an 8Ω load with less than 1% distortion when LS<sub>VDD</sub> = 3.3V and up to 1.3W when LS<sub>VDD</sub> = 5.0V. The LM4935 also contains a general purpose SAR ADC for housekeeping duties such as battery and temperature monitoring. This can also be used for analog volume control of the output stages and can trigger interrupt events.

The LM4935 employs advanced techniques to reduce power consumption, to reduce controller overhead to speed development time and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area and cost are primary requirements.

## 2.0 Applications

- Smartphones
- Mobile Phones and Multimedia Terminals
- PDAs, Internet Appliances and Portable Gaming
- Portable DVD/CD/AAC/MP3 Players
- Digital Cameras/Camcorders

## 3.0 Key Specifications

|                                                                    |        |
|--------------------------------------------------------------------|--------|
| ■ P <sub>HP (AC-COUP)</sub> @ A <sub>VDD</sub> = 3.3V, 32Ω, 1% THD | 33 mW  |
| ■ P <sub>HP (OCL)</sub> @ A <sub>VDD</sub> = 3.3V, 32Ω, 1% THD     | 31 mW  |
| ■ P <sub>LS</sub> @ LS <sub>VDD</sub> = 5V, 8Ω, 1% THD             | 1.3 W  |
| ■ P <sub>LS</sub> @ LS <sub>VDD</sub> = 4.2V, 8Ω, 1% THD           | 900 mW |
| ■ P <sub>LS</sub> @ LS <sub>VDD</sub> = 3.3V, 8Ω, 1% THD           | 600 mW |

### ■ Supply Voltage Range

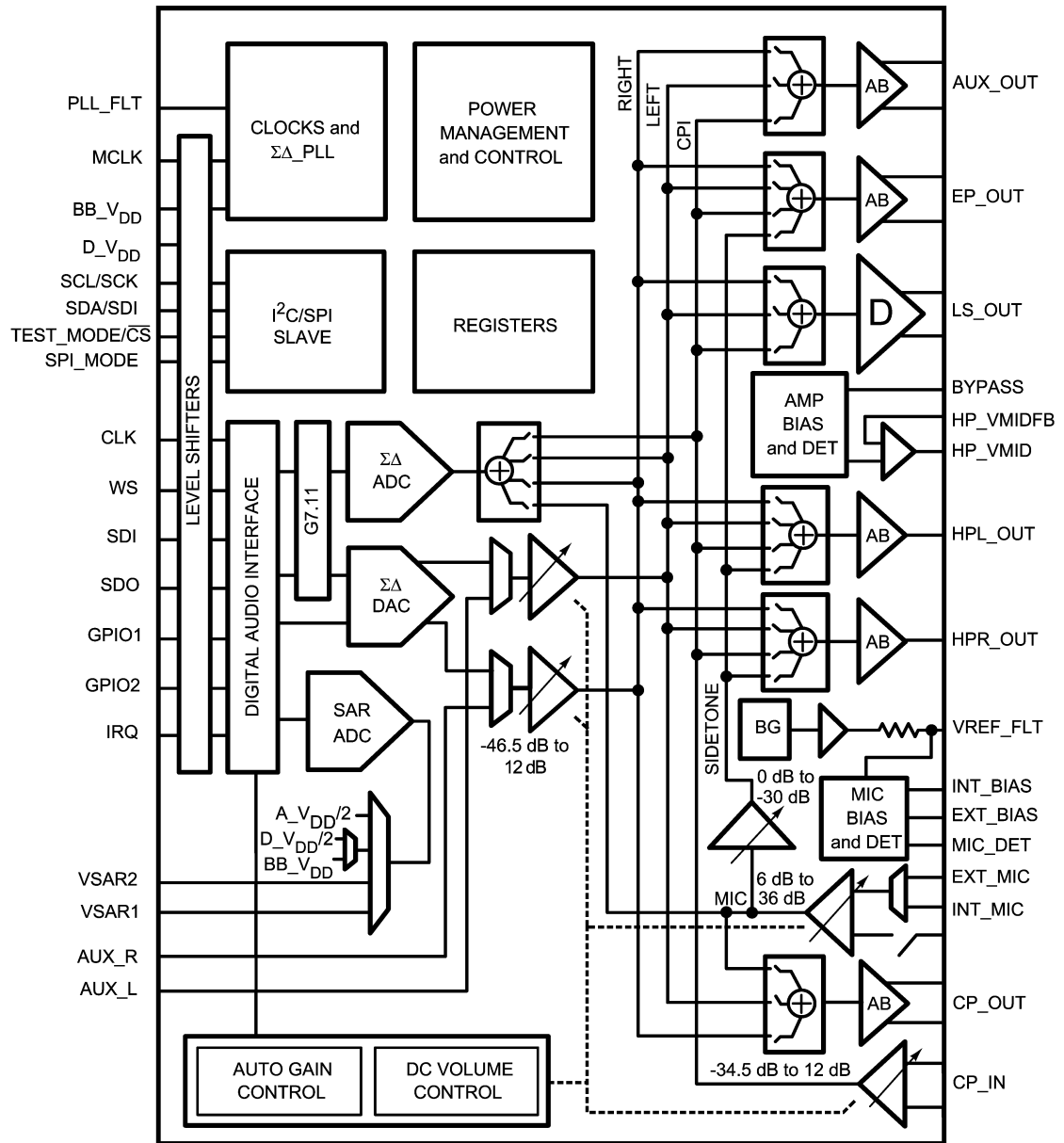
BB<sub>VDD</sub> = 1.8V to 4.5V,  
D<sub>VDD</sub> & PLL<sub>VDD</sub> = 2.7V to 4.5V  
LS<sub>VDD</sub> & A<sub>VDD</sub> = 2.7V to 5.5V

|                                                       |             |
|-------------------------------------------------------|-------------|
| ■ Shutdown Current                                    | 1.1 μA      |
| ■ PSRR @ 217 Hz, A <sub>VDD</sub> = 3.3V, (Headphone) | 60 dB       |
| ■ SNR (Stereo DAC to AUXOUT)                          | 88 dB (typ) |
| ■ SNR (Mono ADC from Cell Phone In)                   | 90 dB (typ) |
| ■ SNR (Aux In to Headphones)                          | 98 dB (typ) |

## 4.0 Features

- 18-bit stereo DAC
- 16-bit mono ADC
- 12-bit 4 input multipurpose SAR ADC
- 8 kHz to 48 kHz stereo audio playback
- 8 kHz to 48 kHz mono recording
- 1 Hz to 13.888 kHz sample rate on all 4 SAR channels
- Bidirectional PCM/I<sup>2</sup>S compatible audio interface
- Sigma-Delta PLL for operation from any clock at any sample rate
- Low power clock network operation if 12 MHz system clock is available
- Read/write I<sup>2</sup>C or SPI compatible control interface
- 33mW stereo headphone amplifier at 3.3V
- OCL or AC-coupled headphone operation
- Automatic headphone & microphone detection
- Support for internal and external microphones
- Automatic gain control for microphone input
- High efficiency BTL 8Ω amplifier, 600 mW @ 3.3V
- 115 mW earpiece amplifier at 3.3V
- Differential audio I/O for external cellphone module
- Mono differential auxiliary output
- Stereo auxiliary inputs
- Differential microphone input for internal microphone
- Flexible audio routing from input to output
- 32 Step volume control for mixers with 1.5 dB steps
- 16 Step volume control for microphone in 2 dB steps
- Programmable sidetone attenuation in 3 dB steps
- DC Volume Control
- Two configurable GPIO ports
- Programmable voltage triggers on SAR channels
- Multi-function IRQ output
- Micro-power shutdown mode
- Available in the 4 x 4 mm 49 bump micro SMDxt package

## 5.0 LM4935 Overview



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FIGURE 1. Conceptual Schematic

## 6.0 Typical Application

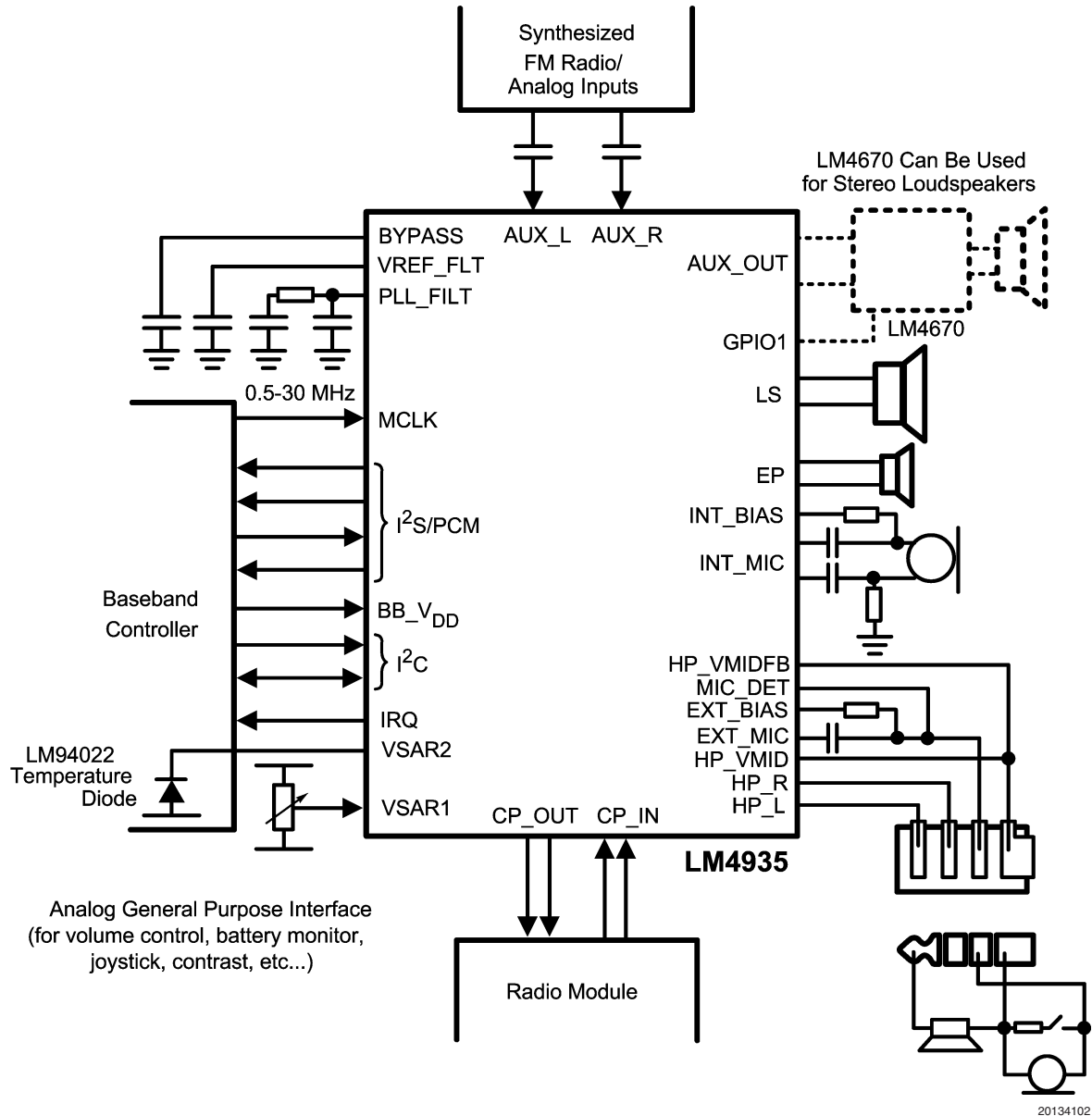


FIGURE 2. Example Application in Multimedia Mobile Phone

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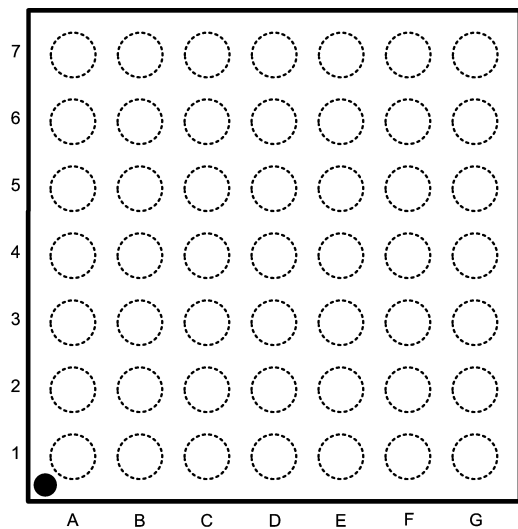
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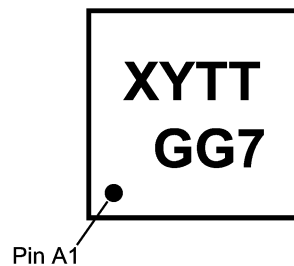
## 7.0 Connection Diagrams

49 Bump micro SMDxt



Top View (Bump Side Down)  
 Order Number LM4935RL  
 See NS Package Number RLA49UUA

49 Bump micro SMDxt Marking



Top View  
 XY — Date Code  
 TT — Die Traceability  
 G — Boomer  
 G7 — LM4935RL

## 7.0 Connection Diagrams (Continued)

### Pin Descriptions

| Pin | Pin Name                          | Type    | Direction | Description                                                                                                                                                             |
|-----|-----------------------------------|---------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1  | EP_NEG                            | Analog  | Output    | Earpiece negative output                                                                                                                                                |
| A2  | A_V <sub>DD</sub>                 | Supply  | Input     | Headphone and mixer V <sub>DD</sub>                                                                                                                                     |
| A3  | INT_MIC_POS                       | Analog  | Input     | Internal microphone positive input                                                                                                                                      |
| A4  | EXT_MIC                           | Analog  | Input     | External microphone input                                                                                                                                               |
| A5  | VSAR2                             | Analog  | Input     | Input to SAR channel 2                                                                                                                                                  |
| A6  | VSAR1                             | Analog  | Input     | Input to SAR channel 1                                                                                                                                                  |
| A7  | PLL_V <sub>SS</sub>               | Supply  | Input     | PLL V <sub>SS</sub>                                                                                                                                                     |
| B1  | A_V <sub>SS</sub>                 | Supply  | Input     | Headphone and mixer V <sub>SS</sub>                                                                                                                                     |
| B2  | EP_POS                            | Analog  | Output    | Earpiece positive output                                                                                                                                                |
| B3  | INT_MIC_NEG                       | Analog  | Input     | Internal microphone negative input                                                                                                                                      |
| B4  | BYPASS                            | Analog  | Inout     | A_V <sub>DD</sub> /2 filter point                                                                                                                                       |
| B5  | TEST_MODE/ $\overline{\text{CS}}$ | Digital | Input     | If SPI_MODE = 1, then this pin becomes $\overline{\text{CS}}$ . If SPI_MODE = 0, and TEST_MODE/ $\overline{\text{CS}}$ = 1, then this places the LM4935 into test mode. |
| B6  | PLL_FILT                          | Analog  | Inout     | Filter point for PLL VCO input                                                                                                                                          |
| B7  | PLL_V <sub>DD</sub>               | Supply  | Input     | PLL V <sub>DD</sub>                                                                                                                                                     |
| C1  | HP_R                              | Analog  | Output    | Headphone Right Output                                                                                                                                                  |
| C2  | EXT_BIAS                          | Analog  | Output    | External microphone supply (2.0/2.5/2.8/3.3V)                                                                                                                           |
| C3  | INT_BIAS                          | Analog  | Output    | 2.0V/2.5V ultra-clean supply for internal microphone                                                                                                                    |
| C4  | AUX_R                             | Analog  | Input     | Right Analog Input                                                                                                                                                      |
| C5  | GPIO_2                            | Digital | Inout     | General Purpose I/O 2                                                                                                                                                   |
| C6  | SDA                               | Digital | Inout     | Control Data, I2C_SDA or SPI_SDI                                                                                                                                        |
| C7  | SCL                               | Digital | Input     | Control Clock, I2C_SCL or SPI_SCK                                                                                                                                       |
| D1  | HP_L                              | Analog  | Output    | Headphone Left Output                                                                                                                                                   |
| D2  | VREF_FLT                          | Analog  | Inout     | Filter point for the microphone power supply                                                                                                                            |
| D3  | AUX_L                             | Analog  | Input     | Left Analog Input                                                                                                                                                       |
| D4  | SPI_MODE                          | Digital | Input     | Control mode select 1 = SPI, 0 = I2C (or test)                                                                                                                          |
| D5  | GPIO_1                            | Digital | Inout     | General Purpose I/O 1                                                                                                                                                   |
| D6  | BB_V <sub>DD</sub>                | Supply  | Input     | Baseband V <sub>DD</sub> for the digital I/Os                                                                                                                           |
| D7  | D_V <sub>DD</sub>                 | Supply  | Input     | Digital V <sub>DD</sub>                                                                                                                                                 |
| E1  | HP_VMID                           | Analog  | Inout     | Virtual Ground for Headphones in OCL mode, otherwise 1st headset detection input                                                                                        |
| E2  | HP_VMID_FB                        | Analog  | Inout     | VMID Feedback in OCL mode, otherwise a 2nd headset detection input                                                                                                      |
| E3  | MIC_DET                           | Analog  | Input     | Headset insertion/removal and Microphone presence detection input                                                                                                       |
| E4  | CPI_NEG                           | Analog  | Input     | Cell Phone analog input negative                                                                                                                                        |
| E5  | IRQ                               | Digital | Output    | Interrupt request signal (NOT open drain)                                                                                                                               |
| E6  | I2S_SDO                           | Digital | Output    | I2S Serial Data Out                                                                                                                                                     |
| E7  | I2S_SDI                           | Digital | Input     | I2S Serial Data Input                                                                                                                                                   |
| F1  | LS_V <sub>DD</sub>                | Supply  | Input     | Loudspeaker V <sub>DD</sub>                                                                                                                                             |
| F2  | LS_V <sub>DD</sub>                | Supply  | Input     | Loudspeaker V <sub>DD</sub>                                                                                                                                             |
| F3  | CPI_POS                           | Analog  | Input     | Cell Phone analog input positive                                                                                                                                        |
| F4  | CPO_NEG                           | Analog  | Output    | Cell Phone analog output negative                                                                                                                                       |
| F5  | AUX_OUT_NEG                       | Analog  | Output    | Auxiliary analog output negative                                                                                                                                        |
| F6  | I2S_WS                            | Digital | Inout     | I2S Word Select Signal (can be master or slave)                                                                                                                         |
| F7  | I2S_CLK                           | Digital | Inout     | I2S Clock Signal (can be master or slave)                                                                                                                               |
| G1  | LS_POS                            | Analog  | Output    | Loudspeaker positive output                                                                                                                                             |
| G2  | LS_V <sub>SS</sub>                | Supply  | Input     | Loudspeaker V <sub>SS</sub>                                                                                                                                             |
| G3  | LS_NEG                            | Analog  | Output    | Loudspeaker negative output                                                                                                                                             |
| G4  | CPO_POS                           | Analog  | Output    | Cell Phone analog output positive                                                                                                                                       |
| G5  | AUX_OUT_POS                       | Analog  | Output    | Auxiliary analog output positive                                                                                                                                        |



## 7.0 Connection Diagrams (Continued)

### Pin Descriptions (Continued)

| Pin | Pin Name          | Type    | Direction | Description                        |
|-----|-------------------|---------|-----------|------------------------------------|
| G6  | D_V <sub>SS</sub> | Supply  | Input     | Digital V <sub>SS</sub>            |
| G7  | MCLK              | Digital | Input     | Input clock from 0.5 MHz to 30 MHz |

#### 7.1 PIN TYPE DEFINITIONS

**Analog Input—** A pin that is used by the analog and is never driven by the device. Supplies are part of this classification.

**Analog Output—** A pin that is driven by the device and should not be driven by external sources.

**Analog Inout—** A pin that is typically used for filtering a DC signal within the device. Passive components can be connected to these pins.

**Digital Input—** A pin that is used by the digital but is

never driven.

**Digital Output—** A pin that is driven by the device and should not be driven by another device to avoid contention.

**Digital Inout—** A pin that is either open drain (I2C\_SDA) or a bidirectional CMOS in/out. In the later case the direction is selected by a control register within the LM4935.

## 8.0 Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                                                                           |                    |
|-------------------------------------------------------------------------------------------|--------------------|
| Analog Supply Voltage<br>(A_V <sub>DD</sub> & LS_V <sub>DD</sub> )                        | 6.0V               |
| Digital Supply Voltage<br>(BB_V <sub>DD</sub> & D_V <sub>DD</sub> & PLL_V <sub>DD</sub> ) | 6.0V               |
| Storage Temperature                                                                       | –65°C to +150°C    |
| Power Dissipation (Note 3)                                                                | Internally Limited |
| ESD Susceptibility                                                                        |                    |
| Human Body Model (Note 4)                                                                 | 2500V              |
| Machine Model (Note 5)                                                                    | 200V               |

|                                                                                                                  |        |
|------------------------------------------------------------------------------------------------------------------|--------|
| Junction Temperature                                                                                             | 150°C  |
| Thermal Resistance<br>$\theta_{JA}$ – RLA49 (soldered down<br>to PCB with 2in <sup>2</sup> 1oz. copper<br>plane) | 60°C/W |
| Soldering Information                                                                                            |        |

## 9.0 Operating Ratings

|                                        |                |
|----------------------------------------|----------------|
| Temperature Range                      | –40°C to +85°C |
| Supply Voltage                         |                |
| D_V <sub>DD</sub> /PLL_V <sub>DD</sub> | 2.7V to 4.5V   |
| BB_V <sub>DD</sub>                     | 1.8V to 4.5V   |
| LS_V <sub>DD</sub> /A_V <sub>DD</sub>  | 2.7V to 5.5V   |

**10.0 Electrical Characteristics** (Notes 1, 2) Unless otherwise stated PLL\_V<sub>DD</sub> = 3.3V, D\_V<sub>DD</sub> = 3.3V, BB\_V<sub>DD</sub> = 1.8V, A\_V<sub>DD</sub> = 3.3V, LS\_V<sub>DD</sub> = 3.3V. The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

| Symbol                 | Parameter                | Conditions                                                                | LM4935              |                   | Units       |
|------------------------|--------------------------|---------------------------------------------------------------------------|---------------------|-------------------|-------------|
|                        |                          |                                                                           | Typical<br>(Note 6) | Limit<br>(Note 7) |             |
| DC CURRENT CONSUMPTION |                          |                                                                           |                     |                   |             |
| DI <sub>SD</sub>       | Digital Shutdown Current | Chip Mode '00', f <sub>MCLK</sub> = 13MHz                                 | 0.7                 |                   | μA          |
|                        |                          | Chip Mode '00', f <sub>MCLK</sub> = 19.2MHz                               | 0.7                 | 5                 | μA<br>(max) |
| DI <sub>ST</sub>       | Digital Standby Current  | Chip Mode '01', f <sub>MCLK</sub> = 13MHz                                 | 1.5                 |                   | mA          |
|                        |                          | Chip Mode '01', f <sub>MCLK</sub> = 19.2MHz                               | 2.2                 | 3                 | mA<br>(max) |
| DI <sub>DD</sub>       | Digital Active Current   | Chip Mode '10', f <sub>MCLK</sub> = 13MHz,<br>DAC, ADC, SAR OFF           | 1.5                 |                   | mA          |
|                        |                          | Chip Mode '10', f <sub>MCLK</sub> = 19.2MHz,<br>DAC, ADC, SAR OFF         | 2.2                 |                   | mA          |
|                        |                          | Chip Mode '10', f <sub>MCLK</sub> = 13MHz<br>DAC, ADC, SAR ON             | 11.2                |                   | mA          |
|                        |                          | Chip Mode '10', f <sub>MCLK</sub> = 19.2MHz,<br>DAC, ADC, SAR ON          | 16.2                | 20                | mA<br>(max) |
| AI <sub>SD</sub>       | Analog Shutdown Current  | Chip Mode '00'                                                            | 0.2                 | 3                 | μA<br>(max) |
| AI <sub>ST</sub>       | Analog Standby Current   | Chip Mode '01',<br>No headset inserted                                    | 0.2                 | 3                 | μA<br>(max) |
| AI <sub>DD</sub>       | Analog Active Current    | All Outputs OFF, SE MODE                                                  | 6.1                 |                   | mA          |
|                        |                          | All Outputs OFF, OCL MODE                                                 | 5.7                 |                   | mA          |
|                        |                          | All Outputs ON, SE MODE                                                   | 18.3                |                   | mA          |
|                        |                          | All Outputs ON, OCL MODE                                                  | 18.7                | 28                | mA<br>(max) |
| PLLI <sub>DD</sub>     | PLL Active Current       | f <sub>MCLK</sub> = 13 MHz<br>f <sub>PLLOUT</sub> = 12 MHz, PLL ON only   | 4.2                 |                   | mA          |
|                        |                          | f <sub>MCLK</sub> = 19.2 MHz<br>f <sub>PLLOUT</sub> = 12 MHz, PLL ON only | 6.2                 |                   | mA          |
| ADCI <sub>DD</sub>     | ADC Active Current       | f <sub>MCLK</sub> = 13MHz, ADC ON only                                    | 2.5                 |                   | mA          |
|                        |                          | f <sub>MCLK</sub> = 19.2MHz, ADC ON only                                  | 3.6                 |                   | mA          |

## 10.0 Electrical Characteristics

(Notes 1, 2) Unless otherwise stated  $PLL\_V_{DD} = 3.3V$ ,  $D\_V_{DD} = 3.3V$ ,  $BB\_V_{DD} = 1.8V$ ,  $A\_V_{DD} = 3.3V$ ,  $LS\_V_{DD} = 3.3V$ . The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

| Symbol                 | Parameter                                      | Conditions                                                                                                                           | LM4935              |                   | Units       |
|------------------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------------------|-------------|
|                        |                                                |                                                                                                                                      | Typical<br>(Note 6) | Limit<br>(Note 7) |             |
| DC CURRENT CONSUMPTION |                                                |                                                                                                                                      |                     |                   |             |
| DACI <sub>DD</sub>     | DAC Active Current                             | f <sub>MCLK</sub> = 13MHz, DAC ON only;<br>PLL OFF, f <sub>S</sub> = 48kHz                                                           | 7.4                 |                   | mA          |
|                        |                                                | f <sub>MCLK</sub> = 19.2MHz, DAC ON only<br>PLL OFF; f <sub>S</sub> = 48kHz                                                          | 10.7                |                   | mA          |
| SARI <sub>DD</sub>     | SAR Active Current                             | f <sub>MCLK</sub> = 13MHz, SAR ON only                                                                                               | 1.6                 |                   | mA          |
|                        |                                                | f <sub>MCLK</sub> = 19.2MHz, SAR ON only                                                                                             | 2.3                 |                   | mA          |
| LSI <sub>DD</sub>      | Loudspeaker Quiescent Current                  | LS ON only                                                                                                                           | 8.8                 |                   | mA          |
| HPI <sub>DD</sub>      | Headphone Quiescent Current                    | HP ON only, SE MODE                                                                                                                  | 3.5                 |                   | mA          |
|                        |                                                | HP ON only, OCL MODE                                                                                                                 | 3.9                 |                   | mA          |
| EPI <sub>DD</sub>      | Earpiece Quiescent Current                     | EP ON only                                                                                                                           | 4.4                 |                   | mA          |
| AUXI <sub>DD</sub>     | AUXOUT Quiescent Current                       | AUXOUT ON only                                                                                                                       | 4.8                 |                   | mA          |
| CPOUTI <sub>DD</sub>   | CPOUT Quiescent Current                        | CPOUT ON only                                                                                                                        | 4.8                 |                   | mA          |
| LOUDSPEAKER AMPLIFIER  |                                                |                                                                                                                                      |                     |                   |             |
| P <sub>LS</sub>        | Max Loudspeaker Power                          | 8Ω load, LS_V <sub>DD</sub> = 5V                                                                                                     | 1.3                 |                   | W           |
|                        |                                                | 8Ω load, LS_V <sub>DD</sub> = 4.2V                                                                                                   | 0.9                 |                   | W           |
|                        |                                                | 8Ω load, LS_V <sub>DD</sub> = 3.3V                                                                                                   | 0.6                 | 0.44              | W (min)     |
| LS <sub>THD+N</sub>    | Loudspeaker Harmonic Distortion                | 8Ω load, LS_V <sub>DD</sub> = 3.3V,<br>P <sub>O</sub> = 400mW                                                                        | 0.4                 |                   | %           |
| LS <sub>EFF</sub>      | Efficiency                                     | 0 dB Input<br>MCLK = 12.000 MHz                                                                                                      | 84                  |                   | %           |
| PSRR <sub>LS</sub>     | Power Supply Rejection Ration<br>(Loudspeaker) | AUX inputs terminated<br>C <sub>BYPASS</sub> = 1.0 μF<br>V <sub>RIPPLE</sub> = 200 mV <sub>P-P</sub><br>f <sub>RIPPLE</sub> = 217 Hz | 54                  |                   | dB          |
| SNR <sub>LS</sub>      | Signal to Noise Ratio                          | From 0 dB Analog AUX input at<br>1 kHz, A-weighted                                                                                   | 76                  |                   | dB          |
| e <sub>N</sub>         | Output Noise                                   | A-weighted                                                                                                                           | 350                 |                   | μV          |
| V <sub>OS</sub>        | Offset Voltage                                 |                                                                                                                                      | 7                   |                   | mV          |
| HEADPHONE AMPLIFIER    |                                                |                                                                                                                                      |                     |                   |             |
| P <sub>HP</sub>        | Headphone Power                                | 32Ω load, 3.3V, SE                                                                                                                   | 33                  | 20                | mW<br>(min) |
|                        |                                                | 16Ω load, 3.3V, SE                                                                                                                   | 52                  |                   | mW          |
|                        |                                                | 32Ω load, 3.3V, OCL, VCM = 1.5V                                                                                                      | 31                  |                   | mW          |
|                        |                                                | 32Ω load, 3.3V, OCL, VCM = 1.2V                                                                                                      | 20                  |                   | mW          |
|                        |                                                | 16Ω load, 3.3V, OCL, VCM = 1.5V                                                                                                      | 50                  |                   | mW          |
|                        |                                                | 16Ω load, 3.3V, OCL, VCM = 1.2V                                                                                                      | 32                  |                   | mW          |
| PSRR <sub>HP</sub>     | Power Supply Rejection Ratio<br>(Headphones)   | AUX inputs terminated<br>C <sub>BYPASS</sub> = 1.0 μF<br>V <sub>RIPPLE</sub> = 200 mV <sub>P-P</sub><br>f <sub>RIPPLE</sub> = 217 Hz |                     |                   |             |
|                        |                                                | SE Mode                                                                                                                              | 60                  |                   | dB          |
|                        |                                                | OCL Mode<br>VCM = 1.2V                                                                                                               | 68                  |                   | dB          |
|                        |                                                | OCL Mode<br>VCM = 1.5V                                                                                                               | 65                  |                   | dB          |

**10.0 Electrical Characteristics** (Notes 1, 2) Unless otherwise stated  $PLL\_V_{DD} = 3.3V$ ,  $D\_V_{DD} = 3.3V$ ,  $BB\_V_{DD} = 1.8V$ ,  $A\_V_{DD} = 3.3V$ ,  $LS\_V_{DD} = 3.3V$ . The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

| Symbol               | Parameter                                  | Conditions                                                                                                                           | LM4935              |                   | Units            |
|----------------------|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------------------|------------------|
|                      |                                            |                                                                                                                                      | Typical<br>(Note 6) | Limit<br>(Note 7) |                  |
| HEADPHONE AMPLIFIER  |                                            |                                                                                                                                      |                     |                   |                  |
| SNR <sub>HP</sub>    | Signal to Noise Ratio                      | From 0dB Analog AUX input<br>A-weighted                                                                                              |                     |                   |                  |
|                      |                                            | SE Mode                                                                                                                              | 98                  |                   | dB               |
|                      |                                            | OCL Mode<br>VCM = 1.2V                                                                                                               | 97                  |                   | dB               |
|                      |                                            | OCL Mode<br>VCM = 1.5V                                                                                                               | 96                  |                   | dB               |
| HP <sub>THD+N</sub>  | Headphone Harmonic Distortion              | 32Ω load, 3.3V, P <sub>O</sub> = 7.5mW                                                                                               | 0.05                |                   | %                |
| e <sub>N</sub>       | Output Noise                               | A-weighted                                                                                                                           | 12                  |                   | μV               |
| ΔA <sub>CH-CH</sub>  | Stereo Channel-to-Channel Gain<br>Mismatch |                                                                                                                                      | 0.3                 |                   | dB               |
| X <sub>TALK</sub>    | Stereo Crosstalk                           | SE Mode                                                                                                                              | 61                  |                   | dB               |
|                      |                                            | OCL Mode                                                                                                                             | 63                  |                   | dB               |
| EARPIECE AMPLIFIER   |                                            |                                                                                                                                      |                     |                   |                  |
| P <sub>EP</sub>      | Earpiece Power                             | 32Ω load, 3.3V                                                                                                                       | 115                 | 100               | mW<br>(min)      |
|                      |                                            | 16Ω load, 3.3V                                                                                                                       | 150                 |                   | mW               |
| PSRR <sub>EP</sub>   | Power Supply Rejection Ratio<br>(Earpiece) | AUX inputs terminated<br>C <sub>BYPASS</sub> = 1.0 μF<br>V <sub>RIPPLE</sub> = 200 mV <sub>P-P</sub><br>F <sub>RIPPLE</sub> = 217 Hz | 65                  |                   | dB               |
| SNR <sub>EP</sub>    | Signal to Noise Ratio                      | From 0dB Analog AUX input,<br>A-weighted                                                                                             | 98                  |                   | dB               |
| EP <sub>THD+N</sub>  | Earpiece Harmonic Distortion               | 32Ω load, 3.3V, P <sub>O</sub> = 50mW                                                                                                | 0.04                |                   | %                |
| e <sub>N</sub>       | Output Noise                               | A-weighted                                                                                                                           | 24                  |                   | μV               |
| V <sub>OS</sub>      | Offset Voltage                             |                                                                                                                                      | 15                  |                   | mV               |
| AUXOUT AMPLIFIER     |                                            |                                                                                                                                      |                     |                   |                  |
| THD+N                | Total Harmonic Distortion + Noise          | V <sub>O</sub> = 1V <sub>RMS</sub> , 5kΩ load                                                                                        | 0.02                |                   | %                |
| PSRR                 | Power Supply Rejection Ratio               | AUX inputs terminated<br>C <sub>BYPASS</sub> = 1.0μF<br>V <sub>RIPPLE</sub> = 200mVPP<br>f <sub>RIPPLE</sub> = 217Hz                 | 70                  |                   | dB               |
| CP_OUT AMPLIFIER     |                                            |                                                                                                                                      |                     |                   |                  |
| THD+N                | Total Harmonic Distortion + Noise          | V <sub>O</sub> = 1V <sub>RMS</sub> , 5kΩ load                                                                                        | 0.02                |                   | %                |
| PSRR                 | Power SUPply Rejection Ratio               | C <sub>BYPASS</sub> = 1.0μF<br>V <sub>RIPPLE</sub> = 200mVPP<br>f <sub>RIPPLE</sub> = 217Hz                                          | 68                  |                   | dB               |
| MONO ADC             |                                            |                                                                                                                                      |                     |                   |                  |
| R <sub>ADC</sub>     | ADC Ripple                                 |                                                                                                                                      | ±0.25               |                   | dB               |
| PB <sub>ADC</sub>    | ADC Passband                               | Lower (HPF Mode 1), f <sub>S</sub> = 8 kHz                                                                                           | 300                 |                   | Hz               |
|                      |                                            | Upper                                                                                                                                | 3470                |                   | Hz               |
| SBA <sub>ADC</sub>   | ADC Stopband Attenuation                   | Above Passband                                                                                                                       | 60                  |                   | dB               |
|                      |                                            | HPF Notch, 50 Hz/60 Hz (worst<br>case)                                                                                               | 58                  |                   | dB               |
| SNR <sub>ADC</sub>   | ADC Signal to Noise Ratio                  | From CPI, A-weighted                                                                                                                 | 90                  |                   | dB               |
| ADC <sub>LEVEL</sub> | ADC Full Scale Input Level                 |                                                                                                                                      | 1                   |                   | V <sub>RMS</sub> |

## 10.0 Electrical Characteristics

(Notes 1, 2) Unless otherwise stated  $PLL\_V_{DD} = 3.3V$ ,  $D\_V_{DD} = 3.3V$ ,  $BB\_V_{DD} = 1.8V$ ,  $A\_V_{DD} = 3.3V$ ,  $LS\_V_{DD} = 3.3V$ . The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

| Symbol                   | Parameter                   | Conditions                          | LM4935              |                   | Units            |
|--------------------------|-----------------------------|-------------------------------------|---------------------|-------------------|------------------|
|                          |                             |                                     | Typical<br>(Note 6) | Limit<br>(Note 7) |                  |
| STEREO DAC               |                             |                                     |                     |                   |                  |
| R <sub>DAC</sub>         | DAC Ripple                  |                                     | 0.1                 |                   | dB               |
| PB <sub>DAC</sub>        | DAC Passband                |                                     | 20                  |                   | kHz              |
| SBA <sub>DAC</sub>       | DAC Stopband Attenuation    |                                     | 70                  |                   | dB               |
| SNR <sub>DAC</sub>       | DAC Signal to Noise Ratio   | A-weighted, AUXOUT                  | 88                  |                   | dB               |
| DR <sub>DAC</sub>        | DAC Dynamic Range           |                                     | 96                  |                   | dB               |
| DAC <sub>LEVEL</sub>     | DAC Full Scale Output Level |                                     | 1                   |                   | V <sub>RMS</sub> |
| PLL                      |                             |                                     |                     |                   |                  |
| F <sub>IN</sub>          | Input Frequency Range       | Min                                 | 0.5                 |                   | MHz              |
|                          |                             | Max                                 | 30                  |                   | MHz              |
| I2S/PCM                  |                             |                                     |                     |                   |                  |
| f <sub>I2SCLK</sub>      | I2S CLK Frequency           | f <sub>S</sub> = 48kHz; 16 bit mode | 1.536               |                   | MHz              |
|                          |                             | f <sub>S</sub> = 48kHz; 25 bit mode | 2.4                 |                   | MHz              |
|                          |                             | f <sub>S</sub> = 8kHz; 16 bit mode  | 0.256               |                   | MHz              |
|                          |                             | f <sub>S</sub> = 8kHz; 25 bit mode  | 0.4                 |                   | MHz              |
| f <sub>PCMCLK</sub>      | PCM CLK Frequency           | f <sub>S</sub> = 48kHz; 16 bit mode | 0.768               |                   | MHz              |
|                          |                             | f <sub>S</sub> = 48kHz; 25 bit mode | 1.2                 |                   | MHz              |
|                          |                             | f <sub>S</sub> = 8kHz; 16 bit mode  | 0.128               |                   | MHz              |
|                          |                             | f <sub>S</sub> = 8kHz; 25 bit mode  | 0.2                 |                   | MHz              |
| DC <sub>I2S_CLK</sub>    | I2S_CLK Duty Cycle          | Min                                 |                     | 40                | % (min)          |
|                          |                             | Max                                 |                     | 60                | % (max)          |
| DC <sub>I2S_WS</sub>     | I2S_WS Duty Cycle           |                                     | 50                  |                   | %                |
| I2C                      |                             |                                     |                     |                   |                  |
| T <sub>I2CSET</sub>      | I2C Data Setup Time         | Refer to Pg. 18 for more details    |                     | 100               | ns (min)         |
| T <sub>I2CHOLD</sub>     | I2C Data Hold Time          | Refer to Pg. 18 for more details    |                     | 300               | ns (min)         |
| SPI                      |                             |                                     |                     |                   |                  |
| T <sub>SPISETENB</sub>   | Enable Setup Time           |                                     |                     | 100               | ns (min)         |
| T <sub>SPIHOLD-ENB</sub> | Enable Hold Time            |                                     |                     | 100               | ns (min)         |
| T <sub>SPISETD</sub>     | Data Setup Time             |                                     |                     | 100               | ns (min)         |
| T <sub>SPIHOLDD</sub>    | Data Hold Time              |                                     |                     | 100               | ns (min)         |
| T <sub>SPICL</sub>       | Clock Low Time              |                                     |                     | 500               | ns (min)         |
| T <sub>SPICH</sub>       | Clock High Time             |                                     |                     | 500               | ns (min)         |
| VOLUME CONTROL           |                             |                                     |                     |                   |                  |
| VCR <sub>AUX</sub>       | AUX Volume Control Range    | Minimum Gain w/ AUX_BOOST OFF       | −46.5               |                   | dB               |
|                          |                             | Maximum Gain w/ AUX_BOOST OFF       | 0                   |                   | dB               |
|                          |                             | Minimum Gain w/ AUX_BOOST ON        | −34.5               |                   | dB               |
|                          |                             | Maximum Gain w/ AUX_BOOST ON        | 12                  |                   | dB               |
| VCR <sub>DAC</sub>       | DAC Volume Control Range    | Minimum Gain w/ DAC_BOOST OFF       | −46.5               |                   | dB               |
|                          |                             | Maximum Gain w/ DAC_BOOST OFF       | 0                   |                   | dB               |
|                          |                             | Minimum Gain w/ DAC_BOOST ON        | −34.5               |                   | dB               |
|                          |                             | Maximum Gain w/ DAC_BOOST ON        | 12                  |                   | dB               |
| VCR <sub>CPIN</sub>      | CPIN Volume Control Range   | Minimum Gain                        | −34.5               |                   | dB               |
|                          |                             | Maximum Gain                        | 12                  |                   | dB               |

**10.0 Electrical Characteristics** (Notes 1, 2) Unless otherwise stated **PLL\_V<sub>DD</sub> = 3.3V, D\_V<sub>DD</sub> = 3.3V, BB\_V<sub>DD</sub> = 1.8V, A\_V<sub>DD</sub> = 3.3V, LS\_V<sub>DD</sub> = 3.3V**. The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

| Symbol              | Parameter                     | Conditions   | LM4935              |                   | Units |
|---------------------|-------------------------------|--------------|---------------------|-------------------|-------|
|                     |                               |              | Typical<br>(Note 6) | Limit<br>(Note 7) |       |
| VOLUME CONTROL      |                               |              |                     |                   |       |
| VCR <sub>MIC</sub>  | MIC Volume Control Range      | Minimum Gain | 6                   |                   | dB    |
|                     |                               | Maximum Gain | 36                  |                   | dB    |
| VCR <sub>SIDE</sub> | SIDETONE Volume Control Range | Minimum Gain | −30                 |                   | dB    |
|                     |                               | Maximum Gain | 0                   |                   | dB    |
| SS <sub>AUX</sub>   | AUX VCR Stepsize              |              | 1.5                 |                   | dB    |
| SS <sub>DAC</sub>   | DAC VCR Stepsize              |              | 1.5                 |                   | dB    |
| SS <sub>CPIN</sub>  | CPIN VCR Stepsize             |              | 1.5                 |                   | dB    |
| SS <sub>MIC</sub>   | MIC VCR Stepsize              |              | 2                   |                   | dB    |
| SS <sub>SIDE</sub>  | SIDETONE VCR Stepsize         |              | 3                   |                   | dB    |

**10.0 Electrical Characteristics** (Notes 1, 2) Unless otherwise stated  $PLL\_V_{DD} = 3.3V$ ,  $D\_V_{DD} = 3.3V$ ,  $BB\_V_{DD} = 1.8V$ ,  $A\_V_{DD} = 3.3V$ ,  $LS\_V_{DD} = 3.3V$ . The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

| Symbol                                                                                                       | Parameter                   | Conditions                                                                       | LM4935              |                   | Units |
|--------------------------------------------------------------------------------------------------------------|-----------------------------|----------------------------------------------------------------------------------|---------------------|-------------------|-------|
|                                                                                                              |                             |                                                                                  | Typical<br>(Note 6) | Limit<br>(Note 7) |       |
| AUDIO PATH GAIN W/ STEREO (bit 6 of 0x00h) ENABLED (AUX_L & AUX_R signals identical and selected onto mixer) |                             |                                                                                  |                     |                   |       |
|                                                                                                              | Loudspeaker Audio Path Gain | Minimum Gain from AUX input, BOOST OFF                                           | −34.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from AUX input, BOOST OFF                                           | 12                  |                   | dB    |
|                                                                                                              |                             | Minimum Gain from CPI input                                                      | −22.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from CPI input                                                      | 24                  |                   | dB    |
|                                                                                                              | Headphone Audio Path Gain   | Minimum Gain from AUX input, BOOST OFF                                           | −52.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from AUX input, BOOST OFF                                           | −6                  |                   | dB    |
|                                                                                                              |                             | Minimum Gain from CPI input                                                      | −40.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from CPI input                                                      | 6                   |                   | dB    |
|                                                                                                              |                             | Minimum Gain from MIC input using SIDETONE path w/ VCR <sub>MIC</sub> gain = 6dB | −30                 |                   | dB    |
|                                                                                                              |                             | Maximum Gain from MIC input using SIDETONE path w/ VCR <sub>MIC</sub> gain = 6dB | 0                   |                   | dB    |
|                                                                                                              | Earpiece Audio Path Gain    | Minimum Gain from AUX input, BOOST OFF                                           | −40.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from AUX input, BOOST OFF                                           | 6                   |                   | dB    |
|                                                                                                              |                             | Minimum Gain from CPI input                                                      | −28.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from CPI input                                                      | 18                  |                   | dB    |
|                                                                                                              |                             | Minimum Gain from MIC input using SIDETONE path w/ VCR <sub>MIC</sub> gain = 6dB | −18                 |                   | dB    |
|                                                                                                              |                             | Maximum Gain from MIC input using SIDETONE path w/ VCR <sub>MIC</sub> gain = 6dB | 12                  |                   | dB    |
|                                                                                                              | AUXOUT Audio Path Gain      | Minimum Gain from AUX input, BOOST OFF                                           | −46.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from AUX input, BOOST OFF                                           | 0                   |                   | dB    |
|                                                                                                              |                             | Minimum Gain from CPI input                                                      | −34.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from CPI input                                                      | 12                  |                   | dB    |
|                                                                                                              | CPOUT Audio Path Gain       | Minimum Gain from AUX input, BOOST OFF                                           | −46.5               |                   | dB    |
|                                                                                                              |                             | Maximum Gain from AUX input, BOOST OFF                                           | 0                   |                   | dB    |
|                                                                                                              |                             | Minimum Gain from MIC input                                                      | 6                   |                   | dB    |
|                                                                                                              |                             | Maximum Gain from MIC input                                                      | 36                  |                   | dB    |

**10.0 Electrical Characteristics** (Notes 1, 2) Unless otherwise stated **PLL\_V<sub>DD</sub> = 3.3V, D\_V<sub>DD</sub> = 3.3V, BB\_V<sub>DD</sub> = 1.8V, A\_V<sub>DD</sub> = 3.3V, LS\_V<sub>DD</sub> = 3.3V**. The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

| Symbol                     | Parameter                           | Conditions                                                                        | LM4935              |                   | Units |
|----------------------------|-------------------------------------|-----------------------------------------------------------------------------------|---------------------|-------------------|-------|
|                            |                                     |                                                                                   | Typical<br>(Note 6) | Limit<br>(Note 7) |       |
| Total DC Power Dissipation |                                     |                                                                                   |                     |                   |       |
|                            | MP3 Mode Power Dissipation          | DAC ( $f_S = 48\text{kHz}$ ) and HP ON                                            |                     |                   |       |
|                            |                                     | $f_{\text{MCLK}} = 12\text{MHz}$ , PLL OFF                                        | 57                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 13\text{MHz}$ , PLL ON<br>$f_{\text{PLLOUT}} = 12\text{MHz}$   | 63                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 19.2\text{MHz}$ , PLL ON<br>$f_{\text{PLLOUT}} = 12\text{MHz}$ | 64                  |                   | mW    |
|                            | FM Mode Power Dissipation           | AUX Inputs selected and HP ON                                                     |                     |                   |       |
|                            |                                     | $f_{\text{MCLK}} = 12\text{MHz}$ , PLL OFF                                        | 24                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 13\text{MHz}$ , PLL OFF                                        | 25                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 19.2\text{MHz}$ , PLL OFF                                      | 27                  |                   | mW    |
|                            | VOICE CODEC Mode Power Dissipation  | PCM DAC ( $f_S = 8\text{kHz}$ ) + ADC ( $f_S = 8\text{kHz}$ ) and EP ON           |                     |                   |       |
|                            |                                     | $f_{\text{MCLK}} = 12\text{MHz}$ , PLL OFF                                        | 49                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 13\text{MHz}$ , PLL OFF                                        | 50                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 19.2\text{MHz}$ , PLL ON<br>$f_{\text{PLLOUT}} = 12\text{MHz}$ | 56                  |                   | mW    |
|                            | VOICE Module Mode Power Dissipation | CP IN selected. EP and CPOUT ON                                                   |                     |                   |       |
|                            |                                     | $f_{\text{MCLK}} = 12\text{MHz}$ , PLL OFF                                        | 30                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 13\text{MHz}$ , PLL OFF                                        | 31                  |                   | mW    |
|                            |                                     | $f_{\text{MCLK}} = 19.2\text{MHz}$ , PLL OFF                                      | 33                  |                   | mW    |



## 10.0 Electrical Characteristics (Notes 1, 2) Unless otherwise stated $PLL\_V_{DD} = 3.3V$ , $D\_V_{DD} = 3.3V$ , $BB\_V_{DD} = 1.8V$ , $A\_V_{DD} = 3.3V$ , $LS\_V_{DD} = 3.3V$ . The following specifications apply for the circuit shown in *Figure 2* unless otherwise stated. Limits apply for 25°C. (Continued)

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits.

Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 2:** All voltages are measured with respect to the relevant  $V_{SS}$  pin unless otherwise specified. All grounds should be coupled as close as possible to the device.

**Note 3:** The maximum power dissipation must be de-rated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$  or the number given in Absolute Maximum Ratings, whichever is lower.

**Note 4:** Human body model: 100pF discharged through a 1.5k $\Omega$  resistor.

**Note 5:** Machine model: 220pF – 240pF discharged through all pins.

**Note 6:** Typical values are measured at 25°C and represent the parametric norm.

**Note 7:** Limits are guaranteed to Nationals AOQL (Average Outgoing Quality Level).

**Note 8:** Best operation is achieved by maintaining  $3.0V < A\_V_{DD} < 5.0$  and  $3.0V < D\_V_{DD} < 3.6V$  and  $A\_V_{DD} > D\_V_{DD}$ .

**Note 9:** Digital shutdown current is measured with system clock set for PLL output while the PLL is disabled.

**Note 10:** Disabling or bypassing the PLL will usually result in an improvement in noise measurements.

## 11.0 System Control

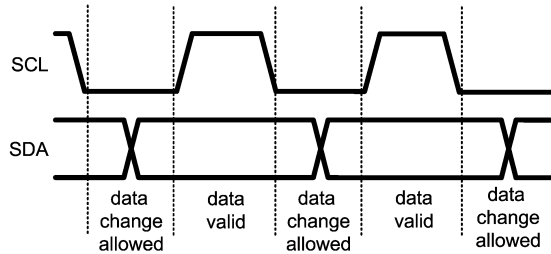
### Method 1. I<sup>2</sup>C Compatible Interface

#### 11.1 I<sup>2</sup>C SIGNALS

In I<sup>2</sup>C mode the LM4935 pin SCL is used for the I<sup>2</sup>C clock SCL and the pin SDA is used for the I<sup>2</sup>C data signal SDA. Both these signals need a pull-up resistor according to I<sup>2</sup>C specification. The I<sup>2</sup>C slave address for LM4935 is **0011010<sub>2</sub>**.

#### 11.2 I<sup>2</sup>C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

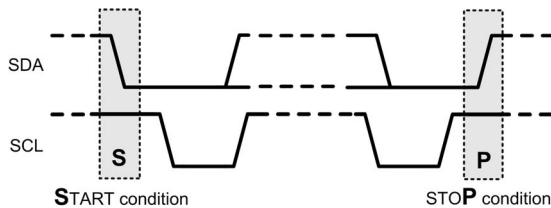


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I<sup>2</sup>C Signals: Data Validity

#### 11.3 I<sup>2</sup>C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

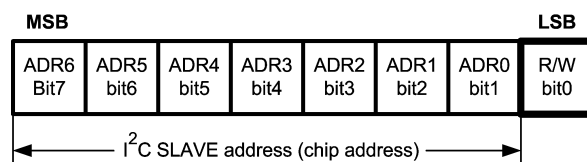


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#### 11.4 TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM4935 address is **0011010<sub>2</sub>**. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

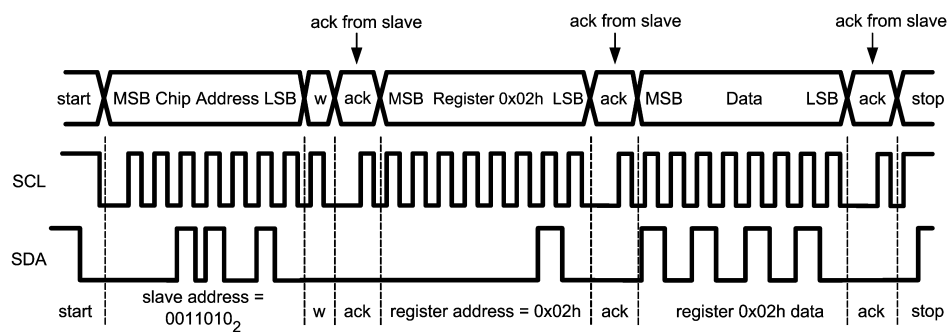


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I<sup>2</sup>C Chip Address

Register changes take an effect at the SCL rising edge during the last ACK from slave.

## 11.0 System Control (Continued)



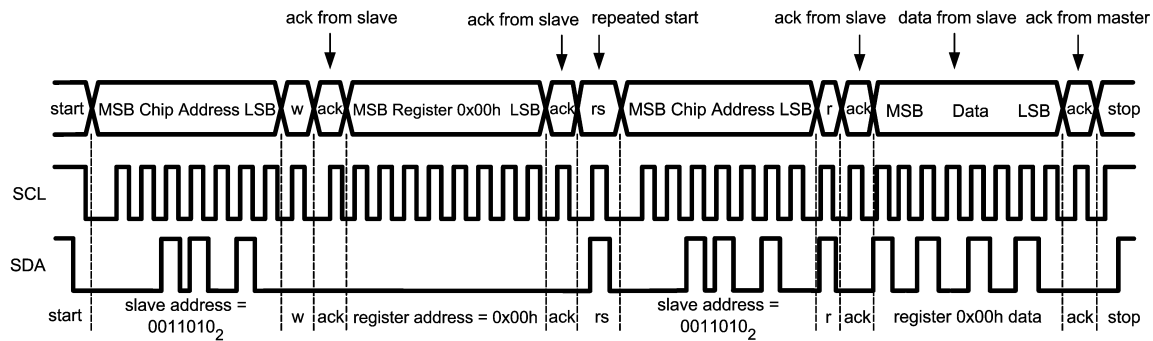
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w = write (SDA = "0")  
 r = read (SDA = "1")  
 ack = acknowledge (SDA pulled down by slave)  
 rs = repeated start

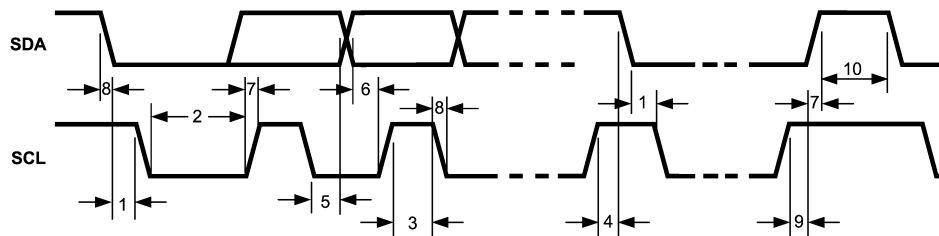
### Example I<sup>2</sup>C Write Cycle

## 11.0 System Control (Continued)

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



Example I²C Read Cycle



I²C Timing Diagram

### 11.5 I²C TIMING PARAMETERS

| Symbol | Parameter                                                       | Limit       |     | Units |
|--------|-----------------------------------------------------------------|-------------|-----|-------|
|        |                                                                 | Min         | Max |       |
| 1      | Hold Time (repeated) START Condition                            | 0.6         |     | μs    |
| 2      | Clock Low Time                                                  | 1.3         |     | μs    |
| 3      | Clock High Time                                                 | 600         |     | ns    |
| 4      | Setup Time for a Repeated START Condition                       | 600         |     | ns    |
| 5      | Data Hold Time (Output direction, delay generated by LM4935)    | 300         | 900 | ns    |
| 5      | Data Hold Time (Input direction, delay generated by the Master) | 0           | 900 | ns    |
| 6      | Data Setup Time                                                 | 100         |     | ns    |
| 7      | Rise Time of SDA and SCL                                        | $20+0.1C_b$ | 300 | ns    |
| 8      | Fall Time of SDA and SCL                                        | $15+0.1C_b$ | 300 | ns    |
| 9      | Set-up Time for STOP condition                                  | 600         |     | ns    |
| 10     | Bus Free Time between a STOP and a START Condition              | 1.3         |     | μs    |
| $C_b$  | Capacitive Load for Each Bus Line                               | 10          | 200 | pF    |

**NOTE:** Data guaranteed by design

## 11.0 System Control (Continued)

### Method 2. SPI/Microwire Control/3-wire Control

The LM4935 can be controlled via a three wire interface consisting of a clock, data and an active low chip\_select. To use this control method connect SPI\_MODE to BB\_V<sub>DD</sub> and use TEST\_MODE/ $\overline{\text{CS}}$  as the chip\_select as follows:

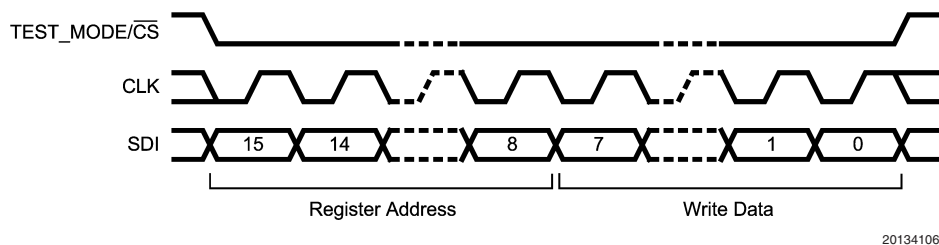


FIGURE 3. SPI Write Transaction

If the application requires read access to the register set; for example to determine the cause of an interrupt request or to read back a SAR data field, the GPIO2 pin can be configured as an SPI format serial data output by setting the GPIO\_SEL in the GPIO configuration register (0x1Ah) to SPI\_SDO. To perform a read rather than a write to a particular address the MSB of the register address field is set to a 1, this effectively mirrors the contents of the register field to read-only locations above 0x80h:

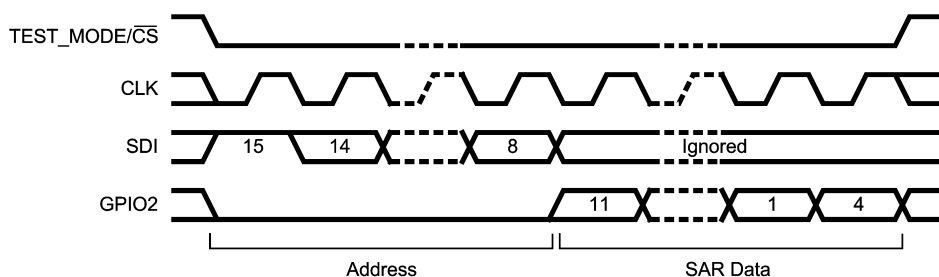


FIGURE 4. SPI Read Transaction

### Three Wire Mode Write Bus Timing

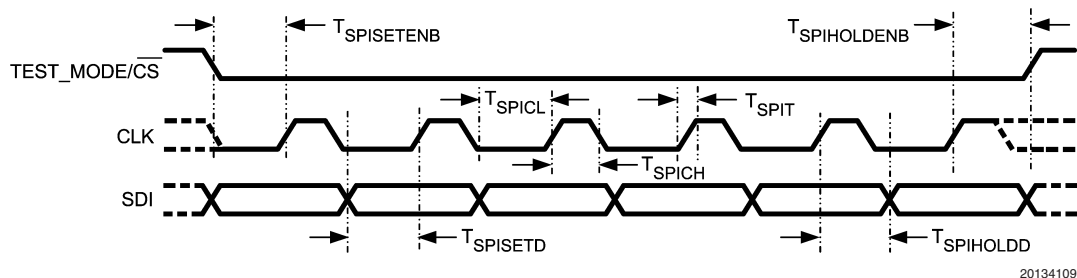


FIGURE 5. SPI Timing

## 12.0 Status & Control Registers

TABLE 1. Register Map

| Address | Register   | 7                    | 6            | 5                 | 4               | 3              | 2                | 1             | 0       |
|---------|------------|----------------------|--------------|-------------------|-----------------|----------------|------------------|---------------|---------|
| 0x00h   | BASIC      | OCL                  | STEREO       | CAP_SIZE          |                 | USE_OSC        | PLL_ENB          | CHP_MODE      |         |
| 0x01h   | CLOCKS     | R_DIV                |              |                   |                 |                |                  | ADCLK         | DACCLK  |
| 0x02h   | PLL_M      | PLLINPUT             | PLL_M        |                   |                 |                |                  |               | RSVD    |
| 0x03h   | PLL_N      | PLL_N                |              |                   |                 |                |                  |               |         |
| 0x04h   | PLL_P      | RSVD                 | Q_DIV        |                   |                 | PLL_P          |                  |               | RSVD    |
| 0x05h   | PLL_MOD    | RSVD                 | DITHER_LEVEL |                   | PLL_N_MOD       |                |                  |               |         |
| 0x06h   | ADC_1      | HPF_MODE             |              | SAMPLE_RATE       |                 | RIGHT          | LEFT             | CPI           | MIC     |
| 0x07h   | ADC_2      | IF216                | ADC_I2SM     | AGC_FRAME_TIME    |                 |                | ADCMUTE          | COMPND        | U/ALAW  |
| 0x08h   | AGC_1      | NOISE_GATE_THRESHOLD |              |                   | NG_ON           | AGC_TARGET     |                  |               | AGC_ENB |
| 0x09h   | AGC_2      | AGC_TIGHT            | AGC_DECAY    |                   |                 | AGC_MAX_GAIN   |                  |               |         |
| 0x0Ah   | AGC_3      | AGC_ATTACK           |              |                   | AGC_HOLD_TIME   |                |                  |               |         |
| 0x0Bh   | MIC_1      |                      | INT_EXT      | SE_DIFF           | MUTE            | PREAMP_GAIN    |                  |               |         |
| 0x0Ch   | MIC_2      |                      |              | BTN_DEBOUNCE_TIME |                 | BTNTYPE        | MIC_BIAS_VOLTAGE |               | VCMVOLT |
| 0x0Dh   | SIDETONE   |                      |              |                   |                 | SIDETONE_ATTEN |                  |               |         |
| 0x0Eh   | CP_INPUT   |                      |              | MUTE              | CPI_LEVEL       |                |                  |               |         |
| 0x0Fh   | AUX_LEFT   | AUX_DAC              | MUTE         | BOOST             | AUX_LEFT_LEVEL  |                |                  |               |         |
| 0x10h   | AUX_RIGHT  | AUX_DAC              | MUTE         | BOOST             | AUX_RIGHT_LEVEL |                |                  |               |         |
| 0x11h   | DAC        | DACMUTE              | BOOST        | USAXLVL           | DAC_LEVEL       |                |                  |               |         |
| 0x12h   | CP_OUTPUT  |                      |              |                   | MICGATE         | MUTE           | LEFT             | RIGHT         | MIC     |
| 0x13h   | AUX OUTPUT |                      |              |                   |                 | MUTE           | LEFT             | RIGHT         | CPI     |
| 0x14h   | LS_OUTPUT  |                      |              |                   |                 | MUTE           | LEFT             | RIGHT         | CPI     |
| 0x15h   | HP_OUTPUT  |                      |              |                   | MUTE            | LEFT           | RIGHT            | CPI           | SIDE    |
| 0x16h   | EP_OUTPUT  |                      |              |                   | MUTE            | LEFT           | RIGHT            | CPI           | SIDE    |
| 0x17h   | DETECT     |                      | HS_DBNC_TIME |                   |                 |                | TEMP_INT         | BTN_INT       | DET_INT |
| 0x18h   | STATUS     | GPIN                 | TEMP         | SARTRG2           | SARTRG1         | BTN            | MIC              | STEREO        | HEADSET |
| 0x19h   | AUDIO_IF   | I2S_SDO_DATA         |              | PCMCLMS           | PCMSYMS         | I2SCLKMS       | I2SWSMS          | AUDIO_IF_MODE |         |
| 0x1Ah   | GPIO       | GPIODATA             | PCM_LNG      | I2S_MODE          | SAR_CH_SEL      |                | GPIO_SEL         |               |         |
| 0x1Bh   | SAR_SLT0/1 | SLT1ENB              | SLOT1_FS     |                   |                 | SLT0ENB        | SLOT0_FS         |               |         |
| 0x1Ch   | SAR_SLT2/3 |                      |              | SLT2VBB           | SLT3ENB         | SLT2ENB        | SLOT2_FS         |               |         |
| 0x1Dh   | SAR_DATA_0 | SLOT0_DATA           |              |                   |                 |                |                  |               |         |
| 0x1Eh   | SAR_DATA_1 | SLOT1_DATA           |              |                   |                 |                |                  |               |         |
| 0x1Fh   | SAR_DATA_2 | SLOT2_DATA           |              |                   |                 |                |                  |               |         |
| 0x20h   | SAR_DATA_3 | SLOT3_DATA           |              |                   |                 |                |                  |               |         |
| 0x21h   | DC_VOL     |                      |              |                   |                 | MAX_LVL        |                  | EFFECT        | DCVLENB |
| 0x22h   | TRIG_1     | TRIG_1 [3:0]         |              |                   |                 | SOURCE         |                  | DIR           | ENB     |
| 0x23h   | TRIG_1_MSB | TRIG_1 [11:4]        |              |                   |                 |                |                  |               |         |
| 0x24h   | TRIG_2     | TRIG_2 [3:0]         |              |                   |                 | SOURCE         |                  | DIR           | ENB     |
| 0x25h   | TRIG_2_MSB | TRIG_2 [11:4]        |              |                   |                 |                |                  |               |         |
| 0x26h   | DEBUG      | GPIO_TEST_MODE       | RSVD         | RSVD              | RSVD            | SOFT RESET     | RSVD             | RSVD          | RSVD    |

For all registers, the default setting of data bits 7 through 0 are all set to zero.

RESERVED bits should always be set to zero.

## 12.0 Status & Control Registers (Continued)

### 12.1 BASIC CONFIGURATION REGISTER

This register is used to control the basic function of the chip.

**TABLE 2. BASIC (0x00h)**

| Bits | Field      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                       |                  |                                            |
|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------------------|--------------------------------------------|
| 1:0  | CHIP_MODE  | The LM4935 can be placed in one of four modes which dictate its basic operation. When a new mode is selected the LM4935 will change operation silently and will re-configure the power management profile automatically. The modes are described as follows:                                                                                                                                                                                                                                                                                                                                                 |                       |                  |                                            |
|      |            | CHIP MODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Audio System          | Detection System | Typical Application                        |
|      |            | 00 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Off                   | Off              | Power-down Mode                            |
|      |            | 01 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Off                   | On               | Stand-by mode with headset event detection |
|      |            | 10 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | On                    | Off              | Active without headset event detection     |
|      |            | 11 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | On                    | On               | Active with headset event detection        |
| 2    | PLL_ENABLE | If set the PLL can be used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                       |                  |                                            |
| 3    | USE_OSC    | If set the power management and control circuits will assume that no external clock is available and will resort to using an on-chip oscillator for SAR, headset detection and analog power management functions such as click and pop.                                                                                                                                                                                                                                                                                                                                                                      |                       |                  |                                            |
| 5:4  | CAP_SIZE   | Programs the extra delays required to stabilize once charge/discharge is complete, based on the size of the bypass capacitor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                       |                  |                                            |
|      |            | CAP_SIZE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Bypass Capacitor Size | Turn-off/on time |                                            |
|      |            | 00 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0.1 μF                | 45 ms/75 ms      |                                            |
|      |            | 01 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 1 μF                  | 45 ms/140 ms     |                                            |
|      |            | 10 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 2.2 μF                | 45 ms/260 ms     |                                            |
|      |            | 11 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 4.7 μF                | 45 ms/500 ms     |                                            |
| 6    | STEREO     | If set, the mixers assume that the signals on the left and right internal busses are highly correlated and when these signals are combined their levels are reduced by 6 dB to allow enough headroom for them to be summed at the Loudspeaker, Earpiece, CPOUT, and AUXOUT amplifiers. For the Headphone amplifier, if this bit is set, the left and right signal levels are routed to the corresponding left or right headphone output; if this bit is cleared, the left and the right signals are added and routed to both headphone outputs and their levels are reduced by 6dB to allow enough headroom. |                       |                  |                                            |
| 7    | OCL        | If set the part is placed in OCL (Output Capacitor Less) mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                       |                  |                                            |

For reliable headset / push button detection the following bits should be defined before enabling the headset detection system by setting bit 0 of CHIP\_MODE:

The OCL-bit (Cap / Capless headphone interface; bit 7 of this register)

The headset insert/removal debounce settings (bits 6:3 of DETECT (0x17h))

The BTN\_TYPE-bit (Parallel / Series push button type; bit 3 MIC\_2 register (0x0Ch))

The parallel push button debounce settings (bits 5:4 of MIC\_2 register (0x0Ch))

All register fields controlling the audio system should be defined before setting bit 1 of CHIP\_MODE and should not be altered while the audio sub-system is active.

If the analog or digital levels are below -12 dB then it is not necessary to set the stereo bit allowing greater output levels to be obtained for such signals.

## 12.0 Status & Control Registers (Continued)

### 12.2 CLOCKS CONFIGURATION REGISTER

This register is used to control the clocks throughout the chip.

**TABLE 3. CLOCKS (0x01h)**

| Bits | Field   | Description                                                         |
|------|---------|---------------------------------------------------------------------|
| 0    | DAC_CLK | Selects the clock to be used by the audio DAC system.               |
|      |         | DAC_CLK                                                             |
|      |         | 0 PLL Input (MCLK or I2S_CLK)                                       |
|      |         | 1 PLL Output                                                        |
| 1    | ADC_CLK | Selects the clock to be used by the audio ADC system.               |
|      |         | ADC_CLK                                                             |
|      |         | 0 MCLK                                                              |
|      |         | 1 PLL Output                                                        |
| 7:2  | R_DIV   | Programs the R divider (divides from an expected 12.000 MHz input). |
|      |         | R_DIV                                                               |
|      |         | 0 Bypass                                                            |
|      |         | 1 Bypass                                                            |
|      |         | 2 1.5                                                               |
|      |         | 3 2                                                                 |
|      |         | 4 2.5                                                               |
|      |         | 5 3                                                                 |
|      |         | 6 3.5                                                               |
|      |         | 7 4                                                                 |
|      |         | 8 4.5                                                               |
|      |         | 9 5                                                                 |
|      |         | 10 5.5                                                              |
|      |         | 11 6                                                                |
|      |         | 12 6.5                                                              |
|      |         | 13 to 61 7 to 31                                                    |
|      |         | 62 31.5                                                             |
|      |         | 63 32                                                               |



## 12.0 Status & Control Registers (Continued)

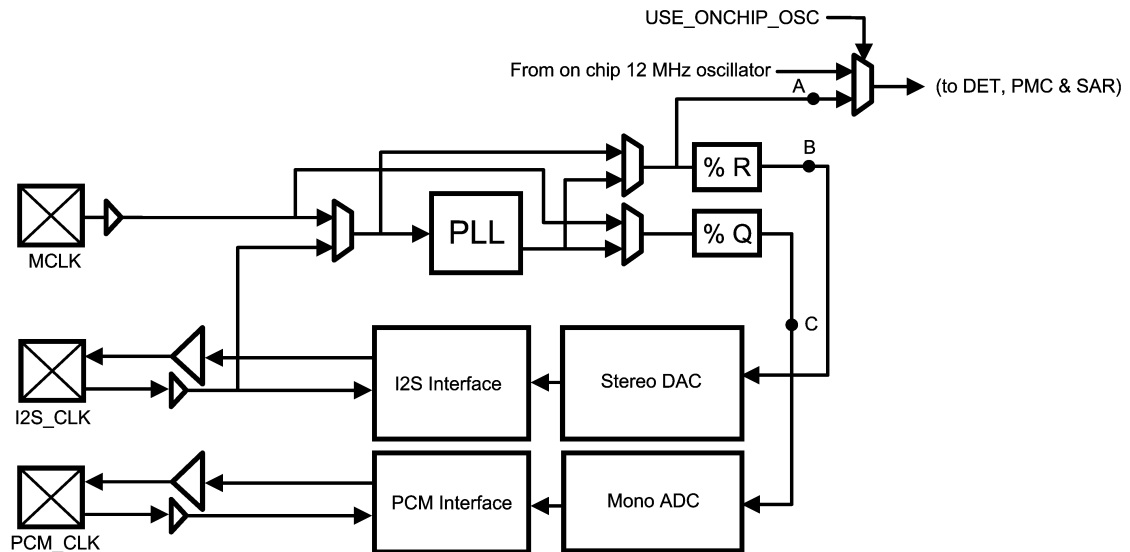
### 12.3 LM4935 CLOCK NETWORK

The audio ADC operates at  $125 \times f_s$ , so it requires a 1.000 MHz clock to sample at 8 kHz (at point **C** as marked on the following diagram). The stereo DAC operates at  $250 \times f_s$ , i.e. 12.000 MHz (at point **B**) for 48 kHz data. It is expected that the PLL is used to drive the audio system unless a 12.000 MHz master clock is supplied and the sample rate is always a multiple of 8 kHz, in which case the PLL can be bypassed to reduce power, clock division instead being performed by the Q and R dividers. The PLL can also use the I2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL and the audio ADC either uses the PLL output divided by  $2 \times \text{FSDAC}/\text{FSADC}$  or a system clock divided by Q, this allows  $n \times 8$  kHz recording and 44.1 kHz playback.

MCLK must be less than or equal to 30 MHz, the I2S clock should be an integer multiple of the DAC's sampling frequency and should be below 6 MHz.

When using the Class D amplifier with the DAC the Class D clock generator will assume 12 MHz at point **A**, if this is not the case then the DAC and power stage may become unsynchronized and SNR performance may be reduced.

The LM4935 is designed to work from a 12.000 MHz or 11.025 MHz clock at point **A**. This is used to drive the power management and control logic. Performance may not meet the electrical specifications if the frequency at this point deviates significantly beyond this range.



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FIGURE 6. LM4935 Clock Network

## 12.0 Status & Control Registers (Continued)

### 12.4 COMMON CLOCK SETTINGS FOR THE DAC & ADC

The DAC has an over sampling rate of 125 but requires a  $250 \times f_s$  clock at point **B**. This allows a simple clocking solution as it will work from 12.000 MHz (common in most systems with Bluetooth or USB) at 48 kHz exactly, the following table describes the clock required at point **B** for various clock sample rates in the different DAC modes:

**TABLE 4. Common DAC Clock Frequencies**

| DAC Sample Rate (kHz) | Clock Required at B (MHz) |
|-----------------------|---------------------------|
| 8                     | 2                         |
| 11.025                | 2.75625                   |
| 12                    | 3                         |
| 16                    | 4                         |
| 22.05                 | 5.5125                    |
| 24                    | 6                         |
| 32                    | 8                         |
| 44.1                  | 11.025                    |
| 48                    | 12                        |

The ADC has an over sampling ratio of 125 so the table below shows the required clock frequency at point **C**.

**TABLE 5. Common ADC Clock Frequencies**

| ADC Sample Rate (kHz) | Clock Required at C (MHz) |
|-----------------------|---------------------------|
| 8                     | 1                         |
| 11.025                | 1.378125                  |
| 12                    | 1.5                       |
| 16                    | 2                         |
| 22.05                 | 2.75625                   |
| 24                    | 3                         |

Methods for producing these clock frequencies are described in the PLL Section.

## 12.0 Status & Control Registers (Continued)

### 12.5 PLL M DIVIDER CONFIGURATION REGISTER

This register is used to control the input section of the PLL.

**TABLE 6. PLL\_M (0x02h)**

| Bits | Field     | Description                                           |                     |
|------|-----------|-------------------------------------------------------|---------------------|
| 0    | RSVD      | RESERVED                                              |                     |
| 6:1  | PLL_M     | PLL_M                                                 | Input Divider Value |
|      |           | 0                                                     | 1                   |
|      |           | 1                                                     | 2                   |
|      |           | 2                                                     | 3                   |
|      |           | 3                                                     | 4                   |
|      |           | 4...62                                                | 5...63              |
|      |           | 63                                                    | 64                  |
| 7    | PLL_INPUT | Programs the PLL input multiplexer to select between: |                     |
|      |           | PLL_INPUT                                             | PLL Input Source    |
|      |           | 0                                                     | MCLK                |
|      |           | 1                                                     | I2S_CLK             |

The M divider should be set such that the output of the divider is between 0.5 MHz and 5 MHz.

The division of the M divider is derived from PLL\_M such that:

$$M = \text{PLL\_M} + 1$$

**Note 11:** See **Further Notes on PLL Programming** for more detail.

## 12.0 Status & Control Registers (Continued)

### 12.6 PLL N DIVIDER CONFIGURATION REGISTER

This register is used to control the feedback divider of the PLL.

**TABLE 7. PLL\_N (0x03h)**

| Bits | Field | Description                                   |                        |
|------|-------|-----------------------------------------------|------------------------|
| 7:0  | PLL_N | Programs the PLL feedback divider as follows: |                        |
|      |       | PLL_N                                         | Feedback Divider Value |
|      |       | 0 to 10                                       | 10                     |
|      |       | 11                                            | 11                     |
|      |       | 12                                            | 12                     |
|      |       | 13                                            | 13                     |
|      |       | 14                                            | 14                     |
|      |       | ...                                           | ...                    |
|      |       | 249                                           | 249                    |
|      |       | 250 to 255                                    | 250                    |

The N divider should be set such that the output of the divider is between 0.5 MHz and 5 MHz.  $(F_{in}/M)*N$  will be the target resting VCO frequency,  $F_{VCO}$ . The N divider should be set such that  $40 \text{ MHz} < (F_{in}/M)*N < 60 \text{ MHz}$ .  $F_{in}/M$  is often referred to as  $F_{comp}$  (comparison frequency) or  $F_{ref}$  (reference frequency), in this document  $F_{comp}$  is used.

The integer division of the N divider is derived from PLL\_N such that:

$$\text{For } 9 < \text{PLL\_N} < 251: N = \text{PLL\_N}$$

**Note 12:** See **Further Notes on PLL Programming** for further details.

## 12.0 Status & Control Registers (Continued)

### 12.7 PLL P DIVIDER CONFIGURATION REGISTER

This register is used to control the output divider of the PLL.

**TABLE 8. PLL\_P (0x04h)**

| Bits | Field | Description                                                         |
|------|-------|---------------------------------------------------------------------|
| 0    | RSVD  | RESERVED                                                            |
| 3:1  | PLL_P | PLL_P                                                               |
|      |       | Output Divider Value                                                |
|      |       | 000 <sub>2</sub>                                                    |
|      |       | 001 <sub>2</sub>                                                    |
|      |       | 010 <sub>2</sub>                                                    |
|      |       | 011 <sub>2</sub>                                                    |
|      |       | 100 <sub>2</sub>                                                    |
|      |       | 101 <sub>2</sub>                                                    |
|      |       | 110 <sub>2</sub>                                                    |
|      |       | 111 <sub>2</sub>                                                    |
| 6:4  | Q_DIV | Programs the Q Divider (divides from an expected 12.000 MHz input). |
|      |       | Q_DIV                                                               |
|      |       | Divide Value                                                        |
|      |       | 000 <sub>2</sub>                                                    |
|      |       | 001 <sub>2</sub>                                                    |
|      |       | 010 <sub>2</sub>                                                    |
|      |       | 011 <sub>2</sub>                                                    |
|      |       | 100 <sub>2</sub>                                                    |
|      |       | 101 <sub>2</sub>                                                    |
|      |       | 110 <sub>2</sub>                                                    |
|      |       | 111 <sub>2</sub>                                                    |
| 7    | RSVD  | RESERVED                                                            |

The division of the P divider is derived from PLL\_P such that:

$$P = \text{PLL\_P} + 1$$

**Note 13:** See **Further Notes on PLL Programming** for more details.

## 12.0 Status & Control Registers (Continued)

### 12.8 PLL N MODULUS CONFIGURATION REGISTER

This register is used to control the modulation applied to the feedback divider of the PLL.

**TABLE 9. PLL\_N\_MOD (0x05h)**

| Bits | Field        | Description                                           |
|------|--------------|-------------------------------------------------------|
| 4:0  | PLL_N_MOD    | Programs the PLL N divider's fractional component:    |
|      |              | PLL_N_MOD                                             |
|      |              | Fractional Addition                                   |
|      |              | 0                                                     |
|      |              | 0/32                                                  |
|      |              | 1                                                     |
| 6:5  | DITHER_LEVEL | 1/32                                                  |
|      |              | 2 to 30                                               |
|      |              | 2/32 to 30/32                                         |
|      |              | 31                                                    |
|      |              | 31/32                                                 |
|      |              |                                                       |
| 6:5  | DITHER_LEVEL | Allows control over the dither used by the N divider: |
|      |              | DITHER_LEVEL                                          |
|      |              | Value                                                 |
|      |              | 00 <sub>2</sub>                                       |
|      |              | Medium                                                |
|      |              | 01 <sub>2</sub>                                       |
| 7    | RSVD         | Small                                                 |
|      |              | 10 <sub>2</sub>                                       |
|      |              | Large                                                 |
|      |              | 11 <sub>2</sub>                                       |
|      |              | Off                                                   |
| 7    | RSVD         | RESERVED                                              |

The complete N divider is a fractional divider as such:

$$N = \text{PLL\_N} + \text{PLL\_N\_MOD}/32$$

If the modulus input is zero then the N divider is simply an integer N divider. The output from the PLL is determined by the following formula:

$$F_{\text{out}} = (F_{\text{in}} * N) / (M * P)$$

**Note 14:** See **Further Notes on PLL Programming** for more details.

## 12.0 Status & Control Registers (Continued)

### 12.9 FURTHER NOTES ON PLL PROGRAMMING

The sigma-delta PLL is designed to drive audio circuits requiring accurate clock frequencies of up to 30 MHz with frequency errors noise-shaped away from the audio band. The 5 bits of modulus control provide exact synchronization of 48 kHz and 44.1 kHz sample rates from any common system clock. In systems where an isochronous I2S data stream is the source of data to the DAC a clock synchronous to the sample rate should be used as input to the PLL (typically the I2S clock). If no isochronous source is available then the PLL can be used to obtain a clock that is accurate to within 1 Hz of the correct sample rate although this is highly unlikely to be a problem.

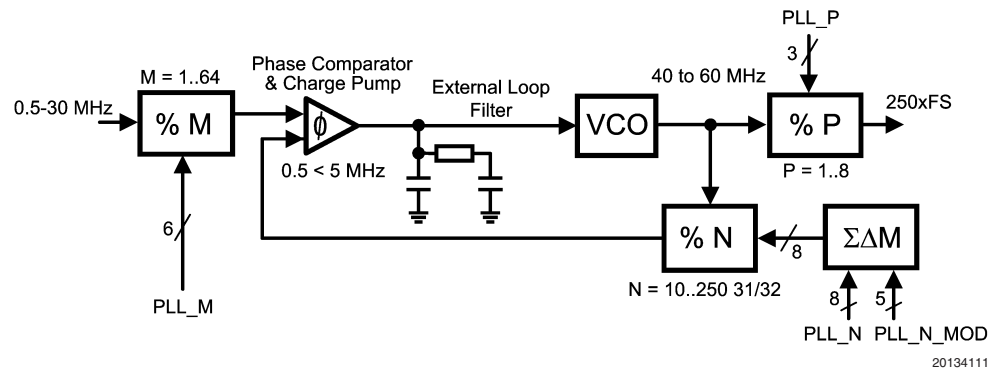


FIGURE 7. PLL Overview

TABLE 10. Example PLL Settings for 48 kHz and 44.1 kHz Sample Rates

| F <sub>in</sub> (MHz) | F <sub>s</sub> (kHz) | M  | N        | P | PLL_M | PLL_N | PLL_N_MOD | PLL_P | F <sub>out</sub> (MHz) |
|-----------------------|----------------------|----|----------|---|-------|-------|-----------|-------|------------------------|
| 11                    | 48                   | 11 | 60       | 5 | 10    | 60    | 0         | 4     | 12                     |
| 12.288                | 48                   | 4  | 19.53125 | 5 | 3     | 19    | 17        | 4     | 12                     |
| 13                    | 48                   | 13 | 60       | 5 | 12    | 60    | 0         | 4     | 12                     |
| 14.4                  | 48                   | 9  | 37.5     | 5 | 8     | 37    | 16        | 4     | 12                     |
| 16.2                  | 48                   | 27 | 100      | 5 | 26    | 100   | 0         | 4     | 12                     |
| 16.8                  | 48                   | 14 | 50       | 5 | 13    | 50    | 0         | 4     | 12                     |
| 19.2                  | 48                   | 13 | 40.625   | 5 | 12    | 40    | 20        | 4     | 12                     |
| 19.44                 | 48                   | 27 | 100      | 6 | 26    | 100   | 0         | 5     | 12                     |
| 19.68                 | 48                   | 21 | 64.03125 | 5 | 20    | 64    | 1         | 4     | 12                     |
| 19.8                  | 48                   | 17 | 51.5     | 5 | 16    | 51    | 16        | 4     | 12                     |
| 11                    | 44.1                 | 11 | 55.125   | 5 | 10    | 55    | 4         | 4     | 11.025                 |
| 11.2896               | 44.1                 | 8  | 39.0625  | 5 | 7     | 39    | 2         | 4     | 11.025                 |
| 12                    | 44.1                 | 5  | 22.96875 | 5 | 4     | 22    | 31        | 4     | 11.025                 |
| 13                    | 44.1                 | 13 | 55.125   | 5 | 12    | 55    | 4         | 4     | 11.025                 |
| 14.4                  | 44.1                 | 12 | 45.9375  | 5 | 11    | 45    | 30        | 4     | 11.025                 |
| 16.2                  | 44.1                 | 9  | 30.625   | 5 | 8     | 9     | 20        | 4     | 11.025                 |
| 16.8                  | 44.1                 | 17 | 55.78125 | 5 | 16    | 30    | 25        | 4     | 11.025                 |
| 19.2                  | 44.1                 | 16 | 45.9375  | 5 | 15    | 45    | 30        | 4     | 11.025                 |
| 19.44                 | 44.1                 | 14 | 39.6875  | 5 | 13    | 39    | 22        | 4     | 11.025                 |
| 19.68                 | 44.1                 | 21 | 47.0625  | 4 | 20    | 47    | 2         | 3     | 11.025                 |
| 19.8                  | 44.1                 | 11 | 30.625   | 5 | 10    | 30    | 204       | 4     | 11.025                 |

## 12.0 Status & Control Registers (Continued)

These tables cover the most common applications, obtaining clocks for derivative sample rates such as 22.05 kHz should be done by increasing the P divider value or using the R/Q dividers.

If the user needs to obtain a clock unrelated to those described above, the following method is advised. An example of obtaining 12.000 MHz from 1.536 MHz is shown below (this is typical for deriving DAC clocks from I2S datastreams).

Choose a small range of P so that the VCO frequency is swept between 40 MHz and 60 MHz. So for P = 3 to 5, sweep the M inputs from 1 to 3. The most accurate N and N\_MOD can be calculated by:

$$N = \text{FLOOR}(((F_{\text{out}}/F_{\text{in}})*(P*M)),1)$$

$$N\_MOD = \text{ROUND}(32*(((F_{\text{out}}/F_{\text{in}})*(P*M)-N),0)$$

This shows that setting M = 1, N = 39+1/16, P = 5 (i.e. PLL\_M = 0, PLL\_N = 39, PLL\_N\_MOD = 2, & PLL\_P = 4) gives a comparison frequency of 1.5 MHz, a VCO frequency of 60 MHz and an output frequency of 12.000 MHz. The same settings can be used to get 11.025 from 1.4112 MHz for 44.1 kHz sample rates.

Care must be taken when synchronization of isochronous data is not possible, i.e. when the PLL has to be used but an exact frequency match cannot be found. The I2S should be master on the LM4935 so that the data source can support appropriate SRC as required. This method should only be used with data being read on demand to eliminate sample rate mismatch problems.

Where a system clock exists at an integer multiple of the required ADC or DAC clock rate it is preferable to use this rather than the PLL. The LM4935 is designed to work in 8, 12, 16, 24, 48 kHz modes from a 12 MHz clock and 8, 13, 26, 52 kHz modes from a 13 MHz clock without the use of the PLL. This saves power and reduces clock jitter which can affect SNR.

The actual ADC and DAC sample rates are set up by the PLL and internal clock dividers.



## 12.0 Status & Control Registers (Continued)

### 12.10 ADC\_1 CONFIGURATION REGISTER

This register is used to control the LM4935's audio ADC.

**TABLE 11. ADC\_1 (0x06h)**

| Bits | Field           | Description                                                                                                                                                                                      |
|------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | MIC_SELECT      | If set the microphone preamp output is added to the ADC input signal.                                                                                                                            |
| 1    | CPI_SELECT      | If set the cell phone input is added to the ADC input signal.                                                                                                                                    |
| 2    | LEFT_SELECT     | If set the left stereo bus is added to the ADC input signal.                                                                                                                                     |
| 3    | RIGHT_SELECT    | If set the right stereo bus is added to the ADC input signal.                                                                                                                                    |
| 5:4  | ADC_SAMPLE_RATE | Programs the closest expected sample rate of the mono ADC, which is a variable required by the AGC algorithm whenever the AGC is in use. This does not set the sample rate of the mono ADC.      |
|      |                 | ADC_SAMPLE_RATE      Sample Rate                                                                                                                                                                 |
|      |                 | 00 <sub>2</sub> 8 kHz                                                                                                                                                                            |
|      |                 | 01 <sub>2</sub> 12 kHz                                                                                                                                                                           |
|      |                 | 10 <sub>2</sub> 16 kHz                                                                                                                                                                           |
|      |                 | 11 <sub>2</sub> 24 kHz                                                                                                                                                                           |
| 7:6  | HPF_MODE        | Sets the HPF of the ADC                                                                                                                                                                          |
|      |                 | HPF-MODE      HPF Response                                                                                                                                                                       |
|      |                 | 00 <sub>2</sub> No HPF                                                                                                                                                                           |
|      |                 | 01 <sub>2</sub> F <sub>S</sub> = 8 kHz, –0.5 dB @ 300 Hz, Notch @ 55 Hz<br>F <sub>S</sub> = 12 kHz, –0.5 dB @ 450 Hz, Notch @ 82 Hz<br>F <sub>S</sub> = 16 kHz, –0.5 dB @ 600 Hz, Notch @ 110 Hz |
|      |                 | 10 <sub>2</sub> F <sub>S</sub> = 8 kHz, –0.5 dB @ 150 Hz, Notch @ 27 Hz<br>F <sub>S</sub> = 12 kHz, –0.5 dB @ 225 Hz, Notch @ 41 Hz<br>F <sub>S</sub> = 16 kHz, –0.5 dB @ 300 Hz, Notch @ 55 Hz  |
|      |                 | 11 <sub>2</sub> No HPF                                                                                                                                                                           |

## 12.0 Status & Control Registers (Continued)

### 12.11 ADC\_2 CONFIGURATION REGISTER

This register is used to control the LM4935's audio ADC.

**TABLE 12. ADC\_2 (0x07h)**

| Bits | Field            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | ULAW/ALAW        | If COMPAND is set then the data across the PCM interface to the DAC and from the ADC is companded as follows:                                                                                                                                                                                                                                                                                                                                                             |
|      |                  | ULAW/ALAW                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |                  | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |                  | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1    | COMPAND          | If set the 16 bit PCM data from the ADC is companded before the PCM interface and the PCM data to the DAC is treated as companded data.                                                                                                                                                                                                                                                                                                                                   |
| 2    | ADC_MUTE         | If set the analog inputs to the ADC are muted.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 5:3  | AGC_FRAME_TIME   | This sets the frame time to be used by the AGC algorithm. In a given frame, the AGC's peak detector determines the peak value of the incoming microphone audio signal and compares this value to the target value of the AGC defined by AGC_TARGET (bits [3:1] of register (0x08h)) in order to adjust the microphone preamplifiers gain accordingly. AGC_FRAME_TIME basically sets the sample rate of the AGC to adjust for a wide variety of speech patterns. (Note 15) |
|      |                  | AGC_FRAME_TIME                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      |                  | 000 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 001 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 010 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 011 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 100 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 101 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 110 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                  | 111 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 6    | ADC_I2S_M        | If set the DAC clock system is enabled to drive the I2S in master mode. The Point B frequency should be double that at Point C. This bit should be set when using the I2S interface in master mode to read SAR information whenever both the audio ADC and DAC are inactive.                                                                                                                                                                                              |
| 7    | AUDIO_IF_2_16BIT | If set the PCM and I2S interfaces are 16 bits per word in master mode. The 2 last clock cycles per word are 25% shorter to allow generation.                                                                                                                                                                                                                                                                                                                              |

**Note 15:** Refer to the **AGC overview** for further detail.

## 12.0 Status & Control Registers (Continued)

### 12.12 AGC\_1 CONFIGURATION REGISTER

This register is used to control the LM4935's Automatic Gain Control. (Note 16)

**TABLE 13. AGC\_1 (0x08h)**

| Bits | Field            | Description                                                                                                                                                                                                                                                                                                                                                    |
|------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | AGC_ENABLE       | If set the AGC controls the analog microphone preamplifier gain into the system. The microphone input must be passed to the ADC.                                                                                                                                                                                                                               |
| 3:1  | AGC_TARGET       | Programs the target level of the AGC. This will depend on the expected transients and desired headroom. Refer to AGC_TIGHT (bit 7 of 0x09h) for more detail.                                                                                                                                                                                                   |
|      |                  | AGC_TARGET                                                                                                                                                                                                                                                                                                                                                     |
|      |                  | 000 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 001 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 010 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 011 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 100 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 101 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 110 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 111 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
| 4    | NOISE_GATE_ON    | If set, signals below the noise gate threshold are muted. The noise gate is only activated after a set period of signal absence.                                                                                                                                                                                                                               |
| 7:5  | NOISE_GATE_THRES | This field sets the expected background noise level relative to the peak signal level. The sole presence of signals below this level will not result in an AGC gain change of the input and will be gated from the ADC output if the NOISE_GATE_ON is set. This level must be set even if the noise gate is not in use as it is required by the AGC algorithm. |
|      |                  | NOISE_GATE_THRES                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 000 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 001 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 010 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 011 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 100 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 101 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 110 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |
|      |                  | 111 <sub>2</sub>                                                                                                                                                                                                                                                                                                                                               |

**Note 16:** See the **AGC overview**.

## 12.0 Status & Control Registers (Continued)

### 12.13 AGC\_2 CONFIGURATION REGISTER

This register is used to control the LM4935's Automatic Gain Control.

**TABLE 14. AGC\_2 (0x09h)**

| Bits | Field         | Description                                                                                              |                       |           |
|------|---------------|----------------------------------------------------------------------------------------------------------|-----------------------|-----------|
| 3:0  | AGC_MAX_GAIN  | This programs the maximum gain that the AGC algorithm can apply to the microphone preamplifier.          |                       |           |
|      |               | AGC_MAX_GAIN                                                                                             | Max Preamplifier Gain |           |
|      |               | 0000 <sub>2</sub>                                                                                        | 6 dB                  |           |
|      |               | 0001 <sub>2</sub>                                                                                        | 8 dB                  |           |
|      |               | 0010 <sub>2</sub>                                                                                        | 10 dB                 |           |
|      |               | 0011 <sub>2</sub>                                                                                        | 12 dB                 |           |
|      |               | 0100 <sub>2</sub> to 1100 <sub>2</sub>                                                                   | 14 dB to 30 dB        |           |
|      |               | 1101 <sub>2</sub>                                                                                        | 32 dB                 |           |
|      |               | 1110 <sub>2</sub>                                                                                        | 34 dB                 |           |
|      |               | 1111 <sub>2</sub>                                                                                        | 36 dB                 |           |
| 6:4  | AGC_DECAY     | Programs the speed at which the AGC will increase gains if it detects the input level is a quiet signal. |                       |           |
|      |               | AGC_DECAY                                                                                                | Step Time (ms)        |           |
|      |               | 000 <sub>2</sub>                                                                                         | 32                    |           |
|      |               | 001 <sub>2</sub>                                                                                         | 64                    |           |
|      |               | 010 <sub>2</sub>                                                                                         | 128                   |           |
|      |               | 011 <sub>2</sub>                                                                                         | 256                   |           |
|      |               | 100 <sub>2</sub>                                                                                         | 512                   |           |
|      |               | 101 <sub>2</sub>                                                                                         | 1024                  |           |
|      |               | 110 <sub>2</sub>                                                                                         | 2048                  |           |
|      |               | 111 <sub>2</sub>                                                                                         | 4096                  |           |
| 7    | AGC_TIGHT     | If set the AGC algorithm controls the microphone preamplifier more exactly. (Note 17)                    |                       |           |
|      | AGC_TIGHT = 0 | AGC_TARGET                                                                                               | Min Level             | Max Level |
|      |               | 000 <sub>2</sub>                                                                                         | –6 dB                 | –3 dB     |
|      |               | 001 <sub>2</sub>                                                                                         | –8 dB                 | –4 dB     |
|      |               | 010 <sub>2</sub>                                                                                         | –10 dB                | –5 dB     |
|      |               | 011 <sub>2</sub>                                                                                         | –12 dB                | –6 dB     |
|      |               | 100 <sub>2</sub>                                                                                         | –14 dB                | –7 dB     |
|      |               | 101 <sub>2</sub>                                                                                         | –16 dB                | –8 dB     |
|      |               | 110 <sub>2</sub>                                                                                         | –18 dB                | –9 dB     |
|      |               | 111 <sub>2</sub>                                                                                         | –20 dB                | –10 dB    |
|      | AGC_TIGHT = 1 | 000 <sub>2</sub>                                                                                         | –6 dB                 | –3 dB     |
|      |               | 001 <sub>2</sub>                                                                                         | –8 dB                 | –5 dB     |
|      |               | 010 <sub>2</sub>                                                                                         | –10 dB                | –7 dB     |
|      |               | 011 <sub>2</sub>                                                                                         | –12 dB                | –9 dB     |
|      |               | 100 <sub>2</sub>                                                                                         | –14 dB                | –11 dB    |
|      |               | 101 <sub>2</sub>                                                                                         | –16 dB                | –13 dB    |
|      |               | 110 <sub>2</sub>                                                                                         | –18 dB                | –15 dB    |
|      |               | 111 <sub>2</sub>                                                                                         | –20 dB                | –17 dB    |

**Note 17:** The AGC can be used to control the analog path of the microphone to the output stages or to optimize the microphone path for recording on the ADC. When the analog path is used this bit should be set to ensure the target is tightly adhered to. If the ADC is the only destination of the microphone or the desired analog mixer level is line level then AGC\_TIGHT should be cleared, allowing greater dynamic range of the recorded signal. For further details see the **AGC overview**.

## 12.0 Status & Control Registers (Continued)

### 12.14 AGC\_3 CONFIGURATION REGISTER

This register is used to control the LM4935's Automatic Gain Control. (Note 18)

**TABLE 15. AGC\_3 (0x0Ah)**

| Bits | Field        | Description                                                                                                     |
|------|--------------|-----------------------------------------------------------------------------------------------------------------|
| 4:0  | AGC_HOLDTIME | Programs the amount of delay before the AGC algorithm begins to adjust the gain of the microphone preamplifier. |
|      |              | AGC_HOLDTIME                                                                                                    |
|      |              | No. of speech segments                                                                                          |
|      |              | 00000 <sub>2</sub>                                                                                              |
|      |              | 0                                                                                                               |
|      |              | 00001 <sub>2</sub>                                                                                              |
|      |              | 1                                                                                                               |
|      |              | 00010 <sub>2</sub>                                                                                              |
|      |              | 2                                                                                                               |
|      |              | 00011 <sub>2</sub>                                                                                              |
|      |              | 3                                                                                                               |
|      |              | 00100 <sub>2</sub> to 11100 <sub>2</sub>                                                                        |
|      |              | 4 to 28                                                                                                         |
|      |              | 11101 <sub>2</sub>                                                                                              |
|      |              | 29                                                                                                              |
|      |              | 11110 <sub>2</sub>                                                                                              |
|      |              | 30                                                                                                              |
|      |              | 11111 <sub>2</sub>                                                                                              |
|      |              | 31                                                                                                              |
| 7:5  | AGC_ATTACK   | Programs the speed at which the AGC will reduce gains if it detects the input level is too large.               |
|      |              | AGC_ATTACK                                                                                                      |
|      |              | Step Time (ms)                                                                                                  |
|      |              | 000 <sub>2</sub>                                                                                                |
|      |              | 32                                                                                                              |
|      |              | 001 <sub>2</sub>                                                                                                |
|      |              | 64                                                                                                              |
|      |              | 010 <sub>2</sub>                                                                                                |
|      |              | 128                                                                                                             |
|      |              | 011 <sub>2</sub>                                                                                                |
|      |              | 256                                                                                                             |
|      |              | 100 <sub>2</sub>                                                                                                |
|      |              | 512                                                                                                             |
|      |              | 101 <sub>2</sub>                                                                                                |
|      |              | 1024                                                                                                            |
|      |              | 110 <sub>2</sub>                                                                                                |
|      |              | 2048                                                                                                            |
|      |              | 111 <sub>2</sub>                                                                                                |
|      |              | 4096                                                                                                            |

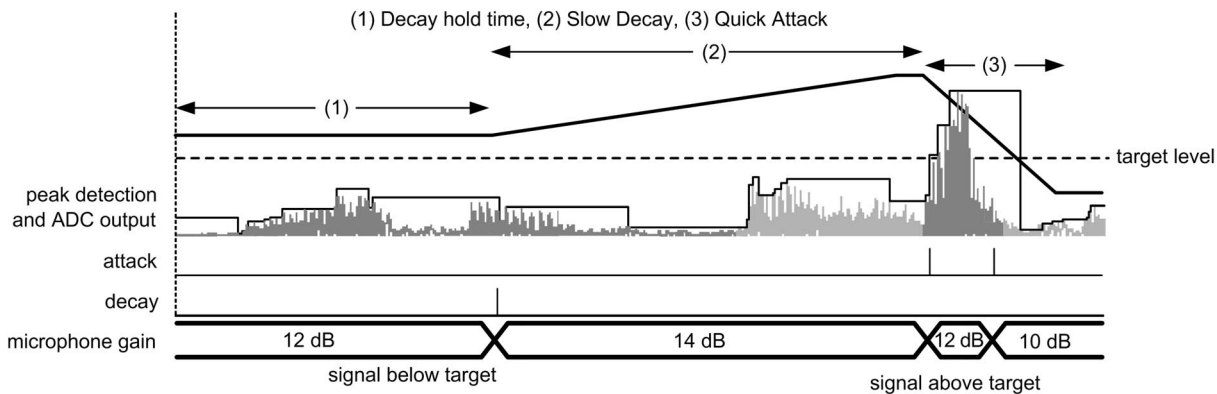
**Note 18:** See the **AGC overview**.

## 12.0 Status & Control Registers (Continued)

### 12.15 AGC OVERVIEW

The Automatic Gain Control (AGC) system can be used to optimize the dynamic range of the ADC for voice data when the level of the source is unknown. A target level for the output is set so that any transients on the input won't clip during normal operation. The AGC circuit then compares the output of the ADC to this level and increases or decreases the gain of the microphone preamplifier to compensate. If the audio from the microphone is to be output digitally through the ADC then the full dynamic range of the ADC can be used automatically. If the output is through the analog mixer then the ADC is used to monitor the microphone level. In this case, the analog dynamic range is less important than the absolute level, so *AGC\_TIGHT* should be set to tie transients closely to the target level.

To ensure that the system doesn't reduce the quality of the speech by constantly modulating the microphone preamplifier gain, the ADC output is passed through an envelope detector. This frames the output of the ADC into time segments roughly equal to the phonemes found in speech (*AGC\_FRAME\_TIME*). To calculate this, the circuit must also know the sample rate of the data from the ADC (*ADC\_SAMPLERATE*). If after a programmable number of these segments (*AGC\_HOLDTIME*), the level is consistently below target, the gain will be increased at a programmable rate (*AGC\_DECAY*). If the signal ever exceeds the target level (*AGC\_TARGET*) then the gain of the microphone is reduced immediately at a programmable rate (*AGC\_ATTACK*). This is demonstrated below:



AGC Operation Example

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The signal in the above example starts with a small analog input which, after the hold time has timed out, triggers a rise in the gain ((1) → (2)). After some time the real analog input increases and it reaches the threshold for a gain reduction which decreases the gain at a faster rate ((2) → (3)) to allow the elimination of typical popping noises.

Only ADC outputs that are considered signal (rather than noise) are used to adjust the microphone preamplifier gain. The signal to noise ratio of the expected input signal is set by *NOISE\_GATE\_THRESHOLD*. In some situations it is preferable to remove audio considered to be consisting solely of background noise from the audio output; for example conference calls. This can be done by setting *NOISE\_GATE\_ON*. This does not affect the performance of the AGC algorithm.

The AGC algorithm should not be used where very large background noise is present. If the type of input data, application and microphone is known then the AGC will typically not be required for good performance, it is intended for use with inputs with a large dynamic range or unknown nominal level. When setting *NOISE\_GATE\_THRESHOLD* be aware that in some mobile phone scenarios the ADC SNR will be dictated by the microphone performance rather than the ADC or the signal. Gain changes to the microphone are performed on zero crossings. To eliminate DC offsets, wind noise, and pop sounds from the output of the ADC, the ADC's HPF should always be enabled.

## 12.0 Status & Control Registers (Continued)

### 12.16 MIC\_1 CONFIGURATION REGISTER

This register is used to control the microphone configuration.

**TABLE 16. MIC\_1 (0x0Bh)**

| Bits | Field       | Description                                                                                                                                                                                               |
|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0  | PREAMP_GAIN | Programs the gain applied to the microphone preamplifier if the AGC is not in use.                                                                                                                        |
|      |             | PREAMP_GAIN                                                                                                                                                                                               |
|      |             | 0000 <sub>2</sub>                                                                                                                                                                                         |
|      |             | 0001 <sub>2</sub>                                                                                                                                                                                         |
|      |             | 0010 <sub>2</sub>                                                                                                                                                                                         |
|      |             | 0011 <sub>2</sub>                                                                                                                                                                                         |
|      |             | 0100 <sub>2</sub> to 1100 <sub>2</sub>                                                                                                                                                                    |
|      |             | 1101 <sub>2</sub>                                                                                                                                                                                         |
|      |             | 1110 <sub>2</sub>                                                                                                                                                                                         |
|      |             | 1111 <sub>2</sub>                                                                                                                                                                                         |
| 4    | MIC_MUTE    | If set the microphone preamplifier is muted.                                                                                                                                                              |
| 5    | INT_SE_DIFF | If set the internal microphone is assumed to be single ended and the negative connection is connected to the ADC common mode point internally. This allows a single-ended internal microphone to be used. |
| 6    | INT_EXT     | If set the single ended external microphone is used and the negative microphone input is grounded internally, otherwise internal microphone operation is assumed. (Note 19)                               |

**Note 19:** On changing INT\_EXT from internal to external note that the dc blocking cap will not be charged so some time should be taken (300 ms for a 1  $\mu$ F cap) between the detection of an external headset and the switching of the output stages and ADC to that input to allow the DC points on either side of this cap to stabilize. This can be accomplished by deselecting the microphone input from the audio outputs and ADC until the DC points stabilize.

An active MIC path to CPOUT or the ADC may result in the microphone DC blocking caps causing audio pops under the following situations:

- 1) Switching between internal and external microphone operation while in chip modes '10' or '11'.
- 2) Toggling in and out of powerdown/standby modes.
- 3) Toggling between chip modes '10' and '11' whenever external microphone operation is selected.
- 4) The insertion/removal of a headset while in chip modes '10' or '11' whenever external microphone operation is selected.

To avoid these potential pop issues, it is recommended to deselect the microphone input from CPOUT and ADC until the DC points stabilize.

## 12.0 Status & Control Registers (Continued)

### 12.17 MIC\_2 CONFIGURATION REGISTER

This register is used to control the microphone configuration.

**TABLE 17. MIC\_2 (0x0Ch)**

| Bits | Field                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | OCL_<br>VCM_<br>VOLTAGE      | Selects the voltage used as virtual ground (HP_VMID pin) in OCL mode. This will depend on the available supply and the power output requirements of the headphone amplifiers.                                                                                                                                                                                                                                                                                   |
|      |                              | OCL_VCM_VOLTAGE                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |                              | Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |                              | 0 1.2V                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |                              | 1 1.5V                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2:1  | MIC_<br>BIAS_<br>VOLTAGE     | Selects the voltage as a reference to the internal and external microphones. Only one bias pin is driven at once depending on the INT_EXT bit setting found in the MIC_1 (0x0Bh) register. MIC_BIAS_VOLTAGE should be set to '11' only if $A_{V_{DD}} > 3.4V$ . In OCL mode, MIC_BIAS_VOLTAGE = '00' (EXT_BIAS = 2.0V) should not be used to generate the EXT_BIAS supply for a cellular headset external microphone. Please refer to Table 18 for more detail. |
|      |                              | MIC_BIAS_VOLTAGE                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|      |                              | EXT_BIAS                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|      |                              | INT_BIAS                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|      |                              | 00 <sub>2</sub> 2.0V 2.0V                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|      |                              | 01 <sub>2</sub> 2.5V 2.5V                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|      |                              | 10 <sub>2</sub> 2.8V 2.8V                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|      |                              | 11 <sub>2</sub> 3.3V 3.3V                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 3    | BUTTON_TYPE                  | If set the LM4935 assumes that the button (if used) in the headset is in series (series push button) with the microphone, opening the circuit when pressed. The default is for the button to be in parallel (parallel push button), shorting out the microphone when pressed.                                                                                                                                                                                   |
| 5:4  | BUTTON_<br>DEBOUNCE_<br>TIME | Sets the time used for debouncing the pushing of the button on a headset with a parallel push button.                                                                                                                                                                                                                                                                                                                                                           |
|      |                              | BUTTON_DEBOUNCE_TIME                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      |                              | Time (ms)                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|      |                              | 00 <sub>2</sub> 0                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|      |                              | 01 <sub>2</sub> 8                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|      |                              | 10 <sub>2</sub> 16                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|      |                              | 11 <sub>2</sub> 32                                                                                                                                                                                                                                                                                                                                                                                                                                              |

In OCL mode there is a trade-off between the external microphone supply voltage (EXT\_MIC\_BIAS - OCL\_VCM\_VOLTAGE) and the maximum output power possible from the headphones. A lower OCL\_VCM\_VOLTAGE gives a higher microphone supply voltage but a lower maximum output power from the headphone amplifiers due to the lower OCL\_VCM\_VOLTAGE -  $A_{V_{SS}}$ .

**TABLE 18. External MIC Supply Voltages in OCL Mode**

| Available<br>$A_{V_{DD}}$ | Recommended<br>EXT_MIC_BIAS | Supply to Microphone |                     |
|---------------------------|-----------------------------|----------------------|---------------------|
|                           |                             | OCL_VCM_VOLT = 1.5V  | OCL_VCM_VOLT = 1.2V |
| > 3.4V                    | 3.3V                        | 1.8V                 | 2.1V                |
| 2.9V to 3.4V              | 2.8V                        | 1.3V                 | 1.6V                |
| 2.8V to 2.9V              | 2.5V                        | 1.0V                 | 1.3V                |
| 2.7V to 2.8V              | 2.5V                        | -                    | 1.3V                |



## 12.0 Status & Control Registers (Continued)

### 12.18 SIDETONE ATTENUATION REGISTER

This register is used to control the analog sidetone attenuation. (Note 20)

**TABLE 19. SIDETONE (0x0Dh)**

| Bits | Field              | Description                                                                                    |
|------|--------------------|------------------------------------------------------------------------------------------------|
| 3:0  | SIDETONE_<br>ATTEN | Programs the attenuation applied to the microphone preamp output to produce a sidetone signal. |
|      |                    | SIDETONE_ATTEN                                                                                 |
|      |                    | Attenuation                                                                                    |
|      |                    | 0000 <sub>2</sub>                                                                              |
|      |                    | -Inf                                                                                           |
|      |                    | 0001 <sub>2</sub>                                                                              |
|      |                    | -30 dB                                                                                         |
|      |                    | 0010 <sub>2</sub>                                                                              |
|      |                    | -27 dB                                                                                         |
|      |                    | 0011 <sub>2</sub>                                                                              |
|      |                    | -24 dB                                                                                         |
|      |                    | 0100 <sub>2</sub>                                                                              |
|      |                    | -21 dB                                                                                         |
|      |                    | 0101 <sub>2</sub> to 1010 <sub>2</sub>                                                         |
|      |                    | -18 dB to -3 dB                                                                                |
|      |                    | 1011 <sub>2</sub> to 1111 <sub>2</sub>                                                         |
|      |                    | 0 dB                                                                                           |

**Note 20:** An active SIDETONE path to an audio output may result in the microphone DC blocking caps causing audio pops under the following situations:

- 1) Switching between internal and external microphone operation while in chip modes '10' or '11'.
  - 2) Toggling in and out of powerdown/standby modes.
  - 3) Toggling between chip modes '10' and '11' whenever external microphone operation is selected.
  - 4) The insertion/removal of a headset while in chip modes '10' or '11' whenever external microphone operation is selected.
- To avoid potential pop noises, it is recommended to set SIDETONE\_ATTEN to '0000' until DC points have stabilized whenever the SIDETONE path is used.

## 12.0 Status & Control Registers (Continued)

## 12.19 CP\_INPUT CONFIGURATION REGISTER

This register is used to control the differential cell phone input.

**TABLE 20. CP\_INPUT (0x0Eh)**

| Bits | Field     | Description                                                    |                     |
|------|-----------|----------------------------------------------------------------|---------------------|
| 4:0  | CPI_LEVEL | Programs the gain/attenuation applied to the cell phone input. |                     |
|      |           | CPI_LEVEL                                                      | Level               |
|      |           | 00000 <sub>2</sub>                                             | −34.5 dB            |
|      |           | 00001 <sub>2</sub>                                             | −33 dB              |
|      |           | 00010 <sub>2</sub>                                             | −31.5 dB            |
|      |           | 00011 <sub>2</sub>                                             | −30 dB              |
|      |           | 00100 to 11100 <sub>2</sub>                                    | −28.5 dB to +7.5 dB |
|      |           | 11101 <sub>2</sub>                                             | +9 dB               |
|      |           | 11110 <sub>2</sub>                                             | +10.5 dB            |
|      |           | 11111 <sub>2</sub>                                             | +12 dB              |
| 5    | CPI_MUTE  | If set the CPI input is muted at source.                       |                     |

## 12.0 Status & Control Registers (Continued)

### 12.20 AUX\_LEFT CONFIGURATION REGISTER

This register is used to control the left aux analog input.

**TABLE 21. AUX\_LEFT (0x0Fh)**

| Bits | Field          | Description                                                                                                         |
|------|----------------|---------------------------------------------------------------------------------------------------------------------|
| 4:0  | AUX_LEFT_LEVEL | Programs the gain/attenuation applied to the AUX LEFT analog input to the mixer. (Note 21)                          |
|      |                | AUX_LEFT_LEVEL                                                                                                      |
|      |                | Level (With Boost)                                                                                                  |
|      |                | Level (Without Boost)                                                                                               |
|      |                | 00000 <sub>2</sub>                                                                                                  |
|      |                | –34.5 dB                                                                                                            |
|      |                | –46.5 dB                                                                                                            |
|      |                | 00001 <sub>2</sub>                                                                                                  |
|      |                | –33 dB                                                                                                              |
|      |                | –45 dB                                                                                                              |
|      |                | 00010 <sub>2</sub>                                                                                                  |
|      |                | –31.5 dB                                                                                                            |
|      |                | –43.5 dB                                                                                                            |
|      |                | 00011 <sub>2</sub>                                                                                                  |
|      |                | –30 dB                                                                                                              |
|      |                | –42 dB                                                                                                              |
|      |                | 00100 to 11100 <sub>2</sub>                                                                                         |
|      |                | –28.5 dB to +7.5 dB                                                                                                 |
|      |                | –40.5 dB to –4.5 dB                                                                                                 |
|      |                | 11101 <sub>2</sub>                                                                                                  |
|      |                | +9 dB                                                                                                               |
|      |                | –3 dB                                                                                                               |
|      |                | 11110 <sub>2</sub>                                                                                                  |
|      |                | +10.5 dB                                                                                                            |
|      |                | –1.5 dB                                                                                                             |
|      |                | 11111 <sub>2</sub>                                                                                                  |
|      |                | +12 dB                                                                                                              |
|      |                | 0 dB                                                                                                                |
| 5    | AUX_LEFT_BOOST | If set the gain of the AUX_LEFT input to the mixer is increased by 12 dB (see above).                               |
| 6    | AUX_L_MUTE     | If set the AUX LEFT input is muted.                                                                                 |
| 7    | AUX_OR_DAC_L   | If set the AUX LEFT input is passed to the mixer, the default is for the DAC LEFT output to be passed to the mixer. |

**Note 21:** The recommended mixer level is 1V RMS. The auxiliary analog inputs can be boosted by 12 dB if enough headroom is available. Clipping may occur if the analog power supply is insufficient to cater for the required gain.

## 12.0 Status & Control Registers (Continued)

### 12.21 AUX\_RIGHT CONFIGURATION REGISTER

This register is used to control the right aux analog input.

**TABLE 22. AUX\_RIGHT (0x10h)**

| Bits | Field           | Description                                                                                                           |
|------|-----------------|-----------------------------------------------------------------------------------------------------------------------|
| 4:0  | AUX_RIGHT_LEVEL | Programs the gain/attenuation applied to the AUX RIGHT analog input to the mixer. (Note 22)                           |
|      |                 | AUX_RIGHT_LEVEL      Level (With Boost)      Level (Without Boost)                                                    |
|      |                 | 00000 <sub>2</sub> -34.5 dB      -46.5 dB                                                                             |
|      |                 | 00001 <sub>2</sub> -33 dB      -45 dB                                                                                 |
|      |                 | 00010 <sub>2</sub> -31.5 dB      -43.5 dB                                                                             |
|      |                 | 00011 <sub>2</sub> -30 dB      -42 dB                                                                                 |
|      |                 | 00100 to 11100 <sub>2</sub> -28.5 dB to +7.5 dB      -40.5 dB to -4.5 dB                                              |
|      |                 | 11101 <sub>2</sub> +9 dB      -3 dB                                                                                   |
|      |                 | 11110 <sub>2</sub> +10.5 dB      -1.5 dB                                                                              |
|      |                 | 11111 <sub>2</sub> +12 dB      0 dB                                                                                   |
| 5    | AUX_RIGHT_BOOST | If set the gain of the AUX_RIGHT input to the mixer is increased by 12 dB (see above).                                |
| 6    | AUX_R_MUTE      | If set the AUX RIGHT input is muted.                                                                                  |
| 7    | AUX_OR_DAC_R    | If set the AUX RIGHT input is passed to the mixer, the default is for the DAC RIGHT output to be passed to the mixer. |

**Note 22:** The recommended mixer level is 1V RMS. The auxiliary analog inputs can be boosted by 12 dB if enough headroom is available. Clipping may occur if the analog power supply is insufficient to cater for the required gain.

## 12.0 Status & Control Registers (Continued)

### 12.22 DAC CONFIGURATION REGISTER

This register is used to control the DAC levels to the mixer.

**TABLE 23. DAC (0x11h)**

| Bits | Field          | Description                                                                                                                       |
|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 4:0  | DAC_LEVEL      | Programs the gain/attenuation applied to the DAC input to the mixer. (Note 23)                                                    |
|      |                | DAC_LEVEL      Level (With Boost)      Level (Without Boost)                                                                      |
|      |                | 00000 <sub>2</sub> –34.5 dB      –46.5 dB                                                                                         |
|      |                | 00001 <sub>2</sub> –33 dB      –45 dB                                                                                             |
|      |                | 00010 <sub>2</sub> –31.5 dB      –43.5 dB                                                                                         |
|      |                | 00011 <sub>2</sub> –30 dB      –42 dB                                                                                             |
|      |                | 00100 to 11100 <sub>2</sub> –28.5 dB to +7.5 dB      –40.5 dB to –4.5 dB                                                          |
|      |                | 11101 <sub>2</sub> +9 dB      –3 dB                                                                                               |
|      |                | 11110 <sub>2</sub> +10.5 dB      –1.5 dB                                                                                          |
|      |                | 11111 <sub>2</sub> +12 dB      0 dB                                                                                               |
| 5    | USE_AUX_LEVELS | If set the gain of the DAC inputs is controlled by the AUX_LEFT and AUX_RIGHT registers, allowing a stereo balance to be applied. |
| 6    | BOOST          | If set the gain of the DAC inputs to the mixer is increased by 12 dB (see above).                                                 |
| 7    | DAC_MUTE       | If set the stereo DAC input is muted on the next zero crossing.                                                                   |

**Note 23:** The output from the DAC is 1V RMS for a full scale digital input. This can be boosted by 12 dB if enough headroom is available. Clipping may occur if the analog power supply is insufficient to cater for the required gain.

## 12.0 Status & Control Registers (Continued)

### 12.23 CP\_OUTPUT CONFIGURATION REGISTER

This register is used to control the differential cell phone output. (Note 24)

**TABLE 24. CP\_OUTPUT (0x12h)**

| Bits | Field          | Description                                                                                                                                                                                                   |
|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | MIC_SELECT     | If set the microphone channel of the mixer is added to the cellphone output signal.                                                                                                                           |
| 1    | RIGHT_SELECT   | If set the right channel of the mixer is added to the cellphone output signal.                                                                                                                                |
| 2    | LEFT_SELECT    | If set the left channel of the mixer is added to the cellphone output signal.                                                                                                                                 |
| 3    | CPO_MUTE       | If set the CPOUT output is muted.                                                                                                                                                                             |
| 4    | MIC_NOISE_GATE | If this is set and NOISE_GATE_ON (register 0x08h) is enabled, the MIC to CPO path will be gated if the signal is determined to be noise by the AGC (that is, if the signal is below the set noise threshold). |

**Note 24:** The gain of cell phone output amplifier is 0 dB.

## 12.0 Status & Control Registers (Continued)

### 12.24 AUX\_OUTPUT CONFIGURATION REGISTER

This register is used to control the differential auxiliary output. (Note 25)

**TABLE 25. AUX\_OUTPUT (0x13h)**

| Bits | Field        | Description                                                                         |
|------|--------------|-------------------------------------------------------------------------------------|
| 0    | CPI_SELECT   | If set the cell phone input channel of the mixer is added to the aux output signal. |
| 1    | RIGHT_SELECT | If set the right channel of the mixer is added to the aux output signal.            |
| 2    | LEFT_SELECT  | If set the left channel of the mixer is added to the aux output signal.             |
| 3    | AUX_MUTE     | If set the aux output is muted.                                                     |

**Note 25:** The gain of the auxiliary output amplifier is 0 dB. If a second (external) loudspeaker amplifier is to be used its gain should be set to 12 dB to match the onboard loudspeaker amplifier gain.

## 12.0 Status & Control Registers (Continued)

### 12.25 LS\_OUTPUT CONFIGURATION REGISTER

This register is used to control the loudspeaker output. (Note 26)

**TABLE 26. LS\_OUTPUT (0x14h)**

| Bits | Field        | Description                                                                                 |
|------|--------------|---------------------------------------------------------------------------------------------|
| 0    | CPI_SELECT   | If set the cell phone input channel of the mixer is added to the loudspeaker output signal. |
| 1    | RIGHT_SELECT | If set the right channel of the mixer is added to the loudspeaker output signal.            |
| 2    | LEFT_SELECT  | If set the left channel of the mixer is added to the loudspeaker output signal.             |
| 3    | LS_MUTE      | If set the loudspeaker output is muted.                                                     |

**Note 26:** The gain of the loudspeaker output amplifier is 12 dB.



## 12.0 Status & Control Registers (Continued)

### 12.26 HP\_OUTPUT CONFIGURATION REGISTER

This register is used to control the stereo headphone output. (Note 27)

**TABLE 27. HP\_OUTPUT (0x15h)**

| Bits | Field           | Description                                                                                                                                                                                                                                                                            |
|------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | SIDETONE_SELECT | If set the sidetone channel of the mixer is added to both of the headphone output signals.                                                                                                                                                                                             |
| 1    | CPI_SELECT      | If set the cell phone input channel of the mixer is added to both of the headphone output signals.                                                                                                                                                                                     |
| 2    | RIGHT_SELECT    | If set the right channel of the mixer is added to the headphone output. If the STEREO bit (0x00h) is set, the right channel is added to the right headphone output signal only. If the STEREO bit (0x00h) is cleared, it is added to both the right and left headphone output signals. |
| 3    | LEFT_SELECT     | If set the left channel of the mixer is added to the headphone output. If the STEREO bit (0x00h) is set, the left channel is added to the left headphone output signal only. If the STEREO bit (0x00h) is cleared, it is added to both the right and left headphone output signals.    |
| 4    | HP_MUTE         | If set the headphone output is muted.                                                                                                                                                                                                                                                  |

**Note 27:** The gain of the headphone output amplifier is –6 dB for the cell phone input channel and sidetone channel of the mixer. When the STEREO bit (0x00h) is set, headphone output amplifier gain is –6 dB for the left and right channel. When the STEREO bit (0x00h) is cleared, the headphone output amplifier gain is –12 dB for the left and right channel (to allow enough headroom for adding them and routing them to both headphone amplifiers).

## 12.0 Status & Control Registers (Continued)

### 12.27 EP\_OUTPUT CONFIGURATION REGISTER

This register is used to control the mono earpiece output. (Note 28)

**TABLE 28. EP\_OUTPUT (0x16h)**

| Bits | Field           | Description                                                                              |
|------|-----------------|------------------------------------------------------------------------------------------|
| 0    | SIDETONE_SELECT | If set the sidetone channel of the mixer is added to the earpiece output signal.         |
| 1    | CPI_SELECT      | If set the cell phone input channel of the mixer is added to the earpiece output signal. |
| 2    | RIGHT_SELECT    | If set the right channel of the mixer is added to the earpiece output signal.            |
| 3    | LEFT_SELECT     | If set the left channel of the mixer is added to the earpiece output signal.             |
| 4    | EP_MUTE         | If set the earpiece output is muted.                                                     |

**Note 28:** The gain of the earpiece output amplifier is 6 dB.

## 12.0 Status & Control Registers (Continued)

### 12.28 DETECT CONFIGURATION REGISTER

This register is used to control the headset detection system.

**TABLE 29. DETECT (0x17h)**

| Bits | Field        | Description                                                                                                                                                                                                                                                                                                                                 |
|------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | DET_INT      | If set an IRQ is raised when a change is detected in the headset status. Clearing this bit will clear an IRQ that has been triggered by the headset detect.                                                                                                                                                                                 |
| 1    | BTN_INT      | If set an IRQ is raised when the headset button is pressed. Clearing this bit will clear an IRQ that has been triggered by a button event.                                                                                                                                                                                                  |
| 2    | TEMP_INT     | If set an IRQ is raised during a temperature event. If cleared, the LM4935 will still automatically cycle the power amplifiers off if the internal temperature is too high. This bit should not be set whenever the loudspeaker amplifier is turned on. Clearing this bit will clear an IRQ that has been triggered by a temperature event. |
| 6:3  | HS_DBNC_TIME | Sets the time used for debouncing the analog signals from the detection inputs used to sense the insertion/removal of a headset.                                                                                                                                                                                                            |
|      |              | HS_DBNC_TIME                      Time (ms)                                                                                                                                                                                                                                                                                                 |
|      |              | 0000 <sub>2</sub> 0                                                                                                                                                                                                                                                                                                                         |
|      |              | 0001 <sub>2</sub> 8                                                                                                                                                                                                                                                                                                                         |
|      |              | 0010 <sub>2</sub> 16                                                                                                                                                                                                                                                                                                                        |
|      |              | 0011 <sub>2</sub> 32                                                                                                                                                                                                                                                                                                                        |
|      |              | 0100 <sub>2</sub> 48                                                                                                                                                                                                                                                                                                                        |
|      |              | 0101 <sub>2</sub> 64                                                                                                                                                                                                                                                                                                                        |
|      |              | 0110 <sub>2</sub> 96                                                                                                                                                                                                                                                                                                                        |
|      |              | 0111 <sub>2</sub> 128                                                                                                                                                                                                                                                                                                                       |
|      |              | 1000 <sub>2</sub> 192                                                                                                                                                                                                                                                                                                                       |
|      |              | 1001 <sub>2</sub> 256                                                                                                                                                                                                                                                                                                                       |
|      |              | 1010 <sub>2</sub> 384                                                                                                                                                                                                                                                                                                                       |
|      |              | 1011 <sub>2</sub> 512                                                                                                                                                                                                                                                                                                                       |
|      |              | 1100 <sub>2</sub> 768                                                                                                                                                                                                                                                                                                                       |
|      |              | 1101 <sub>2</sub> 1024                                                                                                                                                                                                                                                                                                                      |
|      |              | 1110 <sub>2</sub> 1536                                                                                                                                                                                                                                                                                                                      |
|      |              | 1111 <sub>2</sub> 2048                                                                                                                                                                                                                                                                                                                      |

## 12.0 Status & Control Registers (Continued)

### 12.29 HEADSET DETECT OVERVIEW

The LM4935 has built in monitors to automatically detect headset insertion or removal. The detection scheme can differentiate between mono, stereo, mono-cellular and stereo-cellular headsets. Upon detection of headset insertion or removal, the LM4935 updates read-only bit 0 - headset absence/presence, bit 1 - mono/stereo headset and bit 2 - headset without mic / with mic, of the STATUS register (0x18h). Headset insertion/removal and headset type can also be detected in standby mode; this consumes no analog supply current when the headset is absent.

The LM4935 can be programmed to raise an interrupt (set the IRQ pin high) when headset insert/removal is sensed by setting bit 0 of DETECT (0x17h). When headset detection is enabled in active mode and a headset is not detected, the HPL\_OUT and HPR\_OUT amplifiers will be disabled (switched off for capless mode and muted for AC-coupled mode) and the EXT\_BIAS pin will be disconnected from the MIC\_BIAS amplifier, irrespective of control register settings.

The LM4935 also has the capability to detect button press, when a button is present on the headset microphone. Both parallel button-type (in parallel with the headset microphone, default value) and series button-type (in series with the headset microphone) can be detected; the button type used needs to be defined in bit 3 of MIC\_2 (0x0Ch). Button press can also be detected in stand-by mode; this consumes 10  $\mu$ A of analog supply current for a series type push button and 100  $\mu$ A for a parallel type push button. Upon button press, the LM4935 updates bit 3 of STATUS (0x18h). In active OCL mode, with internal microphone selected (INT\_EXT = 0; (reg 0x0Bh)), if a parallel pushbutton headset is inserted into the system, INT\_EXT must be set high before BTN (bit 3 of STATUS (0x18h)) can be read. The LM4935 can also be programmed to raise an interrupt on the IRQ pin when button press is sensed by setting bit 1 of DETECT.

The LM4935 provides debounce programmability for headset and button detect. Debounce programmability can be used to reject glitches generated, and hence avoid false detection, while inserting/removing a headset or pressing a button.

Headset insert/removal debounce time is defined by HS\_DBNC\_TIME; bits 6:3 of DETECT (0x17h). Parallel button press debounce time is defined by BTN\_DBNC\_TIME; bits 5:4 of MIC\_2 (0x0Ch).

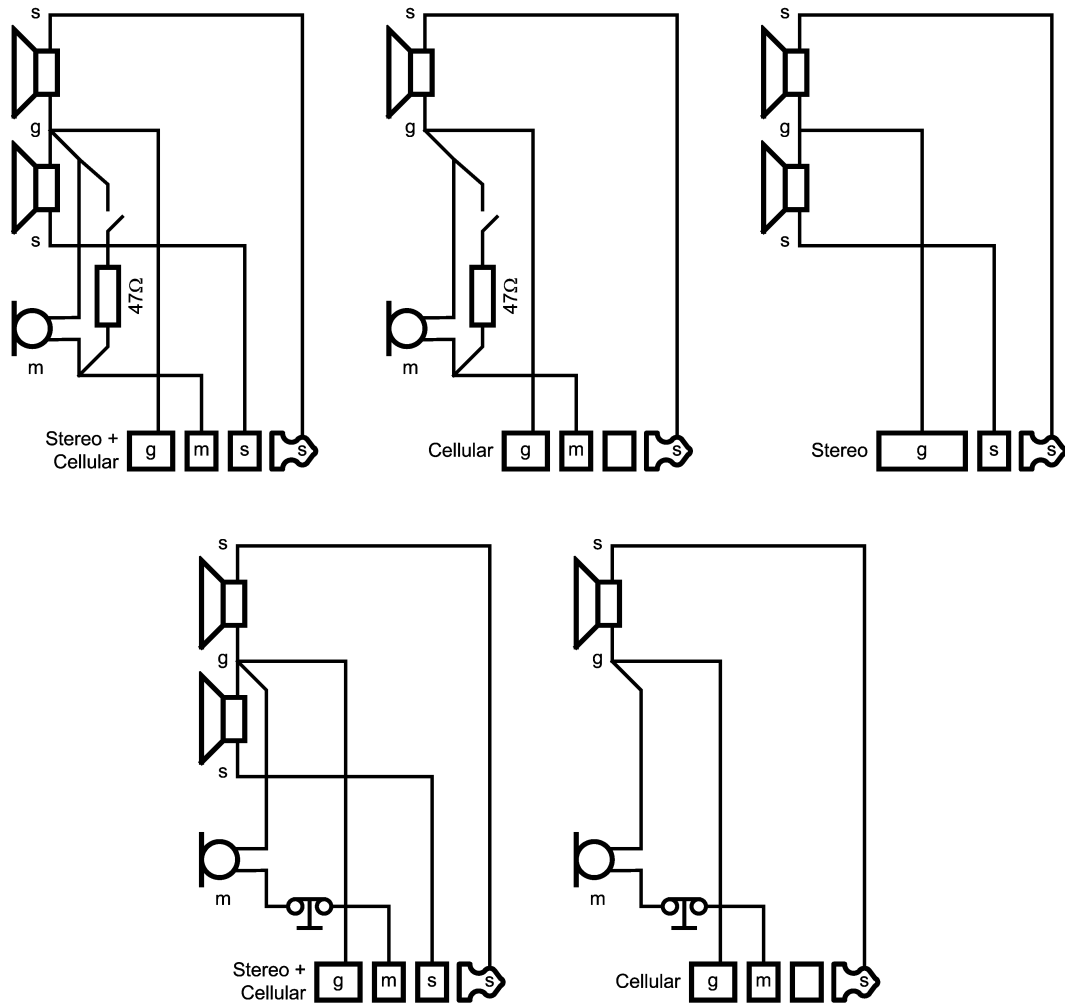
Note that since the first effect of a series button press (microphone disconnected) is indistinguishable from headset removal, the debounce time for series button press is defined by HS\_DBNC\_TIME.

Headset and push button detection can be enabled by setting CHIP\_MODE 0; bit 0 of BASIC (0x00h). For reliable headset / push button detection all following bits should be defined before enabling the headset detection system:

- 1) the OCL-bit (AC-Coupled / Capless headphone interface (bit 7 of BASIC (0x00h))
- 2) the headset insert/removal debounce settings (bit 6:3 of DETECT (0x17h))
- 3) the BTN\_TYPE-bit (Parallel / Series push button type (bit 3 of MIC\_2 (0x0Ch))
- 4) the parallel push button debounce settings (bit 5:4 of MIC\_2 (0x0Ch))

Figure 8 shows terminal connections and jack configuration for various headsets. Care should be taken to avoid any DC path from the MIC\_DET pin to ground when a headset is not inserted.

## 12.0 Status & Control Registers (Continued)

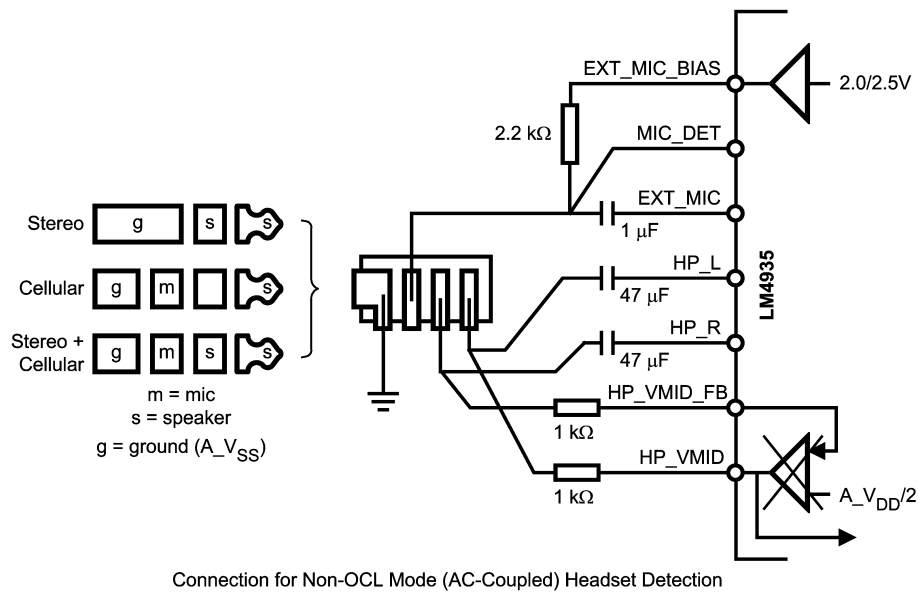
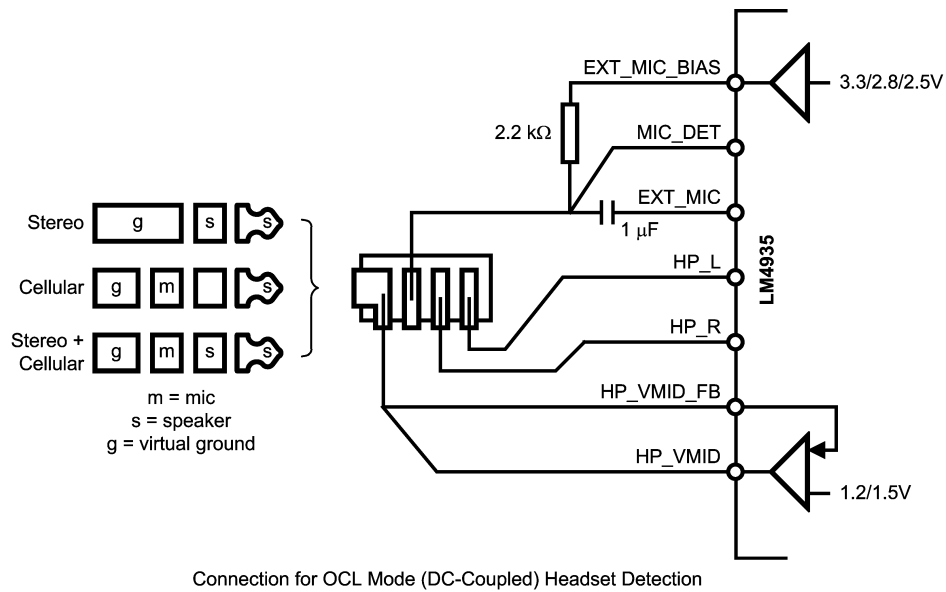


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**FIGURE 8. Headset Configurations Supported by the LM4935**

The wiring of the headset jack to the LM4935 will depend on the intended mode of the headphone amplifier:

## 12.0 Status & Control Registers (Continued)



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FIGURE 9. Connection of Headset Jack to LM4935 Depends on the Mode of the Headphone Amplifier.

## 12.0 Status & Control Registers (Continued)

### 12.30 STATUS REGISTER

This register is used to report the status of the device.

**TABLE 30. STATUS (0x18h)**

| Bits | Field          | Description                                                                                                                                                                                                                                                     |
|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | HEADSET        | This field is high when headset presence is detected (only valid if the detection system is enabled). (Note 29)                                                                                                                                                 |
| 1    | STEREO_HEADSET | This field is high when a headset with stereo speakers is detected (only valid if the detection system is enabled). (Note 29)                                                                                                                                   |
| 2    | MIC            | This field is high when a headset with a microphone is detected (only valid if the detection system is enabled). (Note 29)                                                                                                                                      |
| 3    | BTN            | This field is high when the button on the headset is pressed (only valid if the detection system is enabled). IRQ is cleared when the button has been released <b>and</b> this register has been written to.                                                    |
| 4    | SAR TRIG 1     | If this field is high then an event has happened on SAR trigger 1 (write to this register to clear IRQ).                                                                                                                                                        |
| 5    | SAR TRIG 2     | If this field is high then an event has happened on SAR trigger 2 (write to this register to clear IRQ).                                                                                                                                                        |
| 6    | TEMP           | If this field is high then a temperature event has occurred (write to this register to clear IRQ). This field will stay high even when the IRQ is cleared so long as the event occurs. This bit is only valid whenever the loudspeaker amplifier is turned off. |
| 7    | GPIN           | When GPIO_SEL is set to a readable configuration a digital input on GPIO1 can be read back here.                                                                                                                                                                |

**Note 29:** The detection IRQ is cleared when this register has been written to.

## 12.0 Status & Control Registers (Continued)

### 12.31 AUDIO INTERFACE CONFIGURATION REGISTER

This register is used to control the configuration of the audio data interfaces.

**TABLE 31. AUDIO\_IF (0x19h)**

| Bits | Field         | Description                                                                                                                                                                                                                                   |                          |                         |                          |                          |            |            |
|------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------------------------|--------------------------|--------------------------|------------|------------|
| 1:0  | AUDIO_IF_MODE | Selects the function of the 6 audio interface IOs.                                                                                                                                                                                            |                          |                         |                          |                          |            |            |
|      |               | AUDIO_IF_MODE                                                                                                                                                                                                                                 | I <sup>2</sup> S_CLK pin | I <sup>2</sup> S_WS pin | I <sup>2</sup> S_SDI pin | I <sup>2</sup> S_SDO pin | GPIO_1 pin | GPIO_2 pin |
|      |               | 00 <sub>2</sub>                                                                                                                                                                                                                               | I <sup>2</sup> S_CLK     | I <sup>2</sup> S_WS     | I <sup>2</sup> S_SDI     | I <sup>2</sup> S_SDO     | GPIO_1     | GPIO_2     |
|      |               | 01 <sub>2</sub>                                                                                                                                                                                                                               | PCM_CLK                  | PCM_SYNC                | -                        | PCM_SDO                  | GPIO_1     | GPIO_2     |
|      |               | 10 <sub>2</sub>                                                                                                                                                                                                                               | PCM_CLK                  | PCM_SYNC                | PCM_SDI                  | PCM_SDO                  | GPIO_1     | GPIO_2     |
|      |               | 11 <sub>2</sub>                                                                                                                                                                                                                               | I <sup>2</sup> S_CLK     | I <sup>2</sup> S_WS     | I <sup>2</sup> S_SDI     | PCM_SDO                  | PCM_CLK    | PCM_SYNC   |
| 2    | I2S_WS_MS     | If set the I <sup>2</sup> S_WS is produced by the LM4935 and the I <sup>2</sup> S_WS pin will be an output.                                                                                                                                   |                          |                         |                          |                          |            |            |
| 3    | I2S_CLK_MS    | If set the I <sup>2</sup> S_CLK is produced by the LM4935 and the I <sup>2</sup> S_CLK pin will be an output.                                                                                                                                 |                          |                         |                          |                          |            |            |
| 4    | PCM_SYNC_MS   | If set the PCM_SYNC is produced by the LM4935 and the relevant pin will be an output.                                                                                                                                                         |                          |                         |                          |                          |            |            |
| 5    | PCM_CLK_MS    | If set the PCM_CLK is produced by the LM4935 and the relevant pin will be an output.                                                                                                                                                          |                          |                         |                          |                          |            |            |
| 7:6  | I2S_SDO_DATA  | The two ADCs on the LM4935 can both be read via the isochronous I2S interface. The most recent valid sample is output from the following source: (Please refer to the GPIO configuration register (0x1Ah) for more information on SAR_CH_SEL) |                          |                         |                          |                          |            |            |
|      |               | I2S_SDO_DATA                                                                                                                                                                                                                                  |                          |                         | LEFT                     |                          | RIGHT      |            |
|      |               | 00 <sub>2</sub>                                                                                                                                                                                                                               |                          |                         | AUDIO ADC                |                          | SAR_CH_SEL |            |
|      |               | 01 <sub>2</sub>                                                                                                                                                                                                                               |                          |                         | SAR VSAR 1               |                          | SAR_CH_SEL |            |
|      |               | 10 <sub>2</sub>                                                                                                                                                                                                                               |                          |                         | SAR VSAR 2               |                          | SAR_CH_SEL |            |
|      |               | 11 <sub>2</sub>                                                                                                                                                                                                                               |                          |                         | A_V <sub>DD</sub> /2     |                          | SAR_CH_SEL |            |

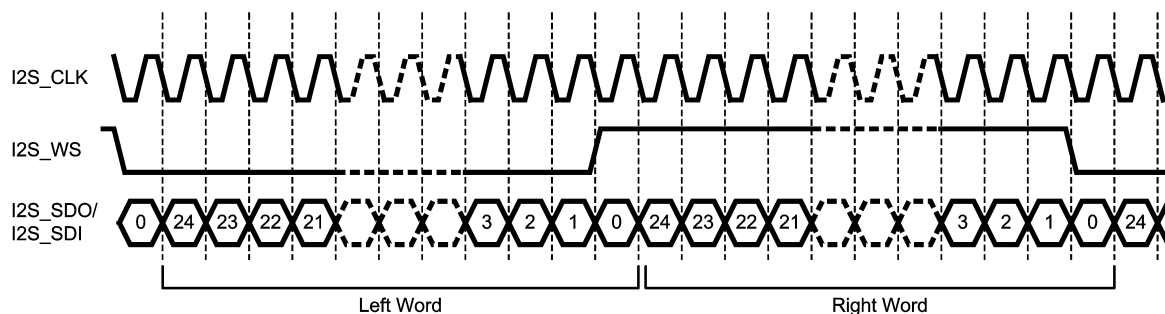


## 12.0 Status & Control Registers (Continued)

### 12.32 DIGITAL AUDIO DATA FORMATS

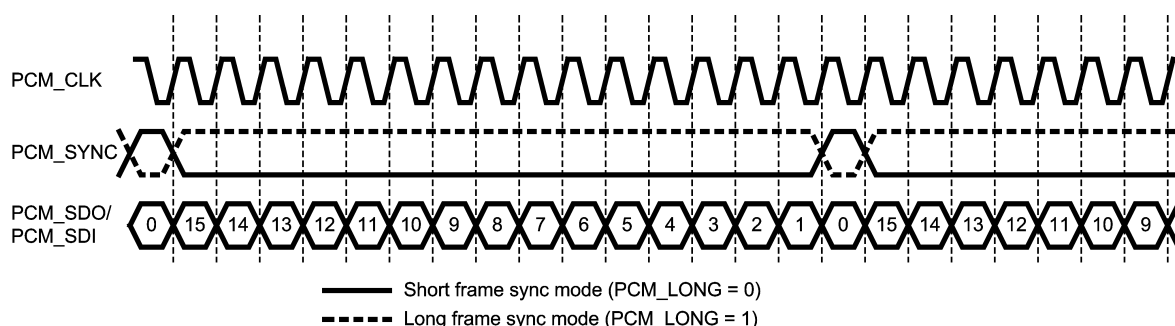
I2S master mode can only be used when the DAC is enabled unless the ADC\_I2S\_M bit is set. PCM Master mode can only be used when the ADC is enabled. If the PCM receiver interface is operated in slave mode the clock and sync should be enabled at the same time as the PCM receiver uses the first PCM frame to calculate the PCM interface format. This format can not be changed unless a soft reset is issued. It is strongly recommended that the LM4935 is operated in master mode as this eliminates the risk of sample rate mismatch between the data converters and the audio interfaces.

In master mode the I2S\_CLK has a 60/40 duty cycle and a frequency of  $50 \times f_s$ . In slave mode the PCM and I2S receivers only record the 1st 16 and 18 bits of the serial words respectively. The I2S format is as follows:



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FIGURE 10. I²S Serial Data Format (Default Mode)



20134116

FIGURE 11. PCM Serial Data Format (16 bit Slave Example)

When SAR SDO data is passed to the I2S, it is left aligned (MSB aligned) to allow lower I2S resolutions to be used. If the DAC is driven from the PCM interface then the left channel of the DAC is used and the right channel is inactive.

## 12.0 Status & Control Registers (Continued)

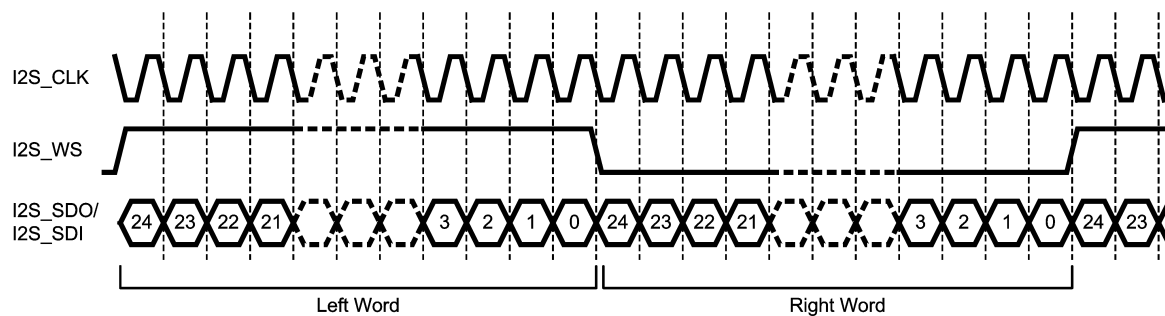
### 12.33 GPIO CONFIGURATION REGISTER

This register is used to control the GPIO system.

**TABLE 32. GPIO (0x1Ah)**

| Bits | Field      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0  | GPIO_SEL   | This sets the function of the GPIOs when the Audio Interface is not using them.                                                                                                                                                                                                                                                                                                                                                                |
|      |            | GPIO_SEL      GPIO 1      GPIO 2                                                                                                                                                                                                                                                                                                                                                                                                               |
|      |            | 000 <sub>2</sub> 0      0                                                                                                                                                                                                                                                                                                                                                                                                                      |
|      |            | 001 <sub>2</sub> READABLE      SPI_SDO                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |            | 010 <sub>2</sub> LS_AMP_ENABLE      SPI_SDO                                                                                                                                                                                                                                                                                                                                                                                                    |
|      |            | 011 <sub>2</sub> GPIO_DATA      SPI_SDO                                                                                                                                                                                                                                                                                                                                                                                                        |
|      |            | 100 <sub>2</sub> 0      SPI_SDO                                                                                                                                                                                                                                                                                                                                                                                                                |
|      |            | 101 <sub>2</sub> READABLE      SAR_SDO                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |            | 110 <sub>2</sub> LS_AMP_ENABLE      SAR_SDO                                                                                                                                                                                                                                                                                                                                                                                                    |
|      |            | 111 <sub>2</sub> GPIO_DATA      SAR_SDO                                                                                                                                                                                                                                                                                                                                                                                                        |
|      |            | Setting GPIO_SEL = "010" with the GPIO_TEST_MODE bit (register 0X26h) set configures the GPIOs for digital mic operation. With this setting, GPIO1 will output VADC_CLK_OUT to provide a clock for the digital mic. GPIO2 will accept digital mic data. GPIO1's LS_AMP_ENABLE setting will be logic high whenever the loudspeaker amplifier is enabled. This is useful for enabling an external amplifier for stereo loudspeaker applications. |
| 4:3  | SAR_CH_SEL | This field selects the SAR output channel for the 2nd (Right) I <sup>2</sup> S channel or for SAR_SDO via GPIO2.                                                                                                                                                                                                                                                                                                                               |
|      |            | SAR_CH_SEL      Selected Channel                                                                                                                                                                                                                                                                                                                                                                                                               |
|      |            | 00 <sub>2</sub> VSAR_1                                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |            | 01 <sub>2</sub> VSAR_2                                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |            | 10 <sub>2</sub> D_V <sub>DD</sub> /2 or BB_V <sub>DD</sub>                                                                                                                                                                                                                                                                                                                                                                                     |
|      |            | 11 <sub>2</sub> A_V <sub>DD</sub> /2                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5    | I2S_MODE   | If set the I2S operates in left justified mode (sometimes referred to as DSP mode). See example below. (Note 30)                                                                                                                                                                                                                                                                                                                               |
| 6    | PCM_LONG   | If set the PCM interface uses LONG frame sync which is essentially an inverted short frame sync.                                                                                                                                                                                                                                                                                                                                               |
| 7    | GPIO_DATA  | If GPIO_SEL is set to GPIO_DATA then the content of this field is passed to GPIO1 as an output.                                                                                                                                                                                                                                                                                                                                                |

**Note 30:** The left justified I<sup>2</sup>S mode is similar to normal I<sup>2</sup>S other than there is no delay between a change in WS to the MSB:



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**FIGURE 12. I<sup>2</sup>S Serial Data Format (Left Justified Mode)**

## 12.0 Status & Control Registers (Continued)

### 12.34 SAR CHANNELS 0 & 1 CONFIGURATION REGISTER

This register is used to control channel 0 and 1 of the SAR system. (Note 31)

**TABLE 33. SAR\_SLOT01 (0x1Bh)**

| Bits | Field      | Description                                                                     |
|------|------------|---------------------------------------------------------------------------------|
| 2:0  | SLOT_0_FS  | Programs the sampling frequency of SAR channel 0:                               |
|      |            | SLOT_0_FS      Sample Rate @ 12.000 MHz (point A)                               |
|      |            | 000 <sub>2</sub> 13.888 kHz                                                     |
|      |            | 001 <sub>2</sub> 3.472 kHz                                                      |
|      |            | 010 <sub>2</sub> 0.868 kHz                                                      |
|      |            | 011 <sub>2</sub> 217 Hz                                                         |
|      |            | 100 <sub>2</sub> 54 Hz                                                          |
|      |            | 101 <sub>2</sub> 14 Hz                                                          |
|      |            | 110 <sub>2</sub> 4 Hz                                                           |
|      |            | 111 <sub>2</sub> 1 Hz                                                           |
| 3    | SLOT_0_ENB | If set then VSAR 1 is sampled into SAR slot 0 which also activates the SAR ADC. |
| 6:4  | SLOT_1_FS  | Programs the sampling frequency of SAR channel 1:                               |
|      |            | SLOT_1_FS      Sample Rate @ 12.000 MHz (point A)                               |
|      |            | 000 <sub>2</sub> 13.888 kHz                                                     |
|      |            | 001 <sub>2</sub> 3.472 kHz                                                      |
|      |            | 010 <sub>2</sub> 0.868 kHz                                                      |
|      |            | 011 <sub>2</sub> 217 Hz                                                         |
|      |            | 100 <sub>2</sub> 54 Hz                                                          |
|      |            | 101 <sub>2</sub> 14 Hz                                                          |
|      |            | 110 <sub>2</sub> 4 Hz                                                           |
|      |            | 111 <sub>2</sub> 1 Hz                                                           |
| 7    | SLOT_1_ENB | If set then VSAR 2 is sampled into SAR slot 1 which also activates the SAR ADC. |

**Note 31:** See the section **SAR Overview** for more details on this register.

## 12.0 Status & Control Registers (Continued)

### 12.35 SAR CHANNELS 2 & 3 CONFIGURATION REGISTER

This register is used to control channel 2 and 3 of the SAR system. (Note 31)

**TABLE 34. SAR\_SLOT23 (0x1Ch)**

| Bits | Field      | Description                                                                                                                                                |
|------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0  | SLOT_2_FS  | Programs the sampling frequency of SAR channels 2 and 3:                                                                                                   |
|      |            | SLOT_2_FS      Sample Rate @ 12.000 MHz (point <b>A</b> )                                                                                                  |
|      |            | 000 <sub>2</sub> 13.888 kHz                                                                                                                                |
|      |            | 001 <sub>2</sub> 3.472 kHz                                                                                                                                 |
|      |            | 010 <sub>2</sub> 0.868 kHz                                                                                                                                 |
|      |            | 011 <sub>2</sub> 217 Hz                                                                                                                                    |
|      |            | 100 <sub>2</sub> 54 Hz                                                                                                                                     |
|      |            | 101 <sub>2</sub> 14 Hz                                                                                                                                     |
|      |            | 110 <sub>2</sub> 4 Hz                                                                                                                                      |
|      |            | 111 <sub>2</sub> 1 Hz                                                                                                                                      |
| 3    | SLOT_2_ENB | If set then D_V <sub>DD</sub> / 2 or BB_V <sub>DD</sub> (depending on SLOT2_V <sub>BB</sub> ) is sampled into SAR slot 2 which also activates the SAR ADC. |
| 4    | SLOT_3_ENB | If set then A_V <sub>DD</sub> / 2 is sampled into SAR slot 3 which also activates the SAR ADC.                                                             |
| 5    | SLOT_2_VBB | If set then BB_V <sub>DD</sub> input is used as input to SAR slot 2 rather than the D_V <sub>DD</sub> .                                                    |

## 12.0 Status & Control Registers (Continued)

### 12.36 SAR DATA 0 TO 3 REGISTERS

These registers are used to read the 8 MSBs from the 4 SAR channels.

**TABLE 35. SAR\_DATA\_0 Register (0x1Dh)**

| Bits | Field       | Description                     |
|------|-------------|---------------------------------|
| 7:0  | SLOT_0_DATA | Latest slot 0 sample bits 11:4. |

**TABLE 36. SAR\_DATA\_1 Register (0x1Eh)**

| Bits | Field       | Description                     |
|------|-------------|---------------------------------|
| 7:0  | SLOT_1_DATA | Latest slot 1 sample bits 11:4. |

**TABLE 37. SAR\_DATA\_2 Register (0x1Fh)**

| Bits | Field       | Description                     |
|------|-------------|---------------------------------|
| 7:0  | SLOT_2_DATA | Latest slot 2 sample bits 11:4. |

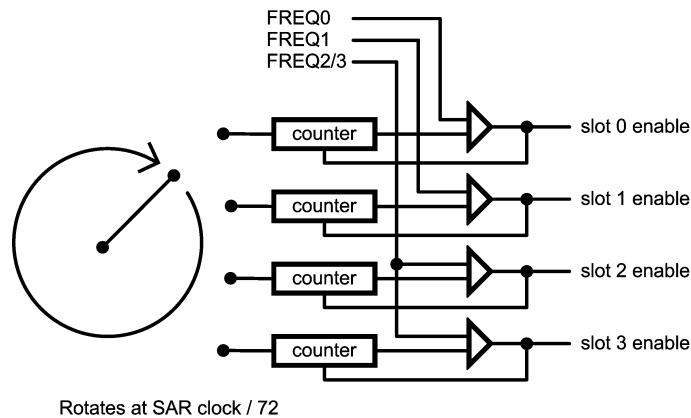
**TABLE 38. SAR\_DATA\_3 Register (0x20h)**

| Bits | Field       | Description                     |
|------|-------------|---------------------------------|
| 7:0  | SLOT_3_DATA | Latest slot 3 sample bits 11:4. |

## 12.0 Status & Control Registers (Continued)

### 12.37 SAR OVERVIEW

The SAR controller works via a scheduler that allocates time slots for each of the four channels. All four channels can operate up to the same maximum frequency. When the sampling frequency of a channel is to be reduced the time slot allocated to that channel is simply enabled less often. For example if one slot is to work at a quarter of the frequency of the others then only one in four of its allocated slot triggers the SAR to activate:



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**FIGURE 13. Internal SAR Control Signals to SAR Module**

Each time slot is used to sample a single fixed input, slot 0 is used for VSAR 1, slot 1 for VSAR 2, slot 2 for either  $D_{V_{DD}}$  or  $BB_{V_{DD}}$ \* and slot 3 for the  $A_{V_{DD}}$ . When a particular time slot is activated the correct mux, clock and enable controls to the ADC module are produced and the output sampled when ready. If the  $D_{V_{DD}}$  or the  $A_{V_{DD}}$  are being sampled then a voltage divider is used to half the input to below the full scale reference of 2.5V. As this results in a current path to ground it is only inserted while the ADC is settling to reduce power consumption.

Using this method, samples can be taken using as little power as possible while allowing sample rates as low as 1 Hz. The data can either be read directly or used to trigger interrupts when set voltages are passed. This reduces the baseband controllers software overhead and IO bandwidth, further reducing system power.

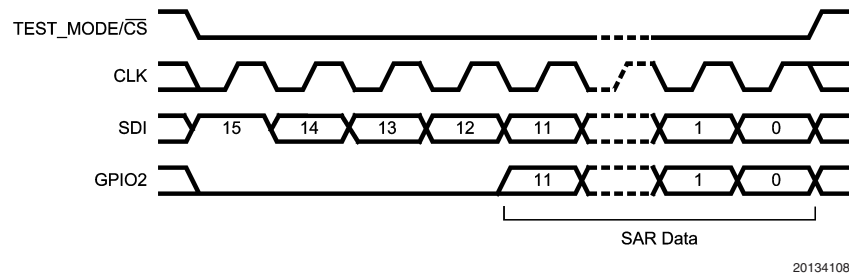
The full scale digital output from the SAR is equal to 2.5V. The  $A_{V_{DD}}$  and  $D_{V_{DD}}$  inputs are divided by two during sampling. The SAR ADC can be activated at any time, even while the chip is in shutdown mode (chip mode '00'). This allows the LM4935 to perform housekeeping duties such as voltage monitoring with minimal power consumption.

\*Depending on SLOT\_2\_VBB in SAR\_SLOT23 (0x1Ch).

## 12.0 Status & Control Registers (Continued)

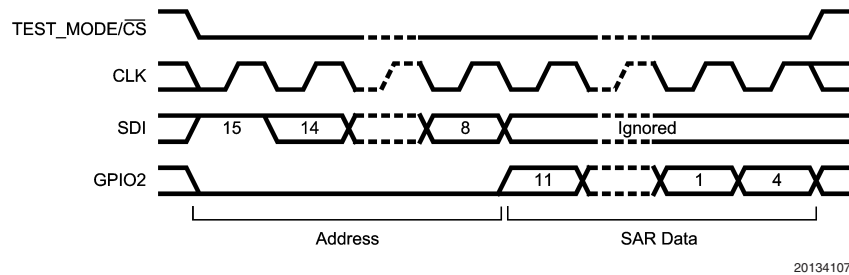
Only the 8 MSBS [11:4] from the 12 bits of SAR output data can be read back using the I<sup>2</sup>C interface.

The SPI interface can be used to access all 12 bits of the SAR output data. In this case, GPIO2 should be set to SAR\_SDO by setting GPIO\_SEL in register (0x1Ah). The SAR channel selected by SAR\_CH\_SEL in the GPIO register is then output onto GPIO2 as follows:



**FIGURE 14. SPI SAR Read Transaction (GPIO2 set to SAR\_SDO)**

In applications where the 8 MSBS [11:4] from the SAR output data is enough resolution, GPIO2 should be set to SPI\_SDO by setting GPIO\_SEL in register (0x1Ah). The SAR data is then output on GPIO2 as follows:



**FIGURE 15. SPI SAR Read Transaction (GPIO2 set to SPI\_SDO)**

If the user performs a write to the GPIO register the changes will not take effect until the next SPI operation so SAR data can be read while the next channel is being selected. The SAR data is sampled at the start of the SPI transaction to ensure that the data is stable during the read operation.

All 12 bits of the SAR output data for up to 2 SAR channels can be read back simultaneously through the bi-directional I<sup>2</sup>S interface. This is accomplished by setting I2S\_SDO\_DATA (bit [7:6] of (0x19h)) to the desired SAR channel(s).

As mentioned previously in the **Digital Audio Data Formats** section, when SAR SDO is passed to the I<sup>2</sup>S bus, the SAR SDO's MSB is aligned with the MSB of I2S\_SDO.

## 12.0 Status & Control Registers (Continued)

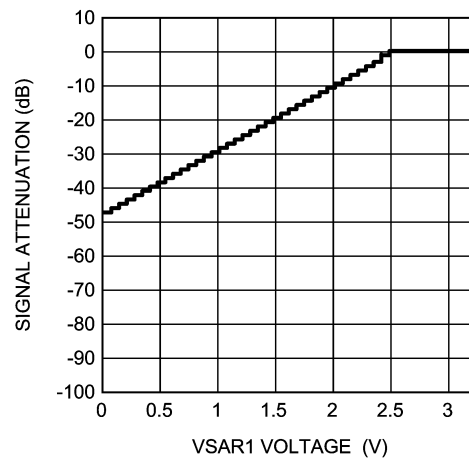
### 12.38 DC VOLUME CONFIGURATION REGISTER

This register is used to control the DC volume control system.

**TABLE 39. DC\_VOLUME (0x21h)**

| Bits | Field         | Description                                                                                                                           |
|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 0    | DC_VOL_ENB    | Enables the DC volume control system to use the voltage applied on the VSAR 1 pin to set the gain of the DC volume control. (Note 32) |
| 1    | DC_VOL_EFFECT | Selects which volume is altered:                                                                                                      |
|      |               | DC_VOL_EFFECT      Source                                                                                                             |
|      |               | 0      AUX/DAC                                                                                                                        |
|      |               | 1      CPI                                                                                                                            |
| 3:2  | MAX_LEVEL     | Programs the maximum level that can be applied by the system                                                                          |
|      |               | MAX_LEVEL      LEVEL                                                                                                                  |
|      |               | 00 <sub>2</sub> 0 dB                                                                                                                  |
|      |               | 01 <sub>2</sub> -3 dB                                                                                                                 |
|      |               | 10 <sub>2</sub> -6 dB                                                                                                                 |
|      |               | 11 <sub>2</sub> -12 dB                                                                                                                |

**Note 32:** The correlation between the voltage on VSAR1 to the attenuation on the AUX/DAC channel is as follows:



201341P4

**FIGURE 16. DC Volume Transfer Function For AUX/DAC**



## 12.0 Status & Control Registers (Continued)

### 12.39 SAR TRIGGER 1 CONFIGURATION REGISTER

This register is used to setup a voltage trigger on one of the SAR outputs.

**TABLE 40. TRIG\_1 (0x22h)**

| Bits | Field           | Description                                                           |
|------|-----------------|-----------------------------------------------------------------------|
| 0    | TRIG_1_ENB      | Enables the 1st SAR trigger interrupt, if cleared will clear the IRQ. |
| 1    | TRIG_1_DIR      | Selects the direction the voltage should be moving:                   |
|      | TRIG_1_DIR      | Trigger if signal passes:                                             |
|      | 0               | Above Threshold                                                       |
|      | 1               | Below Threshold                                                       |
| 3:2  | TRIG_1_SOURCE   | Programs the channel used by the trigger.                             |
|      | TRIG_1_SOURCE   | Source                                                                |
|      | 00 <sub>2</sub> | VSAR_1                                                                |
|      | 01 <sub>2</sub> | VSAR_2                                                                |
|      | 10 <sub>2</sub> | D_V <sub>DD</sub> /2 or BB_V <sub>DD</sub>                            |
|      | 11 <sub>2</sub> | A_V <sub>DD</sub> /2                                                  |
| 7:4  | TRIG_1_LSB      | Sets bits 3:0 of the threshold used by the trigger.                   |

# 12.0 Status & Control Registers (Continued)

## 12.40 SAR TRIGGER 1 MSBs CONFIGURATION REGISTER

This register is used to setup the threshold of a voltage trigger on one of the SAR outputs.

TABLE 41. TRIG\_1\_MSB (0x23h)

| Bits | Field      | Description                                          |
|------|------------|------------------------------------------------------|
| 7:0  | TRIG_1_MSB | Sets bits 11:4 of the threshold used by the trigger. |

## 12.0 Status & Control Registers (Continued)

### 12.41 SAR TRIGGER 2 CONFIGURATION REGISTER

This register is used to setup a voltage trigger on one of the SAR outputs.

**TABLE 42. TRIG\_2 (0x24h)**

| Bits | Field         | Description                                                           |                                            |
|------|---------------|-----------------------------------------------------------------------|--------------------------------------------|
| 0    | TRIG_2_ENB    | Enables the 2nd SAR trigger interrupt, if cleared will clear the IRQ. |                                            |
| 1    | TRIG_2_DIR    | Selects the direction the voltage should be moving:                   |                                            |
|      |               | TRIG_2_DIR                                                            | Trigger if signal passes:                  |
|      |               | 0                                                                     | Above Threshold                            |
|      |               | 1                                                                     | Below Threshold                            |
| 3:2  | TRIG_2_SOURCE | Programs the channel used by the trigger                              |                                            |
|      |               | TRIG_2_SOURCE                                                         | Source                                     |
|      |               | 00 <sub>2</sub>                                                       | VSAR_1                                     |
|      |               | 01 <sub>2</sub>                                                       | VSAR_2                                     |
|      |               | 10 <sub>2</sub>                                                       | D_V <sub>DD</sub> /2 or BB_V <sub>DD</sub> |
|      |               | 11 <sub>2</sub>                                                       | A_V <sub>DD</sub> /2                       |
| 7:4  | TRIG_2_LSB    | Sets bits 3:0 of the threshold used by the trigger.                   |                                            |

12.0 Status & Control Registers (Continued)

12.42 SAR TRIGGER 2 MSBs CONFIGURATION REGISTER

This register is used to setup the threshold of a voltage trigger on one of the SAR outputs.

TABLE 43. TRIG\_2\_MSB (0x25h)

| Bits | Field      | Description                                          |
|------|------------|------------------------------------------------------|
| 7:0  | TRIG_2_MSB | Sets bits 11:4 of the threshold used by the trigger. |

## 12.0 Status & Control Registers (Continued)

### 12.43 DEBUG REGISTER

This register is used to set test modes within the device.

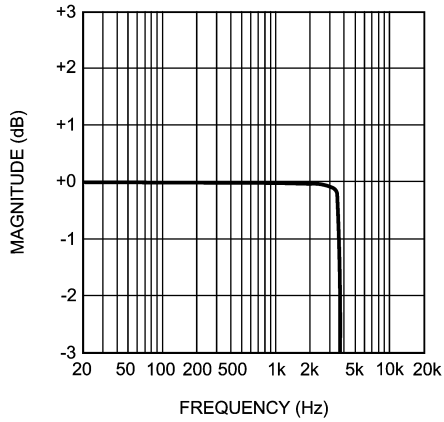
**TABLE 44. DEBUG (0x26h)**

| Bits | Field          | Description                                                                                                                                                      |
|------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | RSVD           | Reserved                                                                                                                                                         |
| 1    | RSVD           | Reserved                                                                                                                                                         |
| 2    | RSVD           | Reserved                                                                                                                                                         |
| 3    | SOFT_RESET     | This field can be used to reset the chip without a power cycle.                                                                                                  |
| 4    | RSVD           | Reserved                                                                                                                                                         |
| 5    | RSVD           | Reserved                                                                                                                                                         |
| 6    | RSVD           | Reserved                                                                                                                                                         |
| 7    | GPIO_TEST_MODE | If set and GPIO_SEL = '010', then the GPIOs are configured to interface with the LMV1026 digital microphone as long as AUDIO_IF_MODE (0x19h) is not set to '11'. |
|      |                | GPIO_SEL                                                                                                                                                         |
|      |                | GPIO 1                                                                                                                                                           |
|      |                | GPIO 2                                                                                                                                                           |
|      |                | 000 <sub>2</sub>                                                                                                                                                 |
|      |                | 001 <sub>2</sub>                                                                                                                                                 |
|      |                | 010 <sub>2</sub>                                                                                                                                                 |
|      |                | 011 <sub>2</sub>                                                                                                                                                 |
|      |                | 100 <sub>2</sub>                                                                                                                                                 |
|      |                | 101 <sub>2</sub>                                                                                                                                                 |
|      |                | 110 <sub>2</sub>                                                                                                                                                 |
|      |                | 111 <sub>2</sub>                                                                                                                                                 |
|      |                | VADC_CLOCK_OUT                                                                                                                                                   |
|      |                | DIG_MIC_IN                                                                                                                                                       |
|      |                | RSVD                                                                                                                                                             |
|      |                | RSVD                                                                                                                                                             |
|      |                | RSVD                                                                                                                                                             |
|      |                | RSVD                                                                                                                                                             |
|      |                | RSVD                                                                                                                                                             |
|      |                | RSVD                                                                                                                                                             |

## 13.0 Typical Performance Characteristics

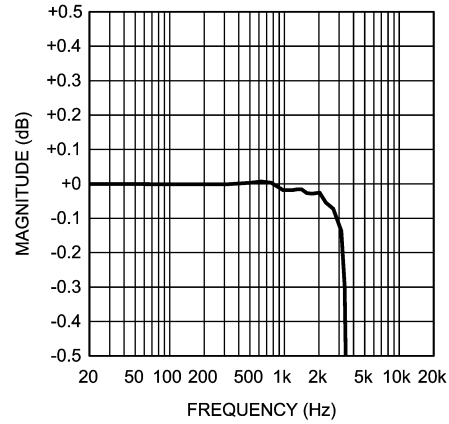
(For all performance curves  $AV_{DD}$  refers to the voltage applied to the  $A\_V_{DD}$  and  $LS\_V_{DD}$  pins.  $DV_{DD}$  refers to the voltage applied to the  $D\_V_{DD}$  and  $PLL\_V_{DD}$  pins;  $AV_{DD} = 3.3V$  and  $DV_{DD} = 3.3V$  unless otherwise specified.)

**Stereo DAC Frequency Response**  
 $f_s = 8kHz$



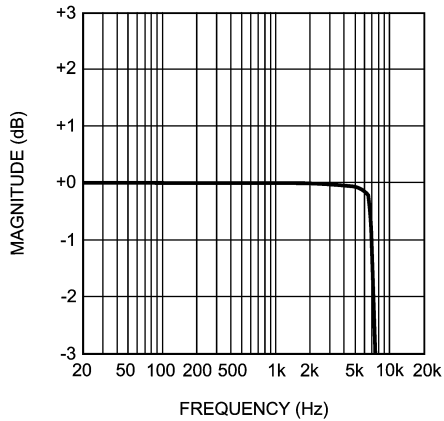
20134136

**Stereo DAC Frequency Response Zoom**  
 $f_s = 8kHz$



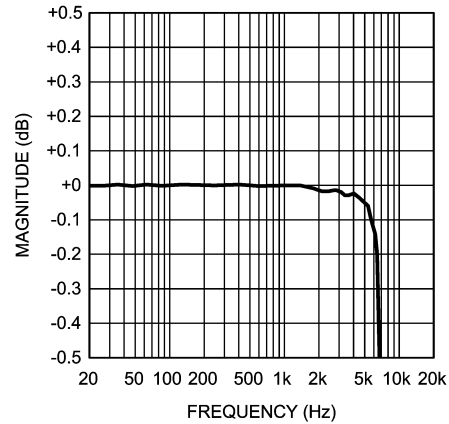
20134137

**Stereo DAC Frequency Response**  
 $f_s = 16kHz$



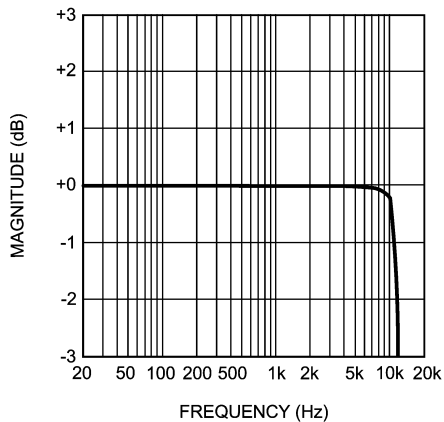
20134138

**Stereo DAC Frequency Response Zoom**  
 $f_s = 16kHz$



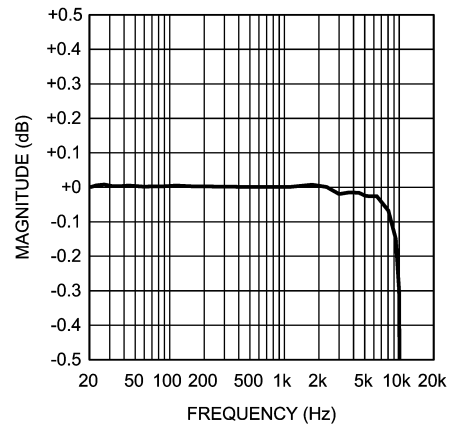
20134139

**Stereo DAC Frequency Response**  
 $f_s = 24kHz$



20134140

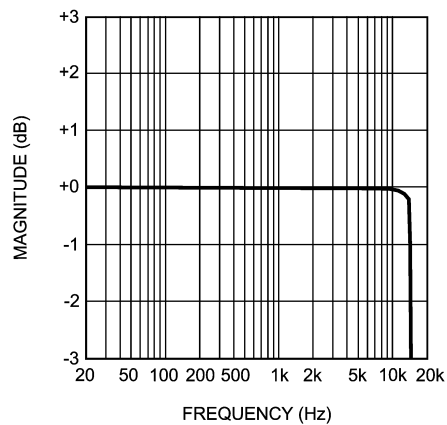
**Stereo DAC Frequency Response Zoom**  
 $f_s = 24kHz$



20134141

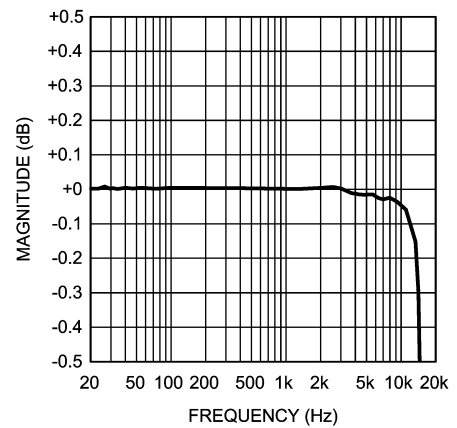
# 13.0 Typical Performance Characteristics (Continued)

**Stereo DAC Frequency Response**  
 $f_s = 32\text{kHz}$



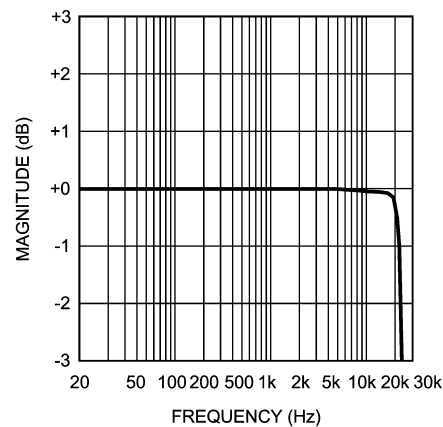
20134142

**Stereo DAC Frequency Response Zoom**  
 $f_s = 32\text{kHz}$



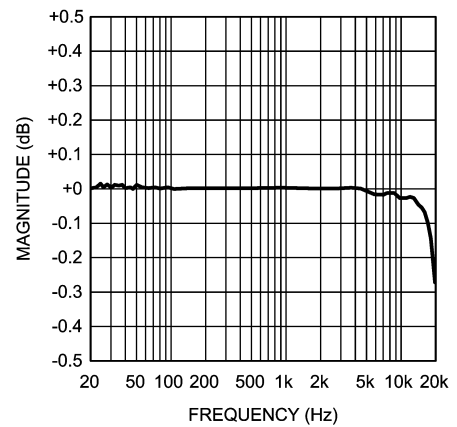
20134143

**Stereo DAC Frequency Response**  
 $f_s = 48\text{kHz}$



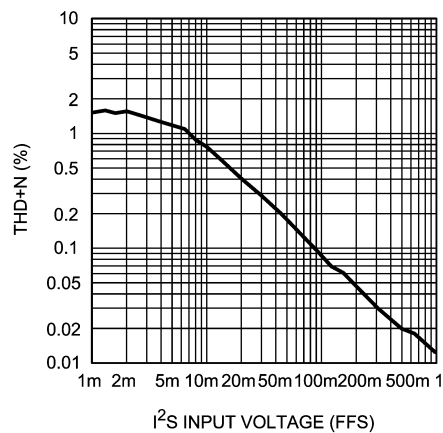
20134144

**Stereo DAC Frequency Response Zoom**  
 $f_s = 48\text{kHz}$



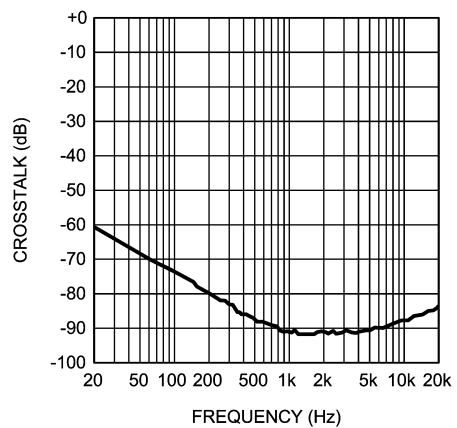
20134145

**THD+N vs**  
**Stereo DAC Input Voltage**  
**(0dB DAC, AUXOUT)**



20134146

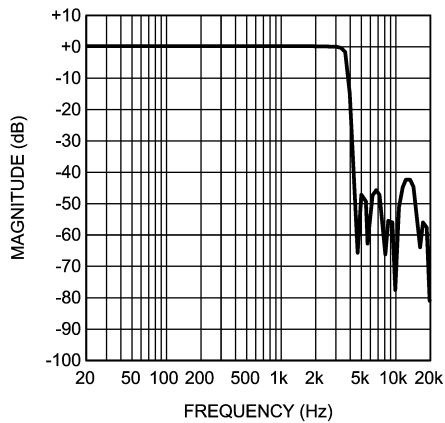
**Stereo DAC Crosstalk**  
**(0dB DAC, HP SE)**



20134147

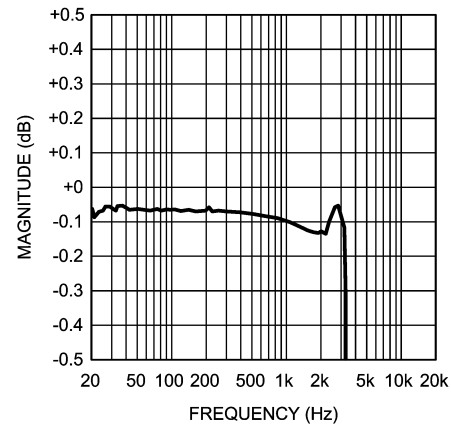
# 13.0 Typical Performance Characteristics (Continued)

**MONO ADC Frequency Response**  
 $f_s = 8\text{kHz}$ , 6dB MIC



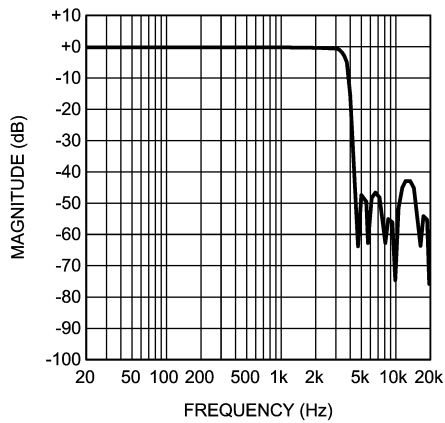
20134148

**MONO ADC Frequency Response Zoom**  
 $f_s = 8\text{kHz}$ , 6dB MIC



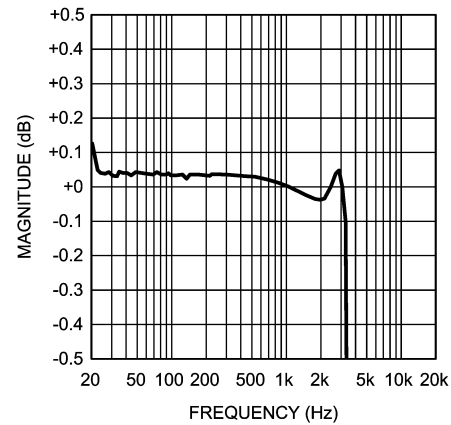
20134149

**MONO ADC Frequency Response**  
 $f_s = 8\text{kHz}$ , 36dB MIC



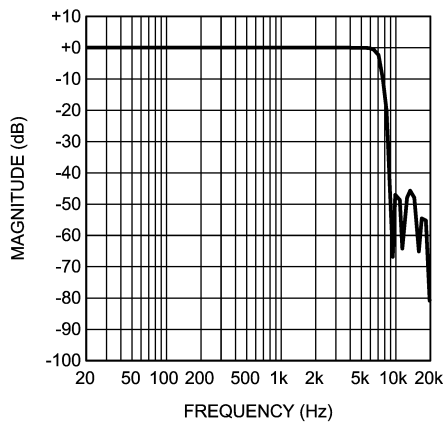
20134150

**MONO ADC Frequency Response Zoom**  
 $f_s = 8\text{kHz}$ , 36dB MIC



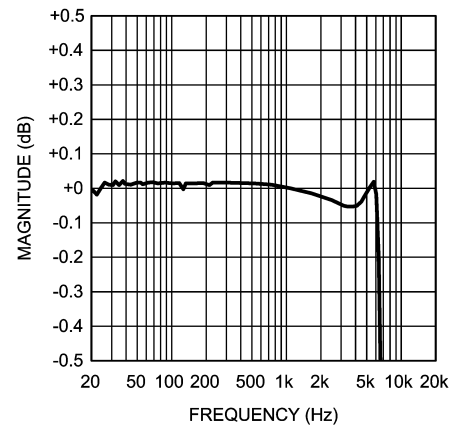
20134151

**MONO ADC Frequency Response**  
 $f_s = 16\text{kHz}$ , 6dB MIC



20134152

**MONO ADC Frequency Response Zoom**  
 $f_s = 16\text{kHz}$ , 6dB MIC

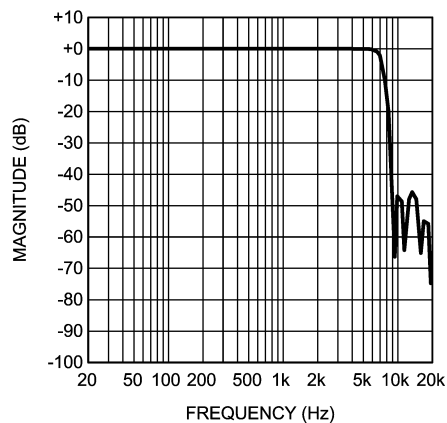


20134153



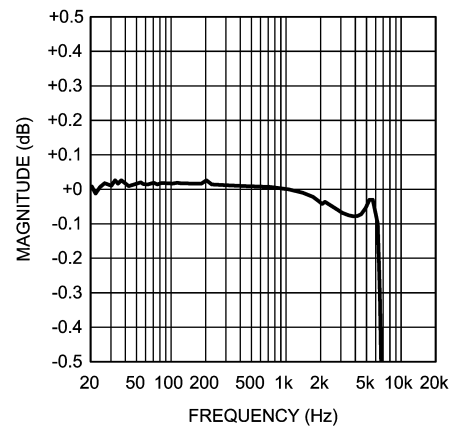
# 13.0 Typical Performance Characteristics (Continued)

**MONO ADC Frequency Response**  
 $f_s = 16\text{kHz}$ , 36dB MIC



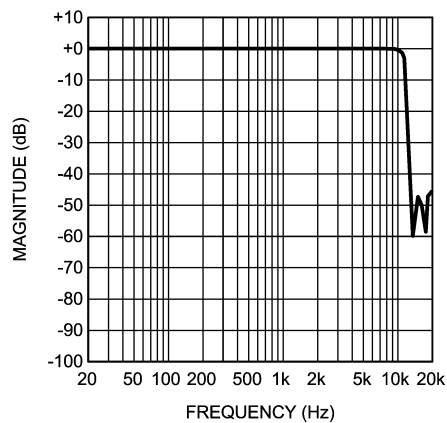
20134154

**MONO ADC Frequency Response Zoom**  
 $f_s = 16\text{kHz}$ , 36dB MIC



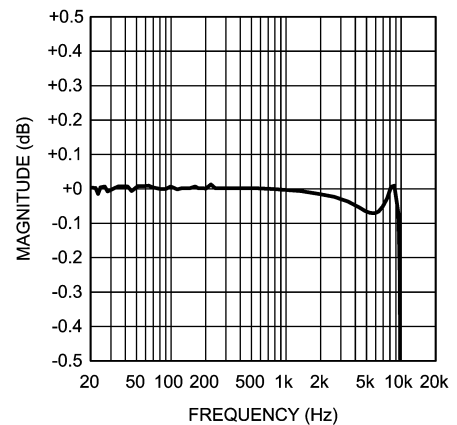
20134155

**MONO ADC Frequency Response**  
 $f_s = 24\text{kHz}$ , 6dB MIC



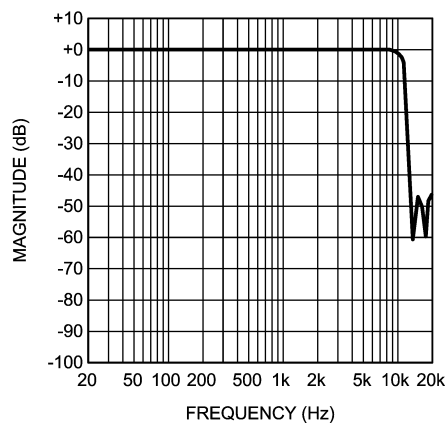
20134156

**MONO ADC Frequency Response Zoom**  
 $f_s = 24\text{kHz}$ , 6dB MIC



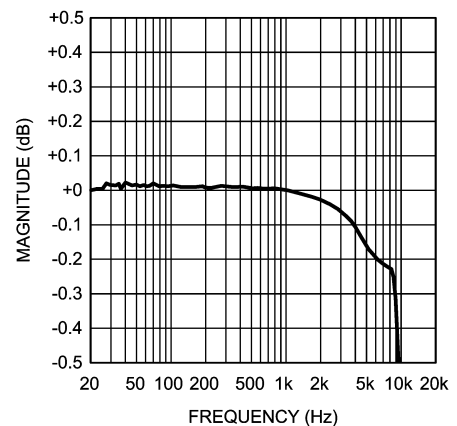
20134157

**MONO ADC Frequency Response**  
 $f_s = 24\text{kHz}$ , 36dB MIC



20134158

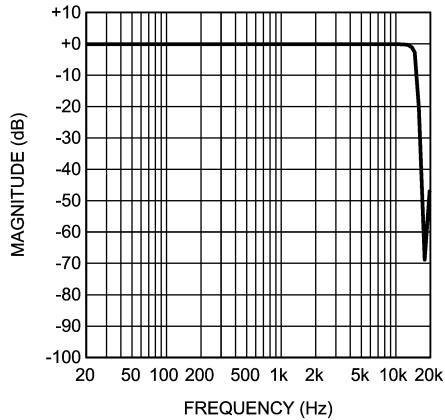
**MONO ADC Frequency Response Zoom**  
 $f_s = 24\text{kHz}$ , 36dB MIC



20134169

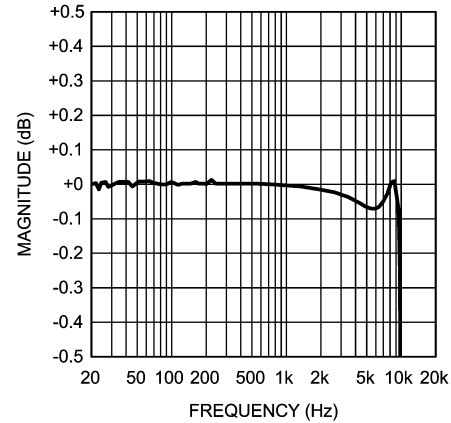
## 13.0 Typical Performance Characteristics (Continued)

**MONO ADC Frequency Response**  
 $f_s = 32\text{kHz}$ , 6dB MIC



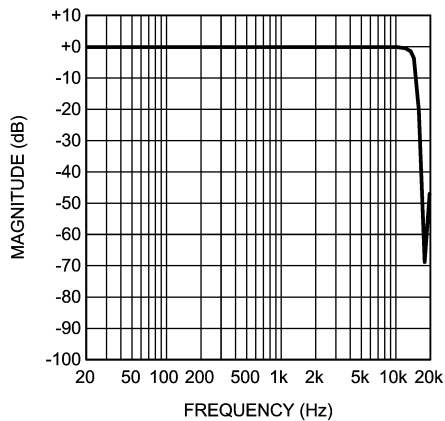
20134159

**MONO ADC Frequency Response Zoom**  
 $f_s = 32\text{kHz}$ , 6dB MIC



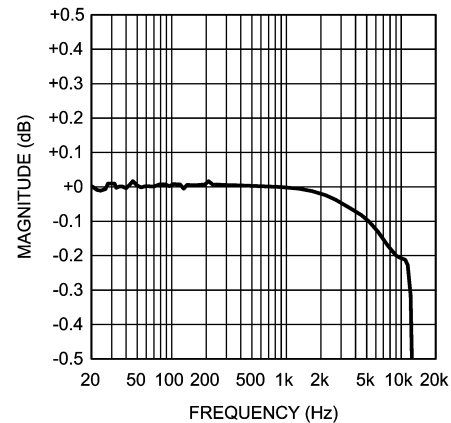
20134160

**MONO ADC Frequency Response**  
 $f_s = 32\text{kHz}$ , 36dB MIC



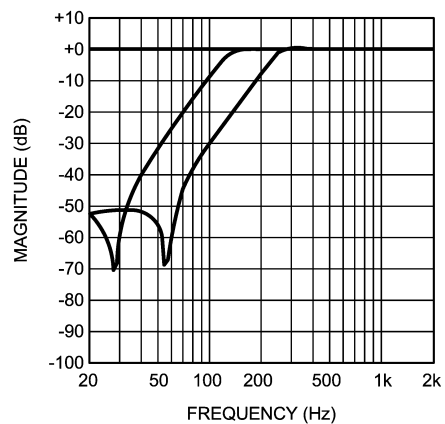
20134161

**MONO ADC Frequency Response Zoom**  
 $f_s = 32\text{kHz}$ , 36dB MIC



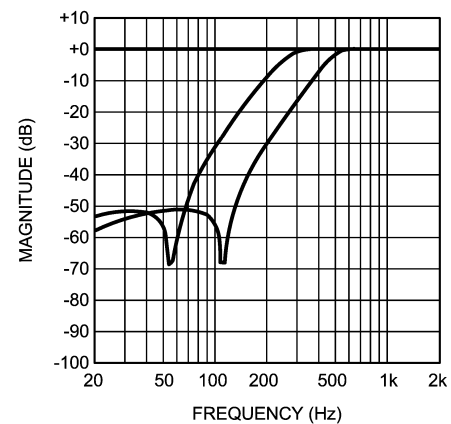
20134162

**MONO ADC HPF Frequency Response**  
 $f_s = 8\text{kHz}$ , 36dB MIC  
 (from left to right: HPF\_MODE '00', '10', '01')



20134163

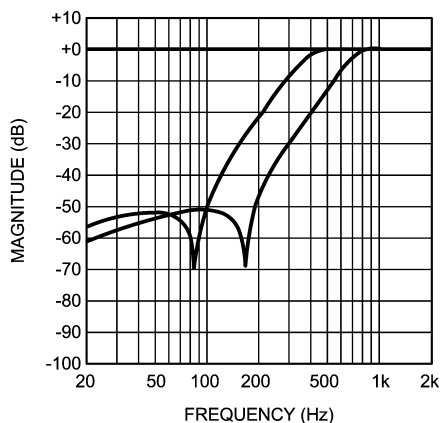
**MONO ADC HPF Frequency Response**  
 $f_s = 16\text{kHz}$ , 36dB MIC  
 (from left to right: HPF\_MODE '00', '10', '01')



20134164

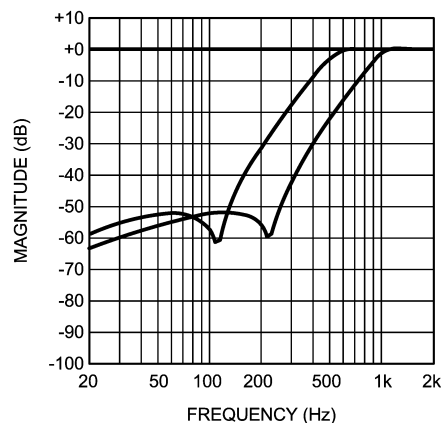
## 13.0 Typical Performance Characteristics (Continued)

**MONO ADC HPF Frequency Response**  
 $f_s = 24\text{kHz}$ , 36dB MIC  
 (from left to right: HPF\_MODE '00', '10', '01')



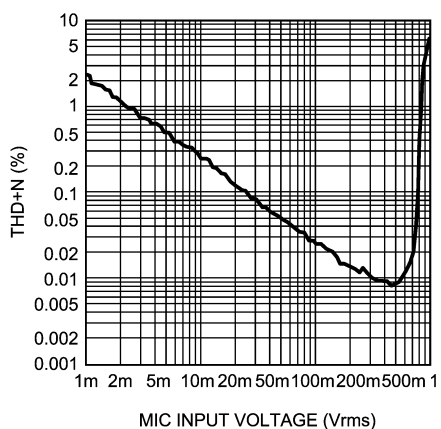
20134165

**MONO ADC HPF Frequency Response**  
 $f_s = 32\text{kHz}$ , 36dB MIC  
 (from left to right: HPF\_MODE '00', '10', '01')



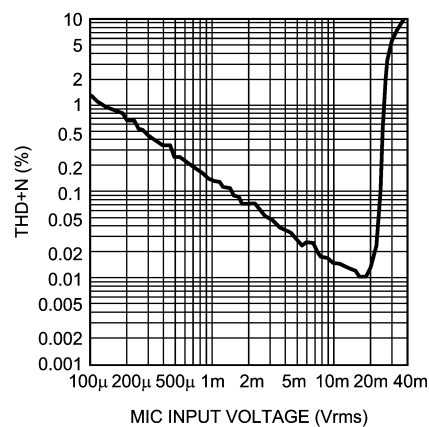
20134166

**MONO ADC THD+N**  
**vs MIC Input Voltage**  
 $(f_s = 8\text{kHz}, 6\text{dB MIC})$



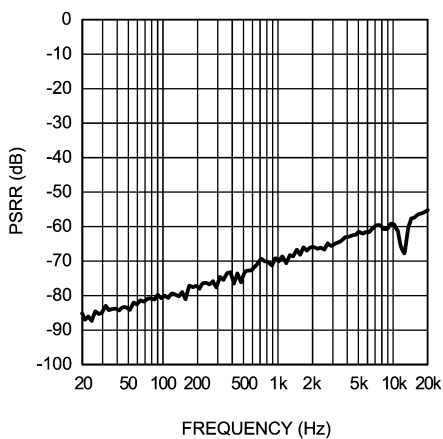
20134167

**MONO ADC THD+N**  
**vs MIC Input Voltage**  
 $(f_s = 8\text{kHz}, 36\text{dB MIC})$



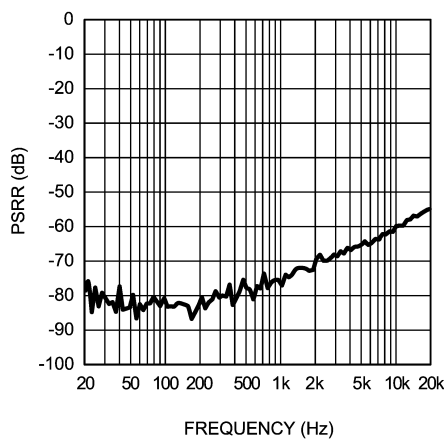
20134168

**MONO ADC PSRR vs Frequency**  
 $AV_{DD} = 3.3\text{V}$ , 6dB MIC



20134170

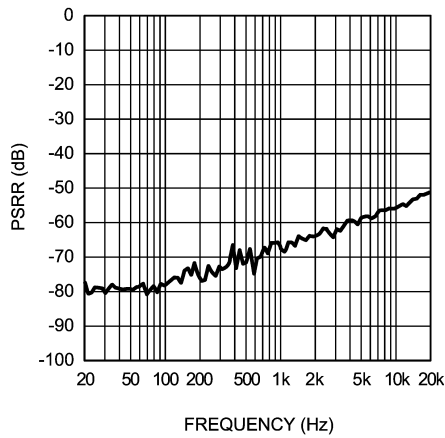
**MONO ADC PSRR vs Frequency**  
 $AV_{DD} = 5\text{V}$ , 6dB MIC



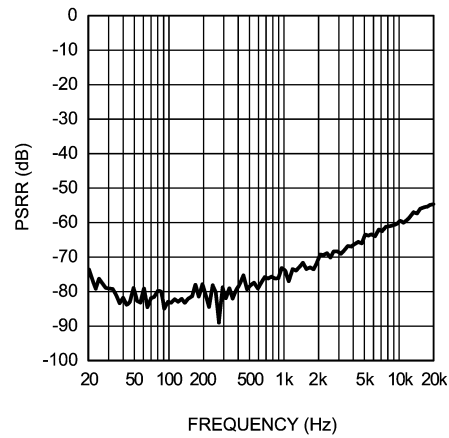
20134171

# 13.0 Typical Performance Characteristics (Continued)

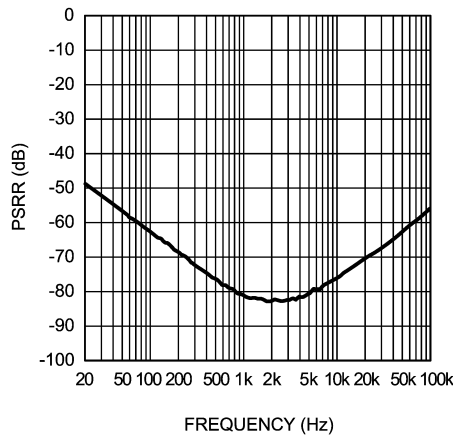
**MONO ADC PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC



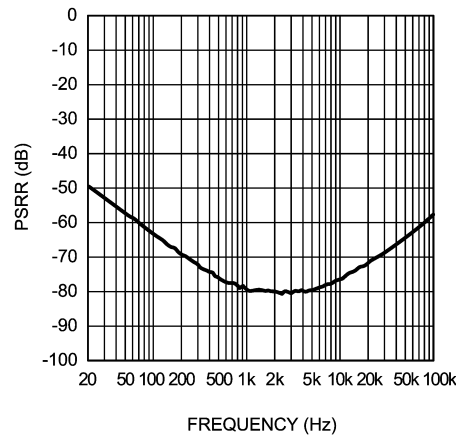
**MONO ADC PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC



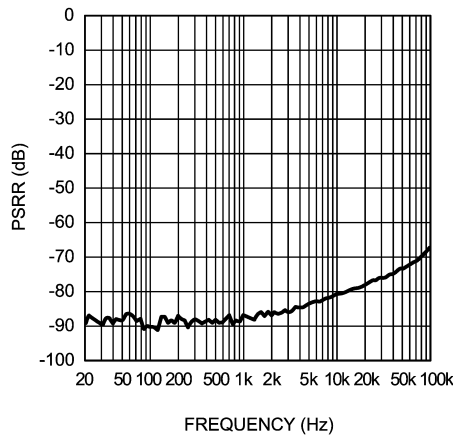
**AUXOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB AUX  
 (AUX inputs terminated)



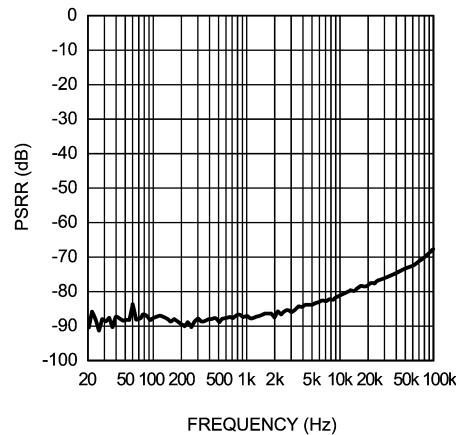
**AUXOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB AUX  
 (AUX inputs terminated)



**AUXOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB CPI  
 (CPI inputs terminated)

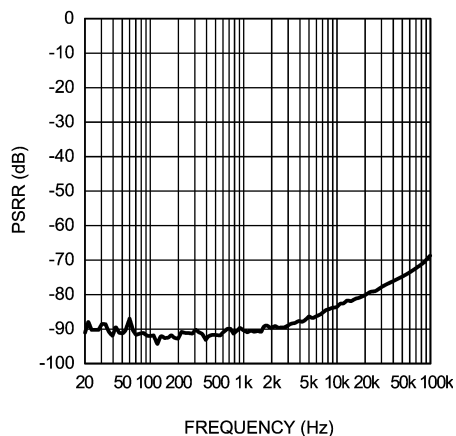


**AUXOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB CPI  
 (CPI inputs terminated)



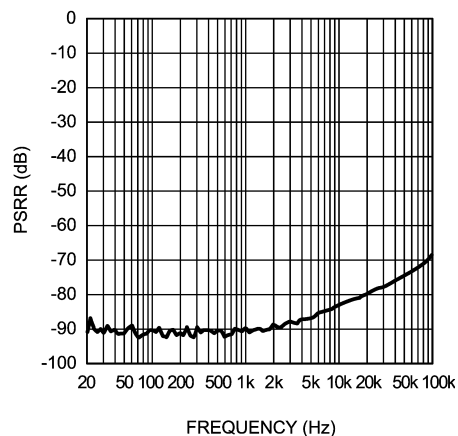
# 13.0 Typical Performance Characteristics (Continued)

**AUXOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB DAC  
 (DAC inputs selected)



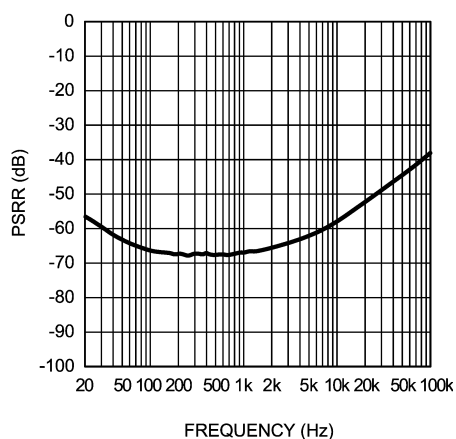
20134178

**AUXOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB DAC  
 (DAC inputs selected)



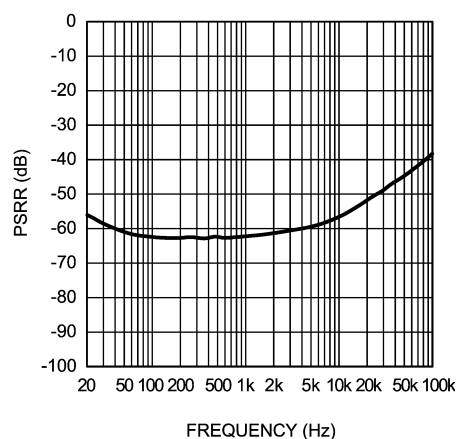
20134179

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB AUX  
 (AUX inputs terminated)



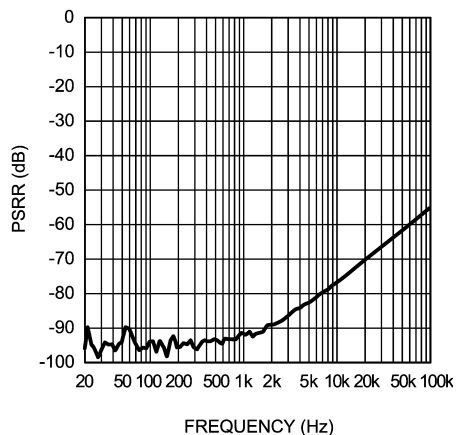
20134180

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB AUX  
 (AUX inputs terminated)



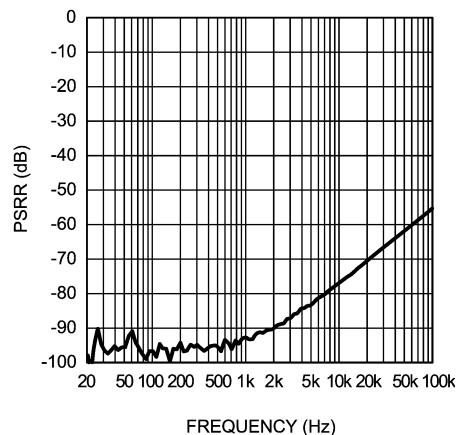
20134181

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB DAC  
 (DAC inputs selected)



20134182

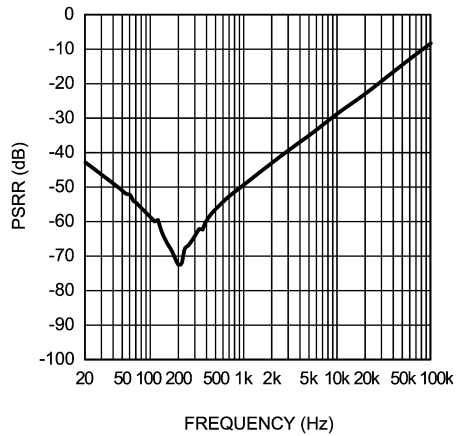
**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB DAC  
 (DAC inputs selected)



20134183

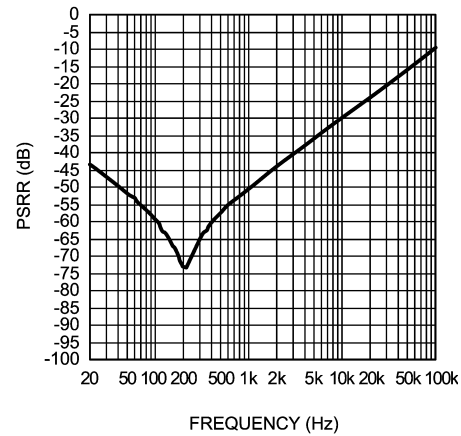
# 13.0 Typical Performance Characteristics (Continued)

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC  
 (EXTMIC inputs terminated, AGC on)



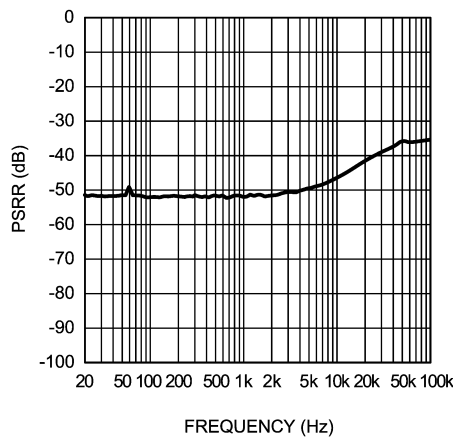
20134185

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC  
 (EXTMIC inputs terminated, AGC on)



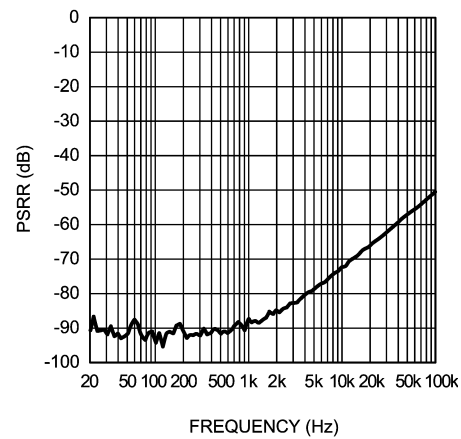
20134187

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC, MICBIAS = 2.0V  
 (INTMIC DIFF inputs terminated, AGC off)



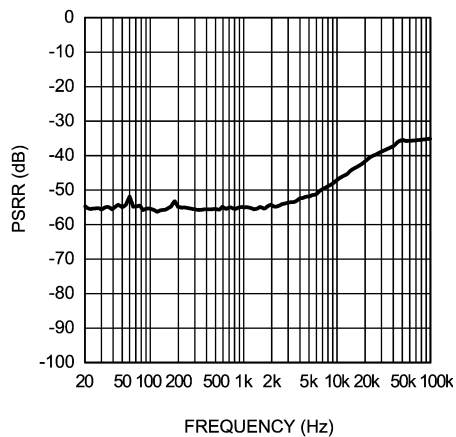
20134188

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC, MICBIAS = 2.0V  
 (INTMIC DIFF inputs terminated, AGC on)



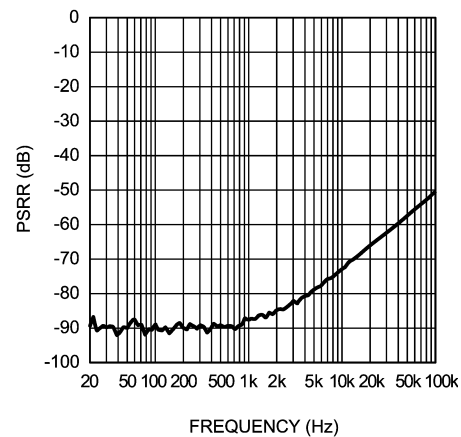
20134189

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC, MICBIAS = 2.5V  
 (INTMIC DIFF inputs terminated, AGC off)



20134190

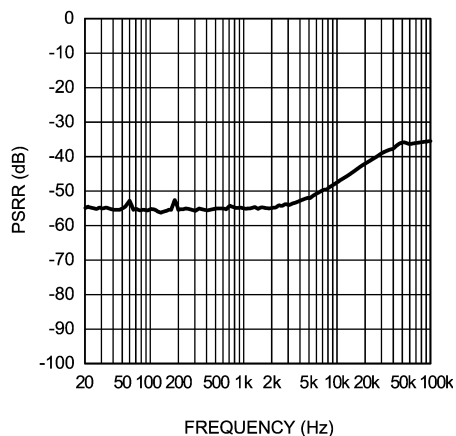
**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC, MICBIAS = 2.5V  
 (INTMIC DIFF inputs terminated, AGC on)



20134191

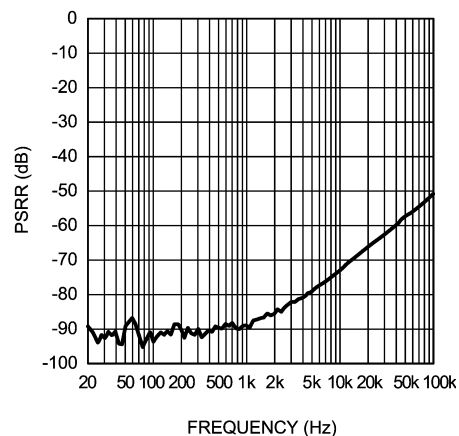
# 13.0 Typical Performance Characteristics (Continued)

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC, MICBIAS = 2.8V  
 (INTMIC DIFF inputs terminated, AGC off)



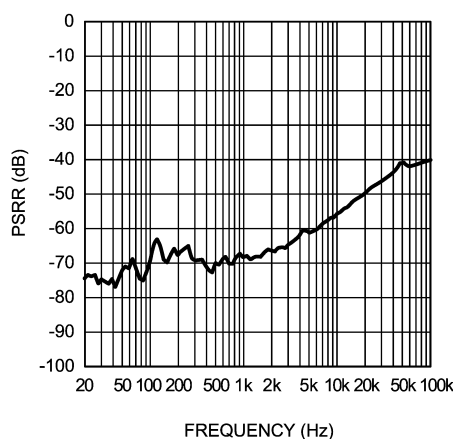
20134192

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC, MICBIAS = 2.8V  
 (INTMIC DIFF inputs terminated, AGC on)



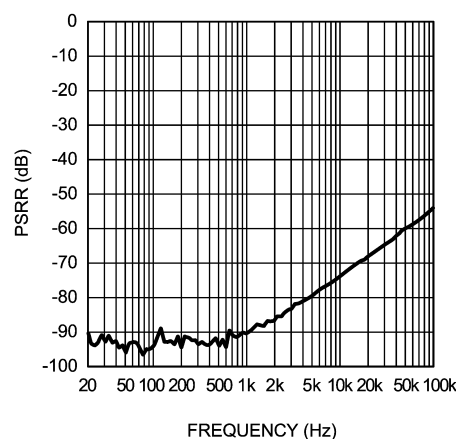
20134193

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 2.0V  
 (INTMIC DIFF inputs terminated, AGC off)



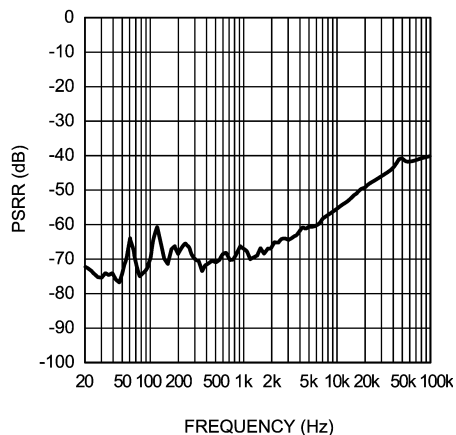
20134196

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 2.0V  
 (INTMIC DIFF inputs terminated, AGC on)



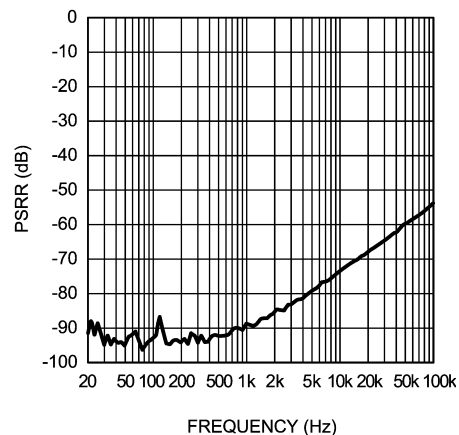
20134197

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 2.5V  
 (INTMIC DIFF inputs terminated, AGC off)



20134198

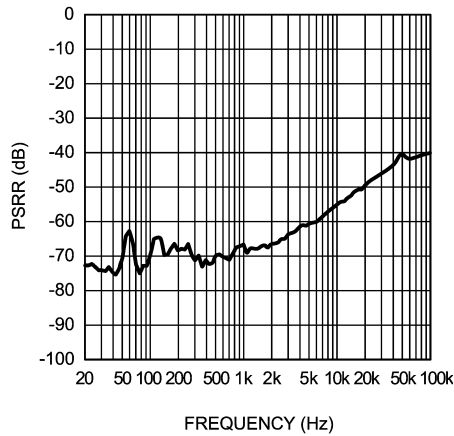
**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 2.5V  
 (INTMIC DIFF inputs terminated, AGC on)



20134199

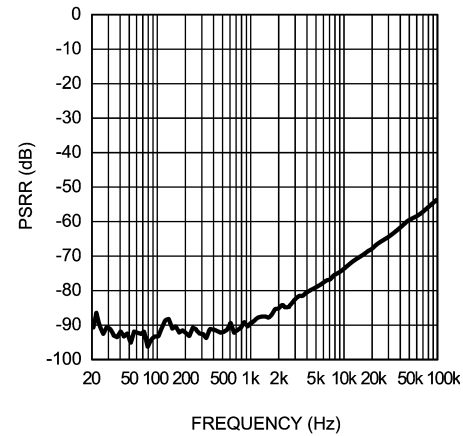
# 13.0 Typical Performance Characteristics (Continued)

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 2.8V  
 (INTMIC DIFF inputs terminated, AGC off)



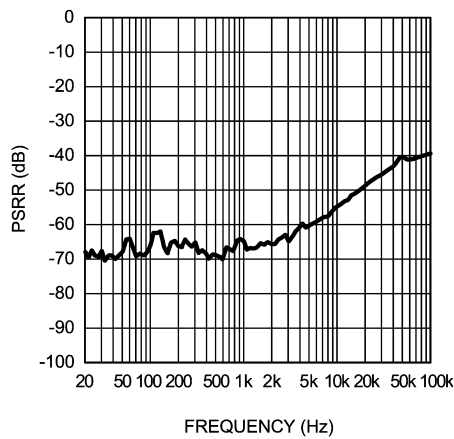
201341A0

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 2.8V  
 (INTMIC DIFF inputs terminated, AGC on)



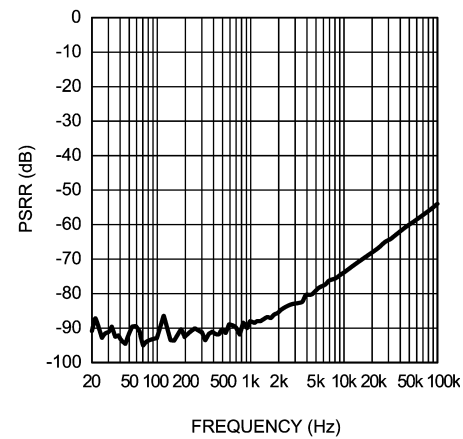
201341A1

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 3.3V  
 (INTMIC DIFF inputs terminated, AGC off)



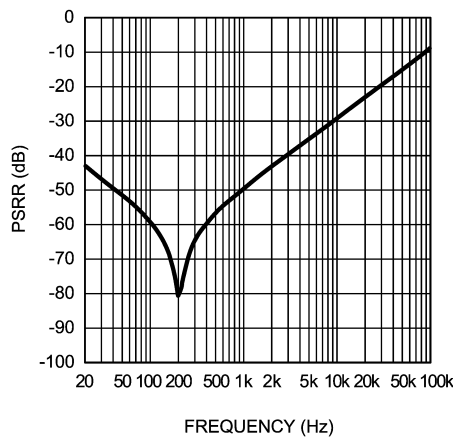
201341A2

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC, MICBIAS = 3.3V  
 (INTMIC DIFF inputs terminated, AGC on)



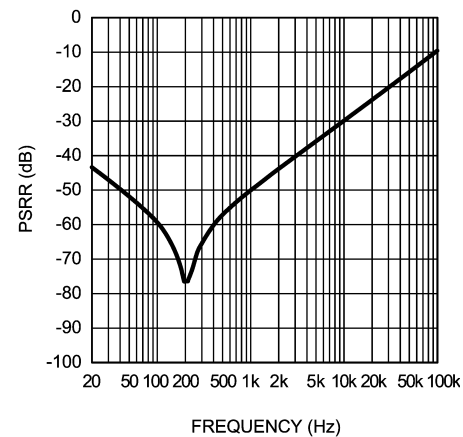
201341A3

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 36dB MIC  
 (INTMIC SE input terminated, AGC on)



201341A5

**CPOUT PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 36dB MIC  
 (INTMIC SE input terminated, AGC on)

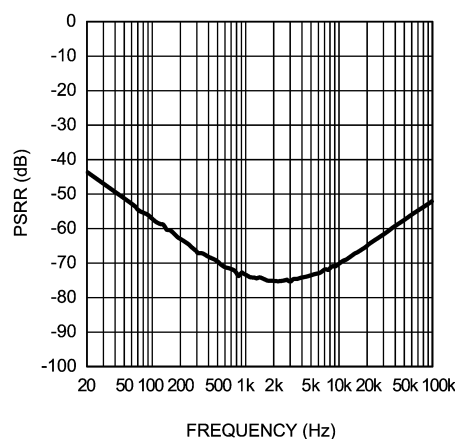


201341A7

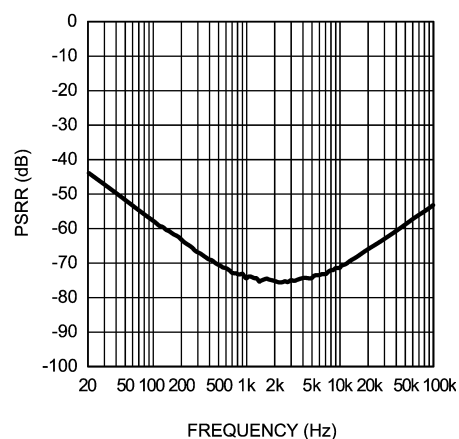


# 13.0 Typical Performance Characteristics (Continued)

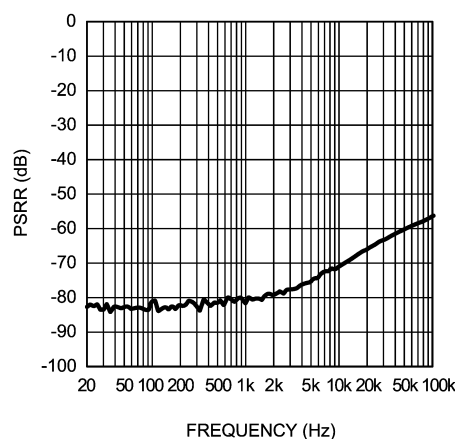
**Earpiece PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB AUX  
 (AUX inputs terminated)



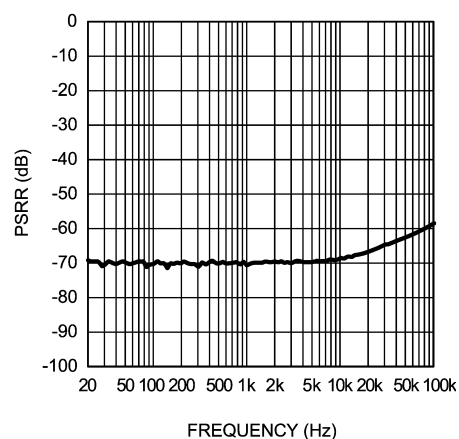
**Earpiece PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB AUX  
 (AUX inputs terminated)



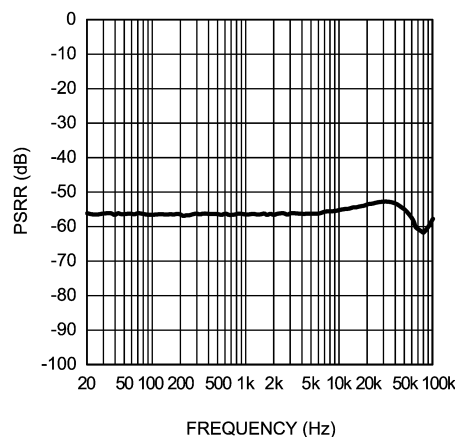
**Earpiece PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB CPI  
 (CPI input terminated)



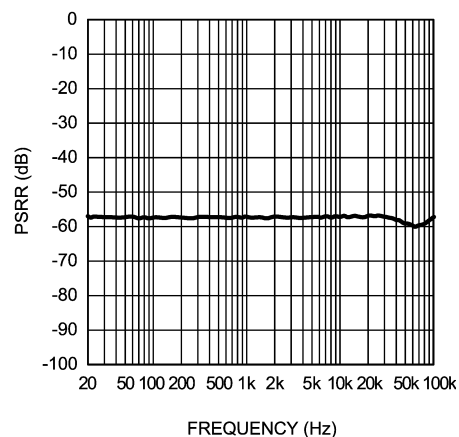
**Earpiece PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB CPI  
 (CPI input terminated)



**Earpiece PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB DAC  
 (DAC input selected)

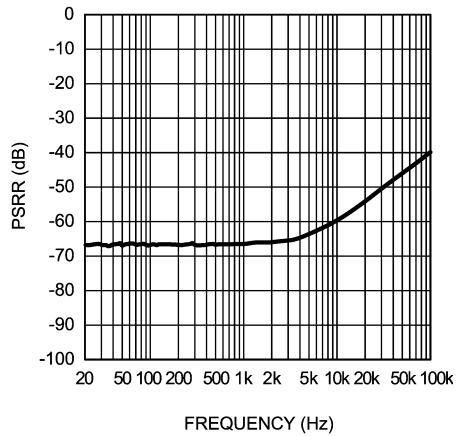


**Earpiece PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB DAC  
 (DAC input selected)

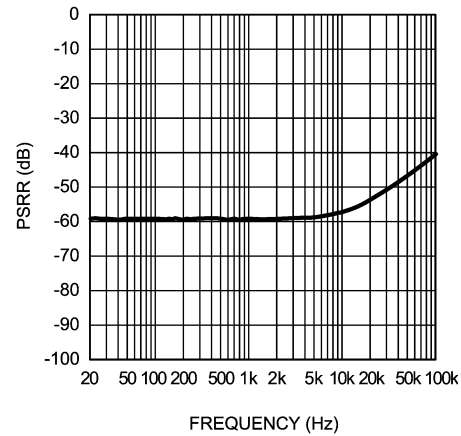


# 13.0 Typical Performance Characteristics (Continued)

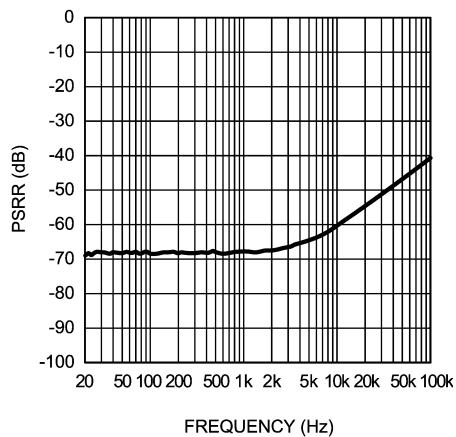
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB AUX, OCL 1.2V  
 (AUX inputs terminated)



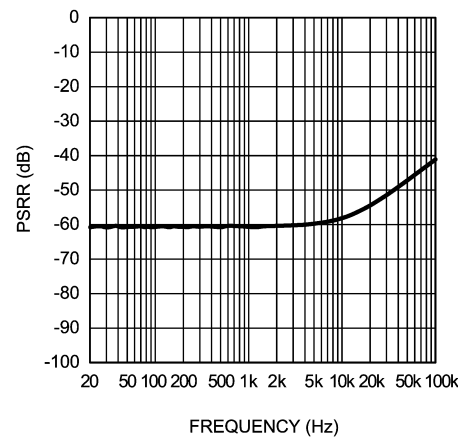
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB AUX, OCL 1.2V  
 (AUX inputs terminated)



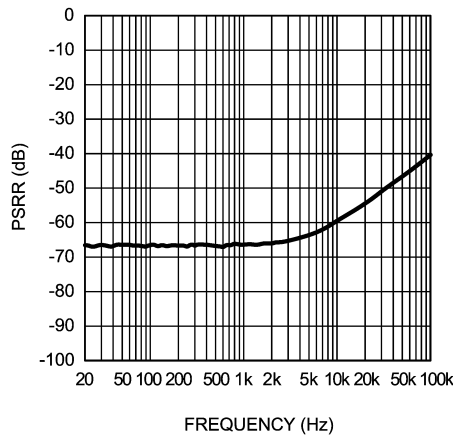
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB CPI, OCL 1.2V  
 (CPI input terminated)



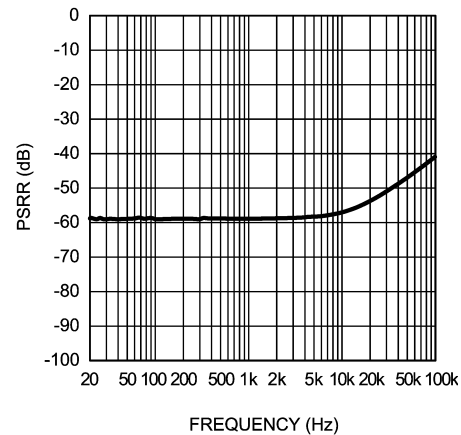
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB CPI, OCL 1.2V  
 (CPI input terminated)



**Headphone PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB ADC, OCL 1.2V  
 (DAC input selected)

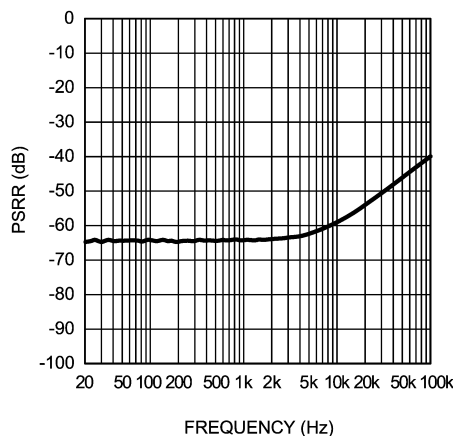


**Headphone PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB ADC, OCL 1.2V  
 (DAC input selected)

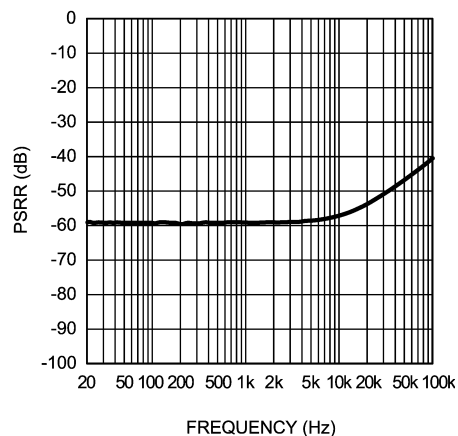


# 13.0 Typical Performance Characteristics (Continued)

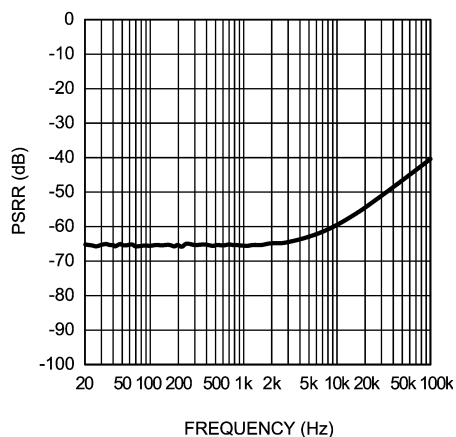
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB AUX, OCL 1.5V  
 (AUX inputs terminated)



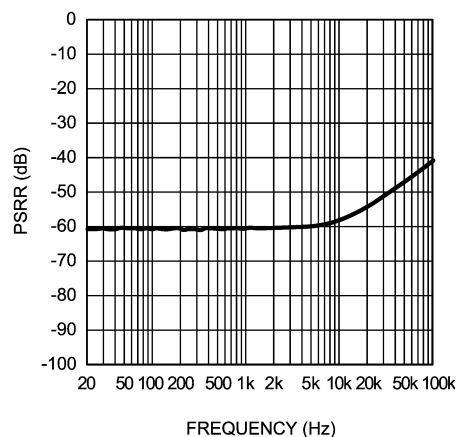
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB AUX, OCL 1.5V  
 (AUX inputs terminated)



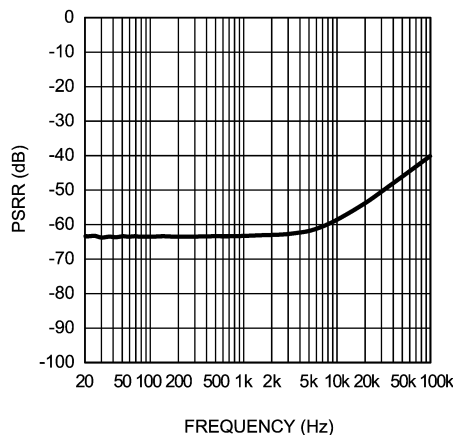
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB CPI, OCL 1.5V  
 (CPI input terminated)



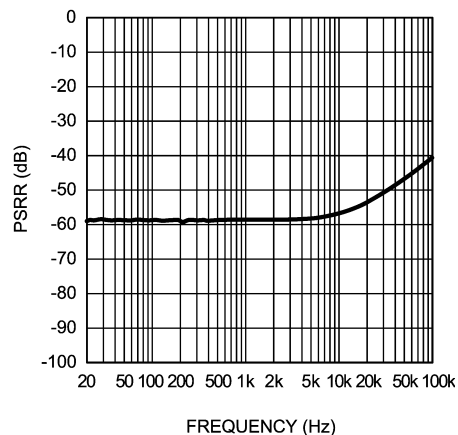
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB CPI, OCL 1.5V  
 (CPI input terminated)



**Headphone PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB DAC, OCL 1.5V  
 (DAC input selected)



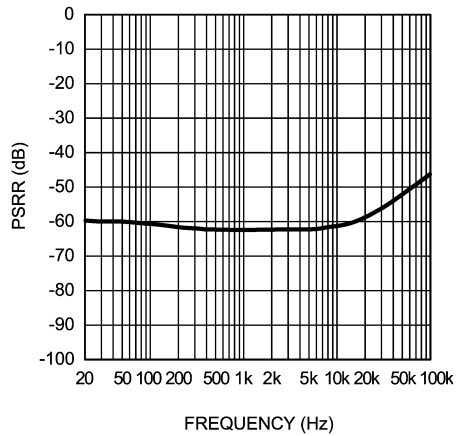
**Headphone PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB DAC, OCL 1.5V  
 (DAC input selected)



## 13.0 Typical Performance Characteristics (Continued)

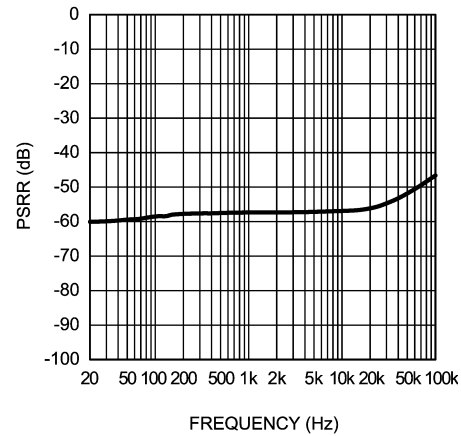
**Headphone PSRR vs Frequency**

$AV_{DD} = 3.3V$ , 0dB AUX, SE  
(AUX inputs terminated)



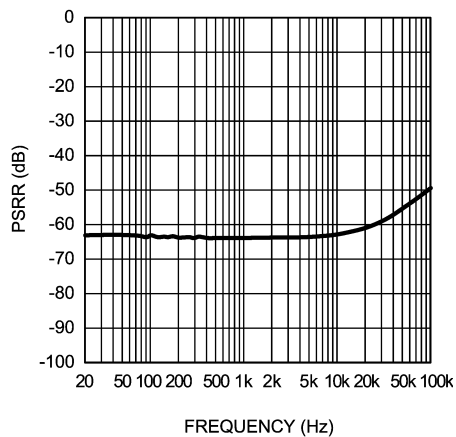
**Headphone PSRR vs Frequency**

$AV_{DD} = 5V$ , 0dB AUX, SE  
(AUX inputs terminated)



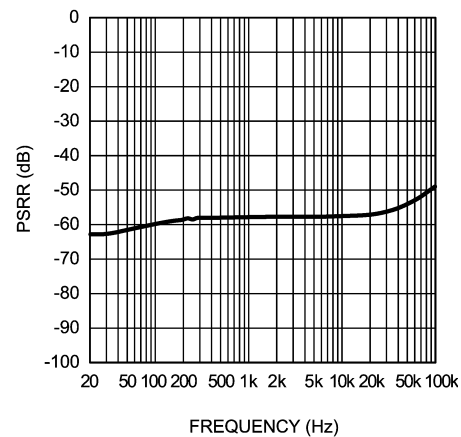
**Headphone PSRR vs Frequency**

$AV_{DD} = 3.3V$ , 0dB CPI, SE  
(CPI input terminated)



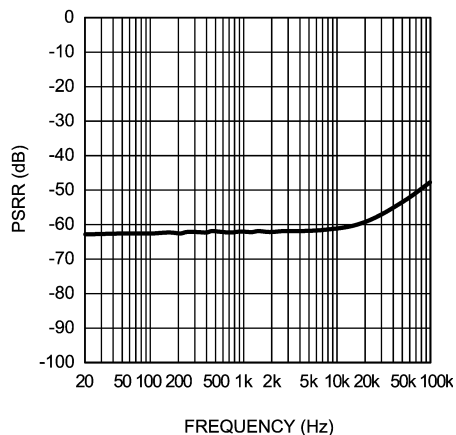
**Headphone PSRR vs Frequency**

$AV_{DD} = 5V$ , 0dB CPI, SE  
(CPI input terminated)



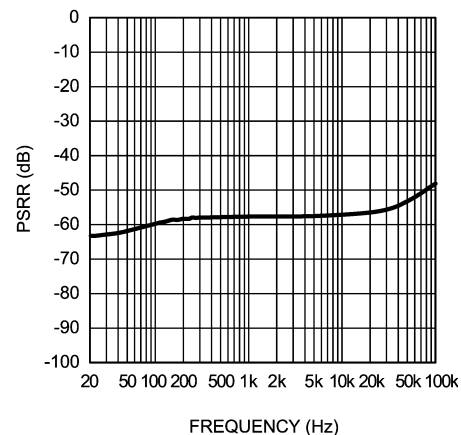
**Headphone PSRR vs Frequency**

$AV_{DD} = 3.3V$ , 0dB DAC, SE  
(DAC input selected)



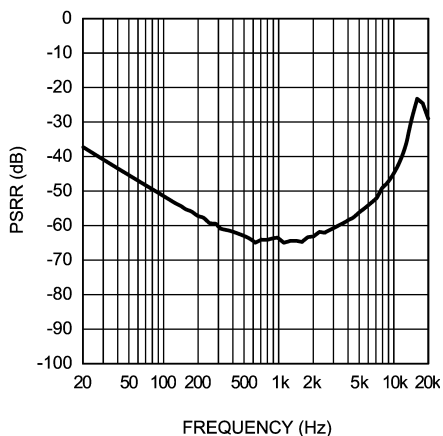
**Headphone PSRR vs Frequency**

$AV_{DD} = 5V$ , 0dB DAC, SE  
(DAC input selected)

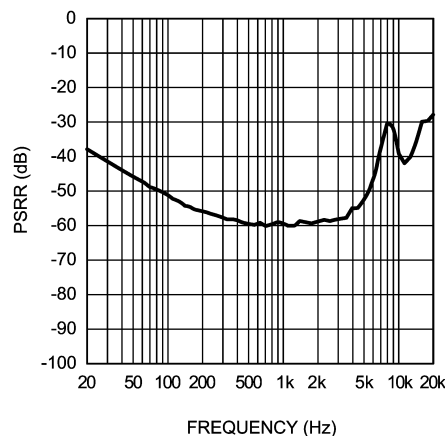


## 13.0 Typical Performance Characteristics (Continued)

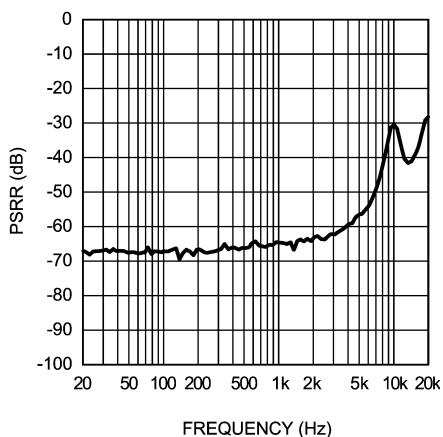
**Loudspeaker PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB AUX  
 (AUX inputs terminated)



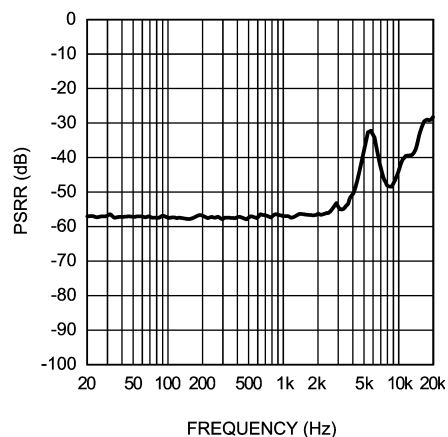
**Loudspeaker PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB AUX  
 (AUX inputs terminated)



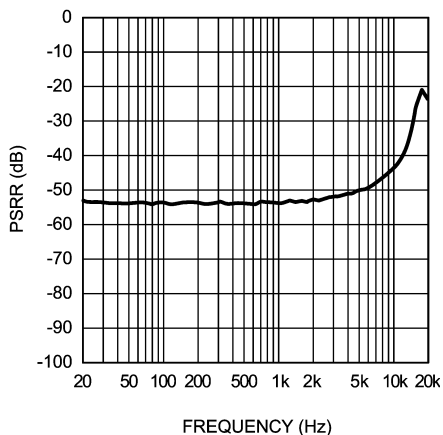
**Loudspeaker PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB CPI  
 (CPI input terminated)



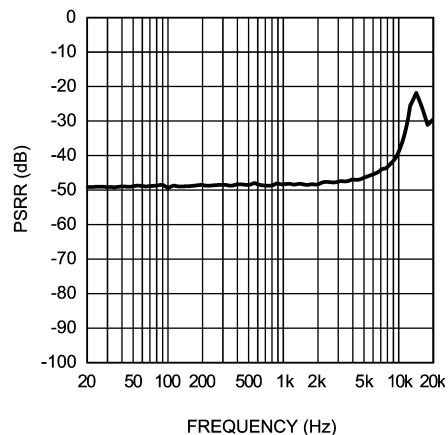
**Loudspeaker PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB CPI  
 (CPI input terminated)



**Loudspeaker PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB DAC  
 (DAC input selected)

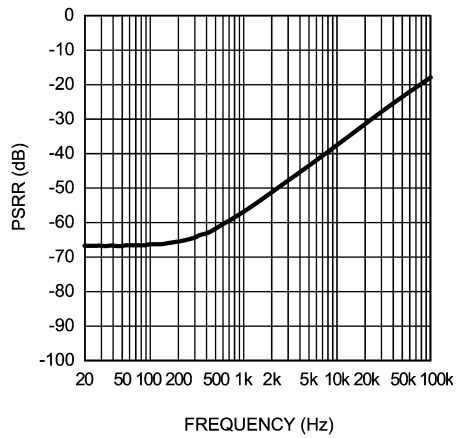


**Loudspeaker PSRR vs Frequency**  
 $AV_{DD} = 5V$ , 0dB DAC  
 (DAC input selected)



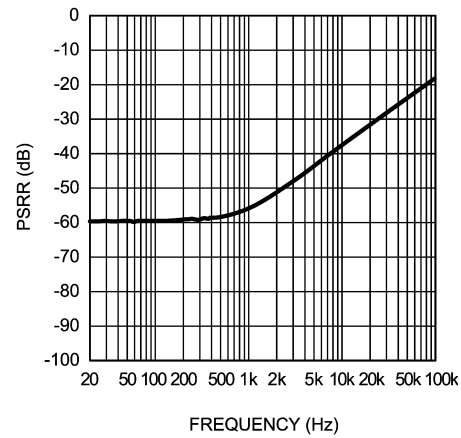
# 13.0 Typical Performance Characteristics (Continued)

**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , MICBIAS = 2.0V



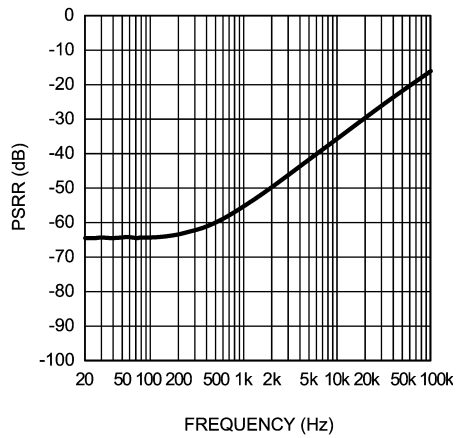
201341D2

**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 5V$ , MICBIAS = 2.0V



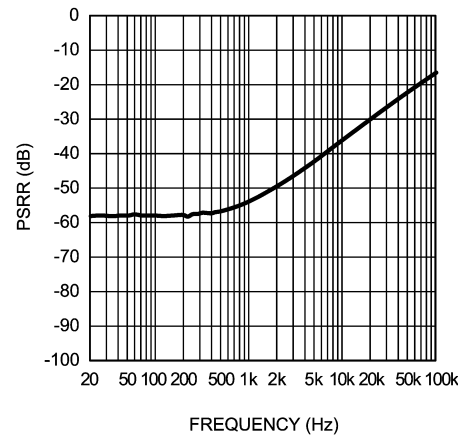
201341D3

**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , MICBIAS = 2.5V



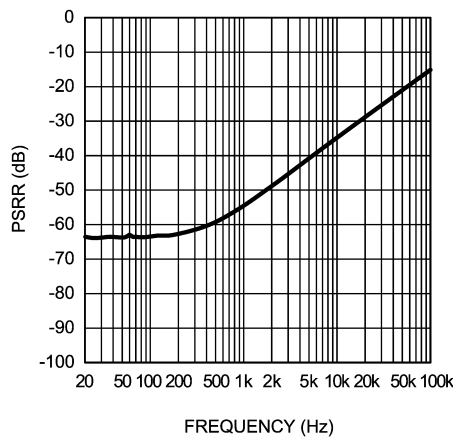
201341D4

**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 5V$ , MICBIAS = 2.5V



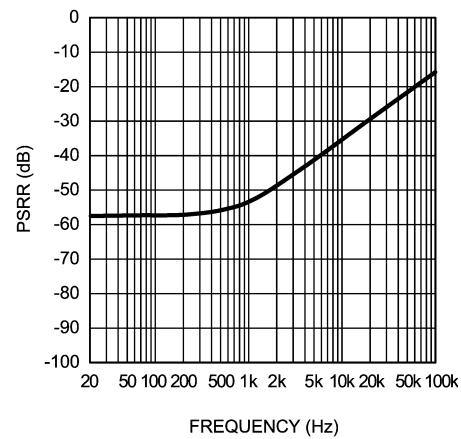
201341D5

**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 3.3V$ , MICBIAS = 2.8V



201341D6

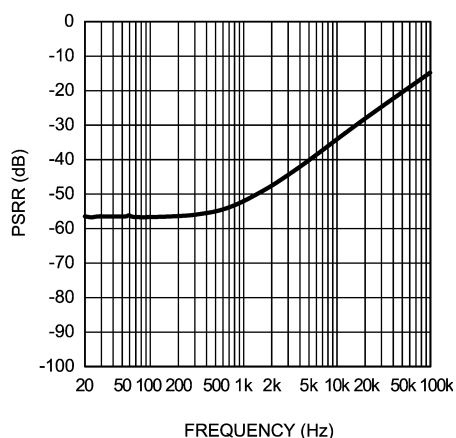
**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 5V$ , MICBIAS = 2.8V



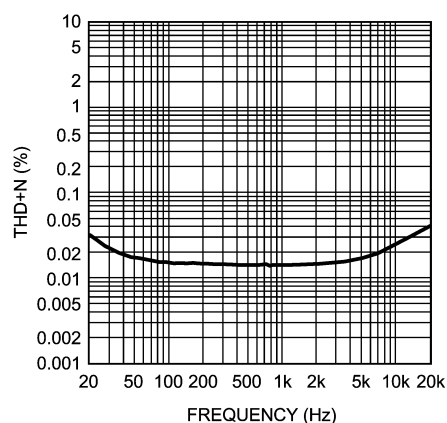
201341D7

# 13.0 Typical Performance Characteristics (Continued)

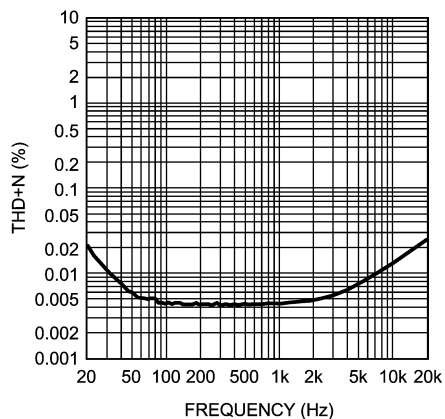
**INT/EXT MICBIAS PSRR vs Frequency**  
 $AV_{DD} = 5V$ , MICBIAS = 3.3V



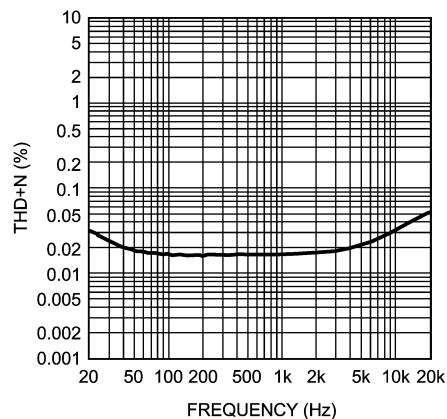
**AUXOUT THD+N vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB,  $V_{OUT} = 1V_{RMS}$ , 5k $\Omega$



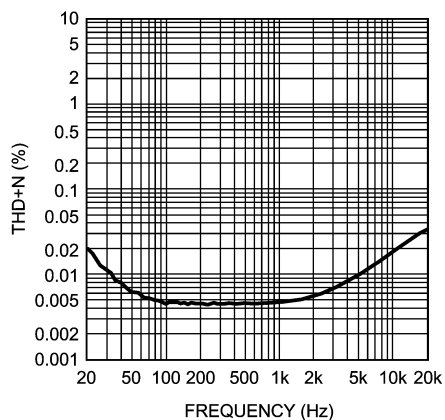
**AUXOUT THD+N vs Frequency**  
 $AV_{DD} = 5V$ , 0dB,  $V_{OUT} = 1V_{RMS}$ , 5k $\Omega$



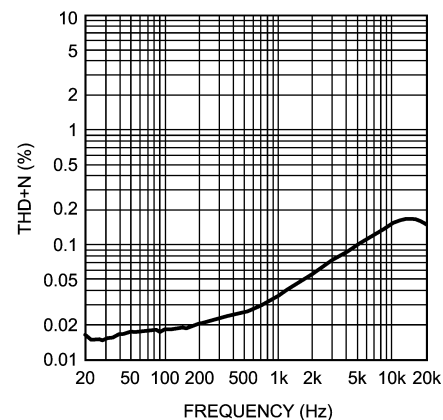
**CPOUT THD+N vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB,  $V_{OUT} = 1V_{RMS}$ , 5k $\Omega$



**CPOUT THD+N vs Frequency**  
 $AV_{DD} = 5V$ , 0dB,  $V_{OUT} = 1V_{RMS}$ , 5k $\Omega$

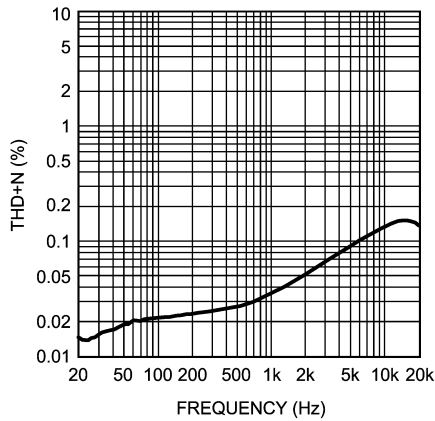


**Earpiece THD+N vs Frequency**  
 $AV_{DD} = 3.3V$ , 0dB,  $P_{OUT} = 500mW$ , 32 $\Omega$



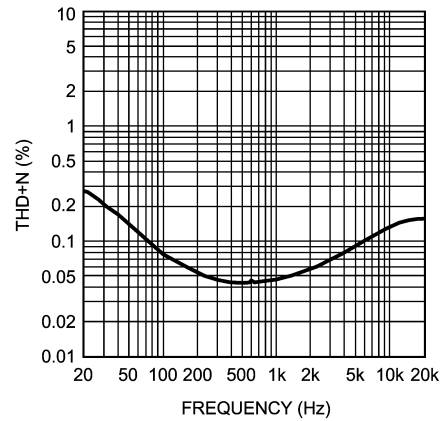
# 13.0 Typical Performance Characteristics (Continued)

**Earpiece THD+N vs Frequency**  
 $AV_{DD} = 5V$ , 0dB,  $P_{OUT} = 50mW$ ,  $32\Omega$



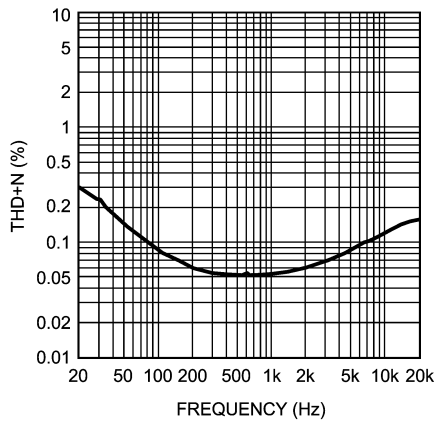
201341E4

**Headphone THD+N vs Frequency**  
 $AV_{DD} = 3.3V$ , OCL 1.5V, 0dB  
 $P_{OUT} = 7.5mW$ ,  $32\Omega$



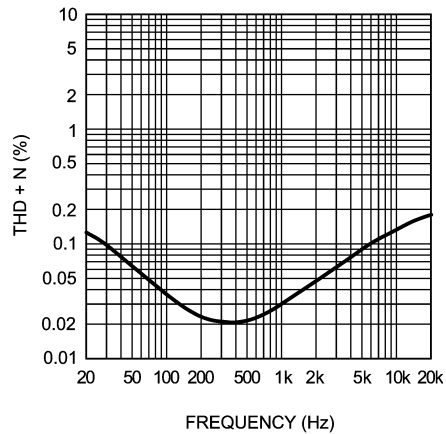
201341E5

**Headphone THD+N vs Frequency**  
 $AV_{DD} = 5V$ , OCL 1.5V, 0dB  
 $P_{OUT} = 10mW$ ,  $32\Omega$



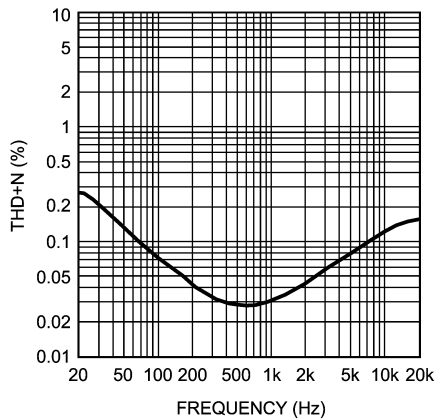
201341E6

**Headphone THD+N vs Frequency**  
 $AV_{DD} = 3.3V$ , OCL 1.2V, 0dB  
 $P_{OUT} = 7.5mW$ ,  $32\Omega$



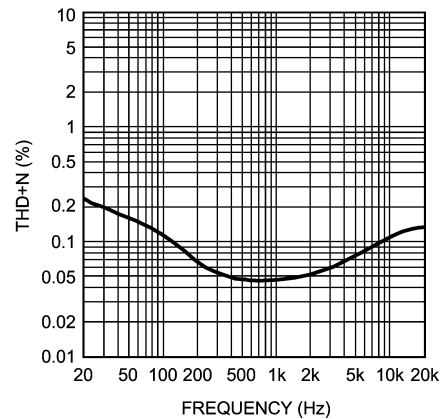
201341N1

**Headphone THD+N vs Frequency**  
 $AV_{DD} = 5V$ , OCL 1.2V, 0dB  
 $P_{OUT} = 10mW$ ,  $32\Omega$



201341E7

**Headphone THD+N vs Frequency**  
 $AV_{DD} = 3.3V$ , SE, 0dB  
 $P_{OUT} = 7.5mW$ ,  $32\Omega$



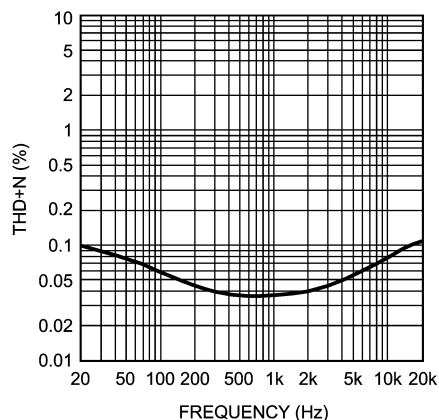
201341E8



# 13.0 Typical Performance Characteristics (Continued)

## Headphone THD+N vs Frequency

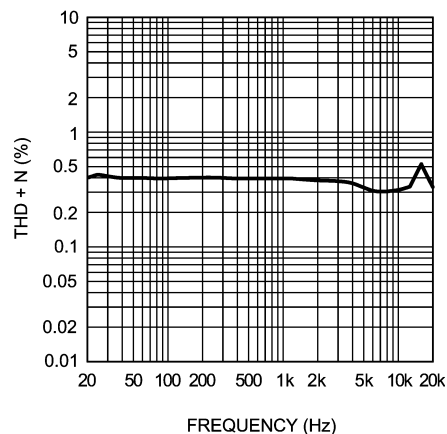
$AV_{DD} = 5V$ , SE, 0dB  
 $P_{OUT} = 10mW$ ,  $32\Omega$



201341E9

## Loudspeaker THD+N vs Frequency

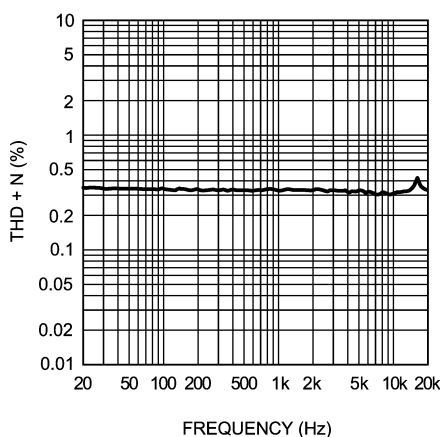
$AV_{DD} = 3.3V$ ,  $P_{OUT} = 400mW$   
 $15\mu H + 8\Omega + 15\mu H$



201341O2

## Loudspeaker THD+N vs Frequency

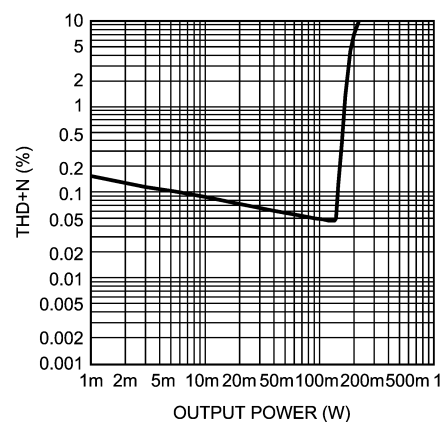
$AV_{DD} = 5V$ ,  $P_{OUT} = 400mW$   
 $15\mu H + 8\Omega + 15\mu H$



201341O3

## Earpiece THD+N vs Output Power

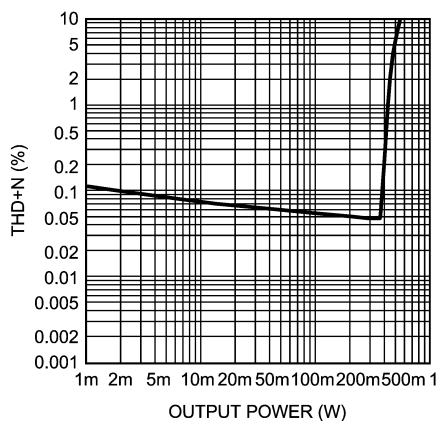
$AV_{DD} = 3.3V$ , 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341F0

## Earpiece THD+N vs Output Power

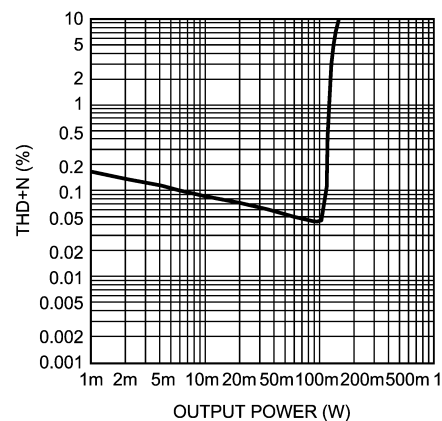
$AV_{DD} = 5V$ , 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341F1

## Earpiece THD+N vs Output Power

$AV_{DD} = 3.3V$ , 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



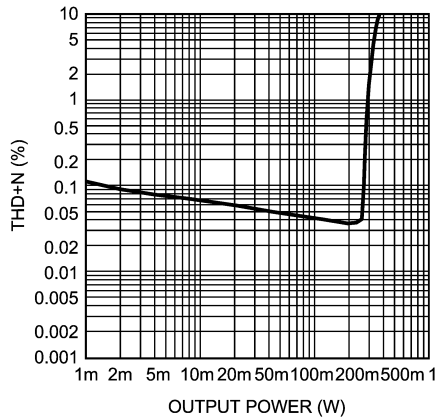
201341F2

# 13.0 Typical Performance Characteristics (Continued)

**Earpiece THD+N vs Output Power**

$AV_{DD} = 5V$ , 0dB AUX

$f_{OUT} = 1kHz$ ,  $32\Omega$

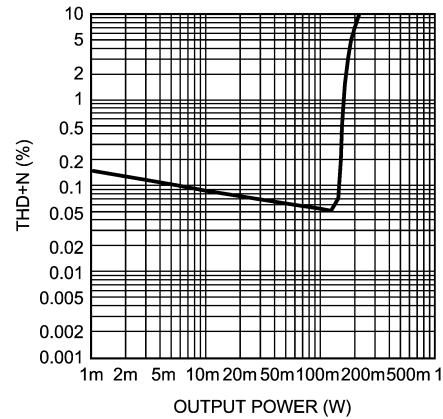


201341F3

**Earpiece THD+N vs Output Power**

$AV_{DD} = 3.3V$ , 0dB CPI

$f_{OUT} = 1kHz$ ,  $16\Omega$

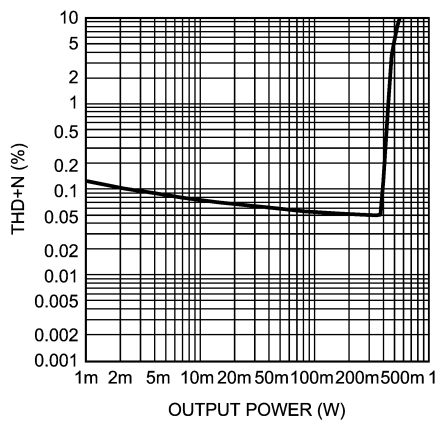


201341F4

**Earpiece THD+N vs Output Power**

$AV_{DD} = 5V$ , 0dB CPI

$f_{OUT} = 1kHz$ ,  $16\Omega$

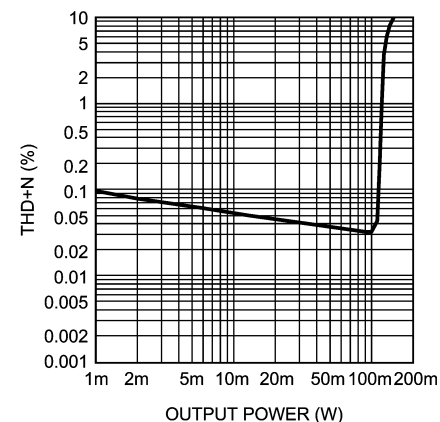


201341F5

**Earpiece THD+N vs Output Power**

$AV_{DD} = 3.3V$ , 0dB CPI

$f_{OUT} = 1kHz$ ,  $32\Omega$

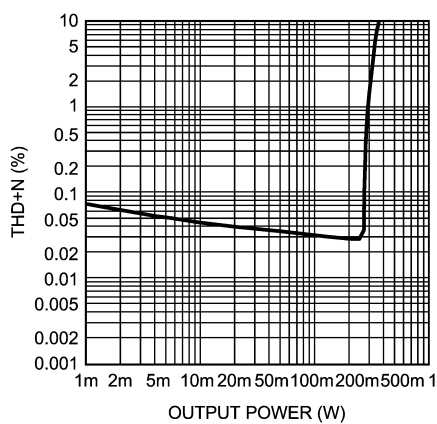


201341F6

**Earpiece THD+N vs Output Power**

$AV_{DD} = 5V$ , 0dB CPI

$f_{OUT} = 1kHz$ ,  $32\Omega$

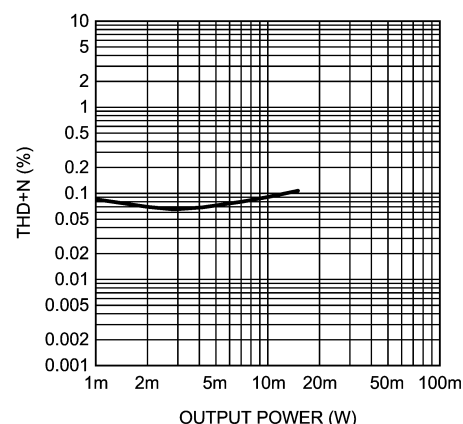


201341F7

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.2V, 0dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$



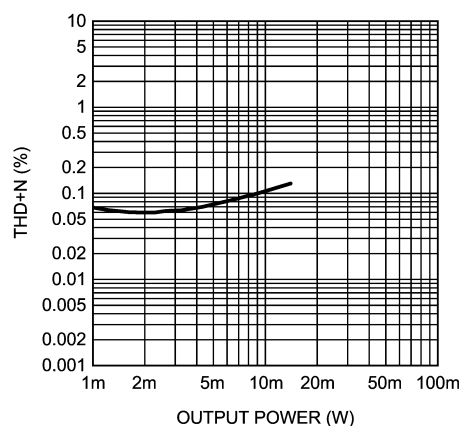
201341F8

## 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , OCL 1.2V, 0dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$

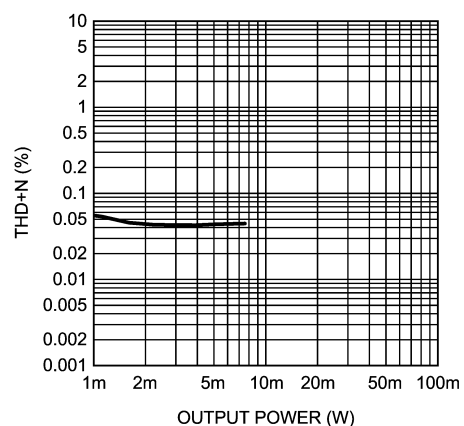


201341F9

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.2V, 0dB DAC

$f_{OUT} = 1kHz$ ,  $32\Omega$

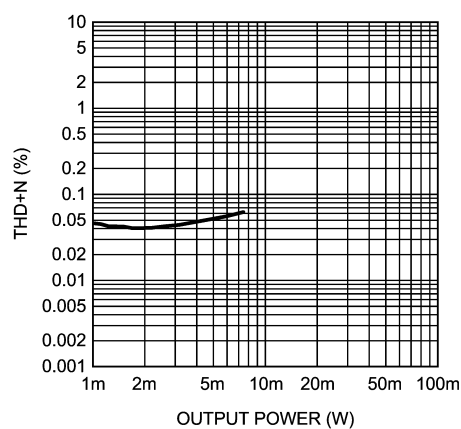


201341G0

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , OCL 1.2V, 0dB DAC

$f_{OUT} = 1kHz$ ,  $32\Omega$

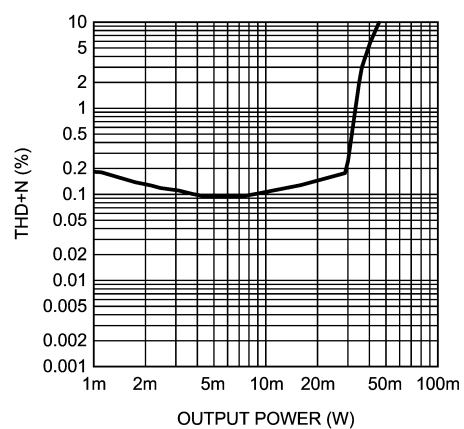


201341G1

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.2V, 12dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$

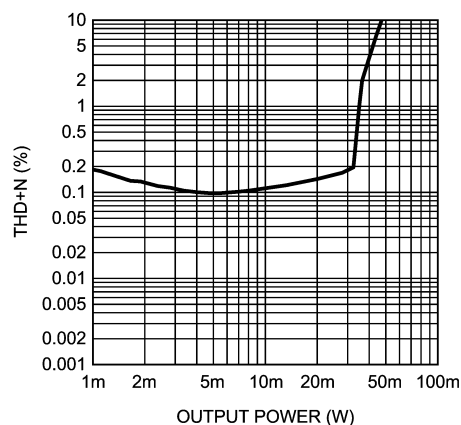


201341G2

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , OCL 1.2V, 12dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$

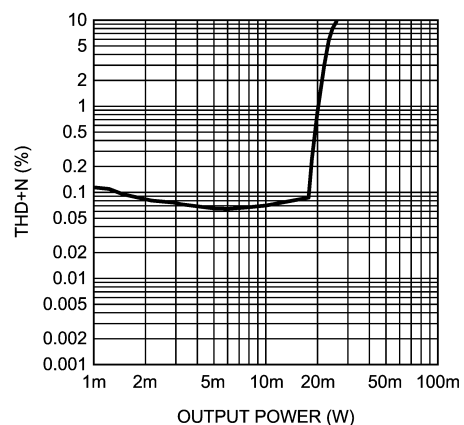


201341G3

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.2V, 12dB DAC

$f_{OUT} = 1kHz$ ,  $32\Omega$

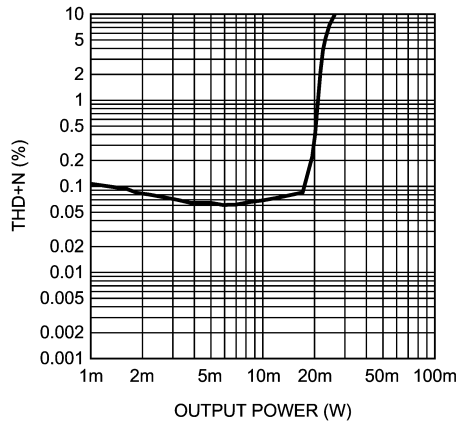


201341G4

# 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**

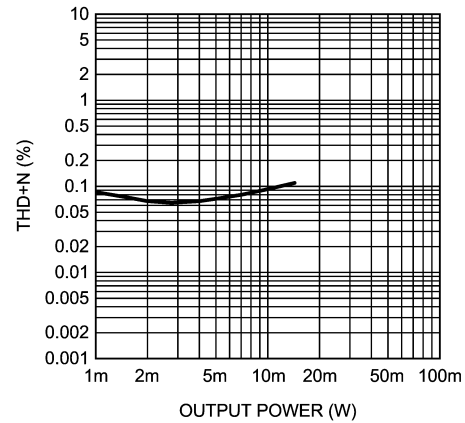
$AV_{DD} = 5V$ , OCL 1.2V, 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341G5

**Headphone THD+N vs Output Power**

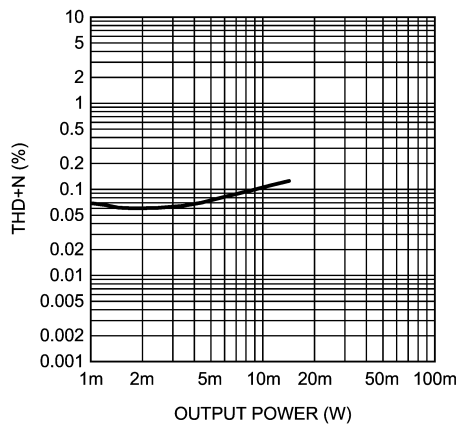
$AV_{DD} = 3.3V$ , OCL 1.5V, 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341G6

**Headphone THD+N vs Output Power**

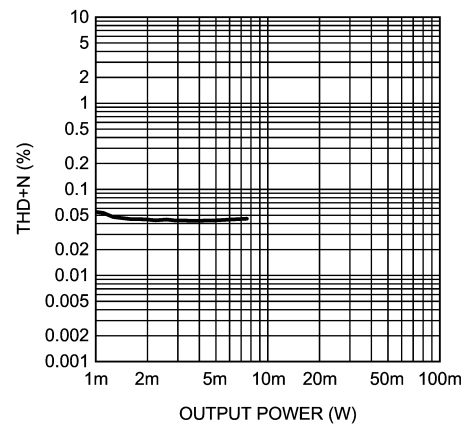
$AV_{DD} = 5V$ , OCL 1.5V, 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341G7

**Headphone THD+N vs Output Power**

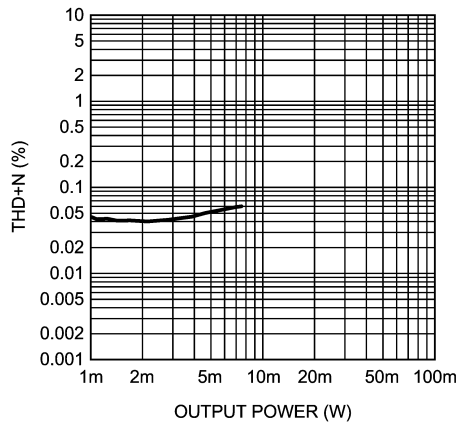
$AV_{DD} = 3.3V$ , OCL 1.5V, 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341G8

**Headphone THD+N vs Output Power**

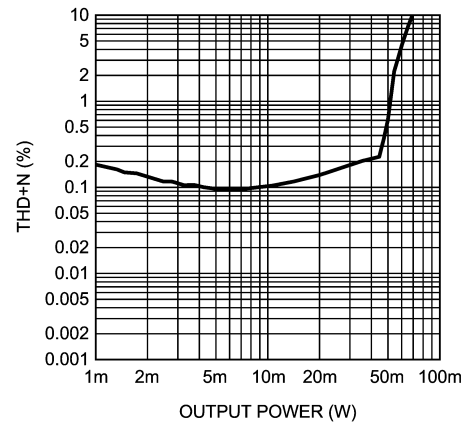
$AV_{DD} = 5V$ , OCL 1.5V, 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341G9

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.5V, 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



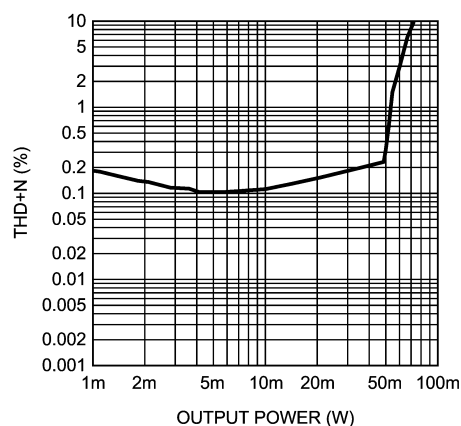
201341H0

# 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , OCL 1.5V, 12dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$

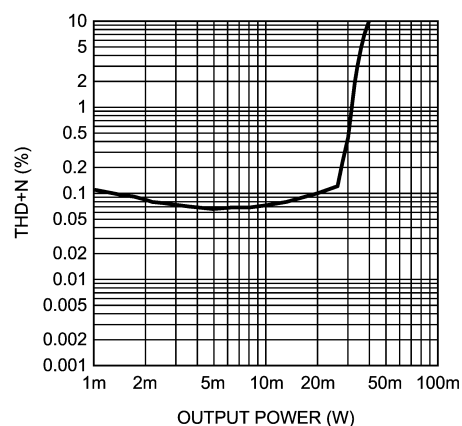


201341H1

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.5V, 12dB DAC

$f_{OUT} = 1kHz$ ,  $32\Omega$

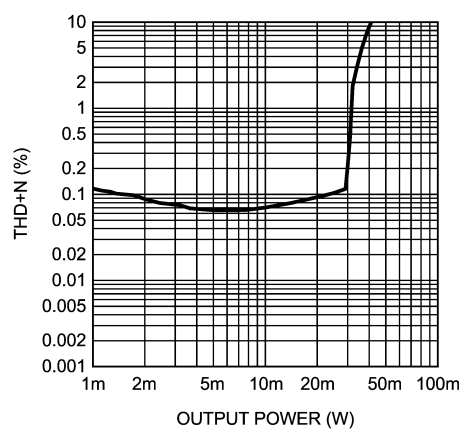


201341H2

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , OCL 1.5V, 12dB DAC

$f_{OUT} = 1kHz$ ,  $32\Omega$

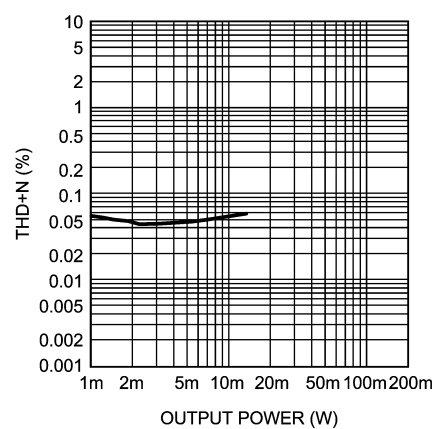


201341H3

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , SE, 0dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$

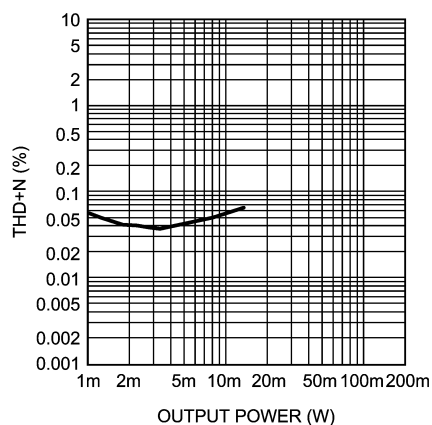


201341H4

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , SE, 0dB DAC

$f_{OUT} = 1kHz$ ,  $16\Omega$

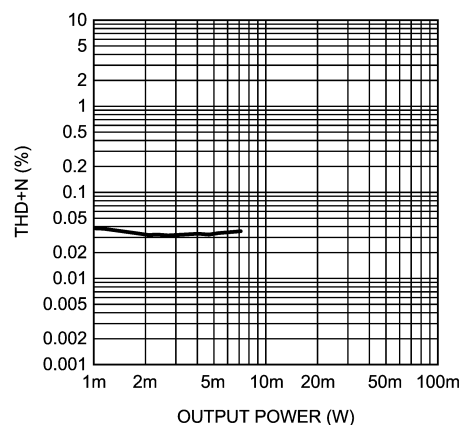


201341H5

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , SE, 0dB DAC

$f_{OUT} = 1kHz$ ,  $32\Omega$

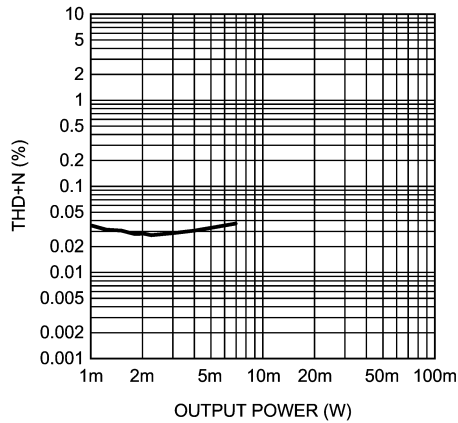


201341H6

# 13.0 Typical Performance Characteristics (Continued)

Headphone THD+N vs Output Power

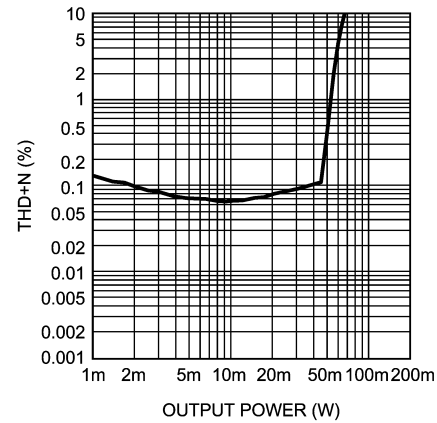
$AV_{DD} = 5V$ , SE, 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341H7

Headphone THD+N vs Output Power

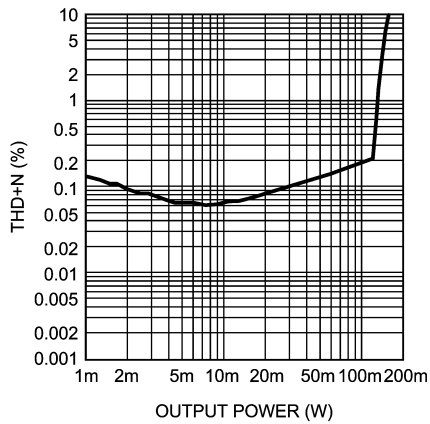
$AV_{DD} = 3.3V$ , SE, 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341H8

Headphone THD+N vs Output Power

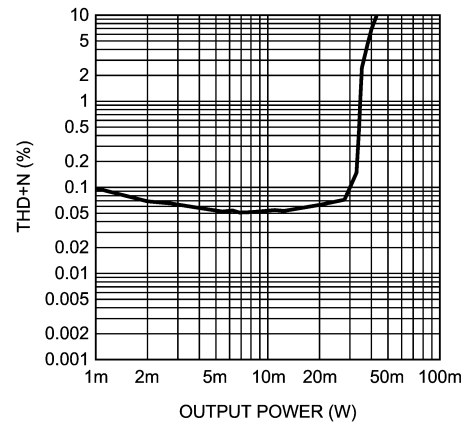
$AV_{DD} = 5V$ , SE, 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341H9

Headphone THD+N vs Output Power

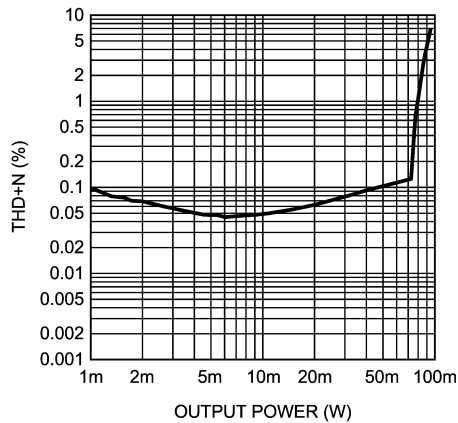
$AV_{DD} = 3.3V$ , SE, 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341I0

Headphone THD+N vs Output Power

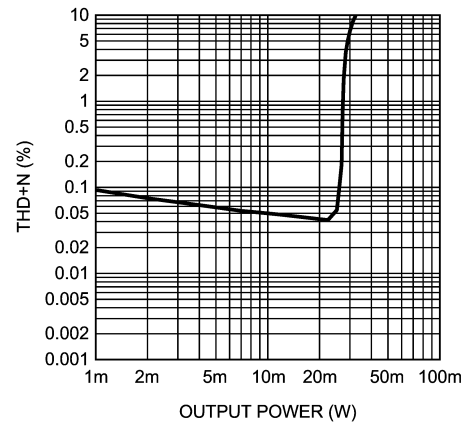
$AV_{DD} = 5V$ , SE, 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341I1

Headphone THD+N vs Output Power

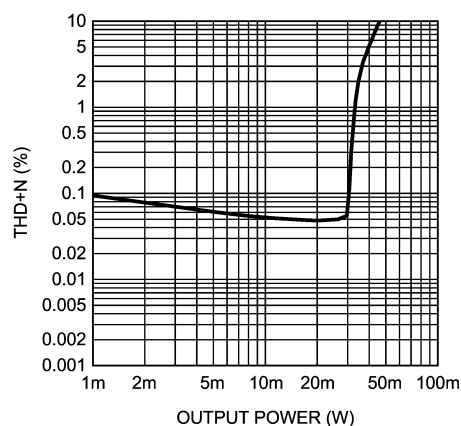
$AV_{DD} = 3.3V$ , OCL 1.2V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341I2

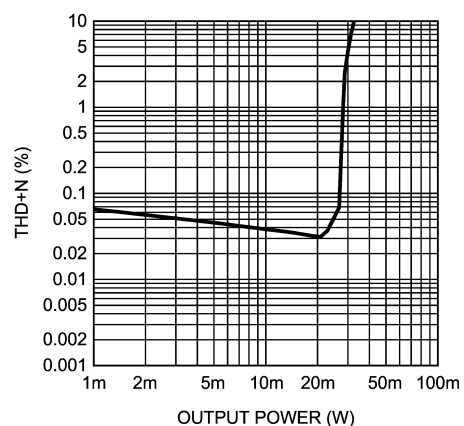
## 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , OCL 1.2V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



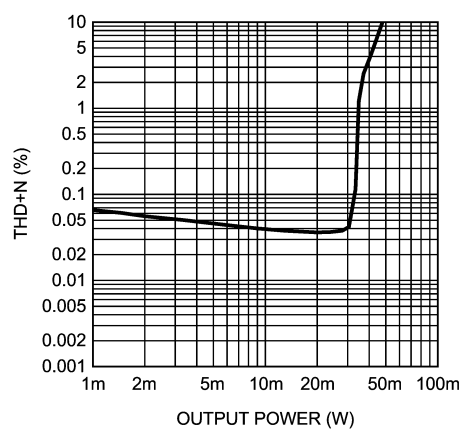
20134113

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 5V$ , OCL 1.2V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



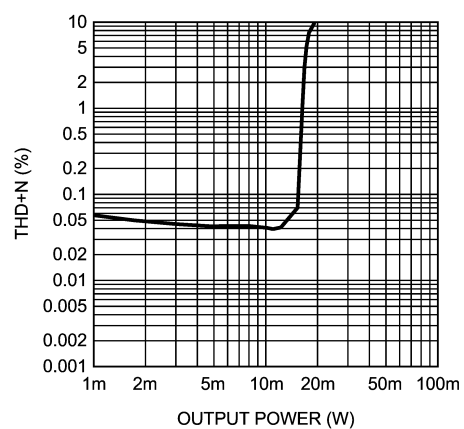
20134114

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 5V$ , OCL 1.2V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



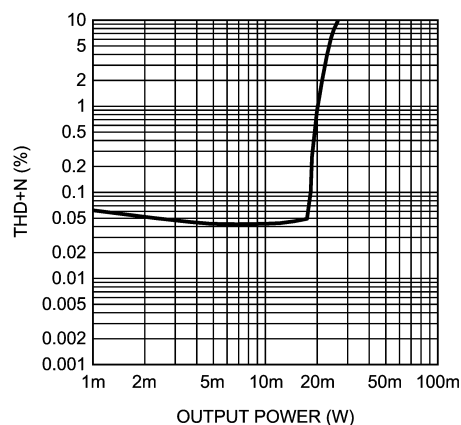
20134115

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , OCL 1.2V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



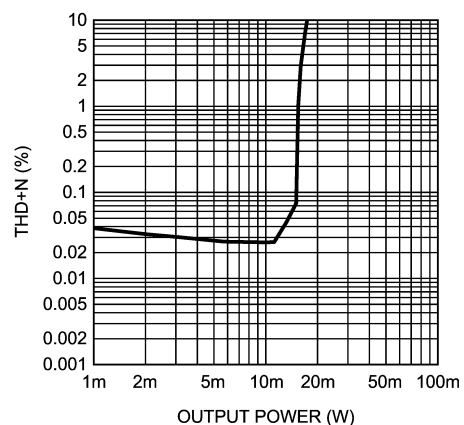
20134116

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , OCL 1.2V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



20134117

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 5V$ , OCL 1.2V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$

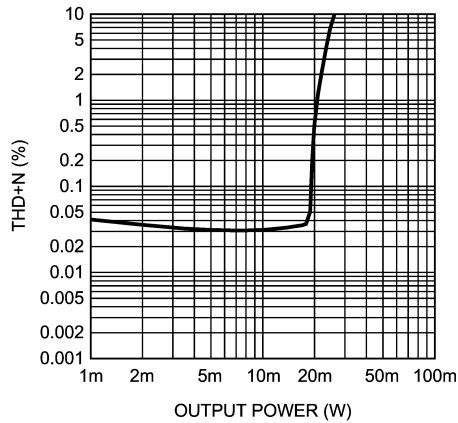


20134118

# 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**

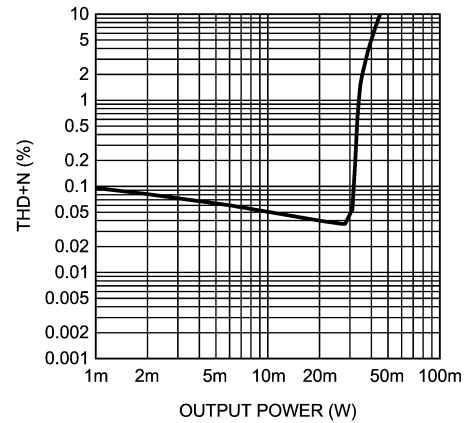
$AV_{DD} = 5V$ , OCL 1.2V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341I9

**Headphone THD+N vs Output Power**

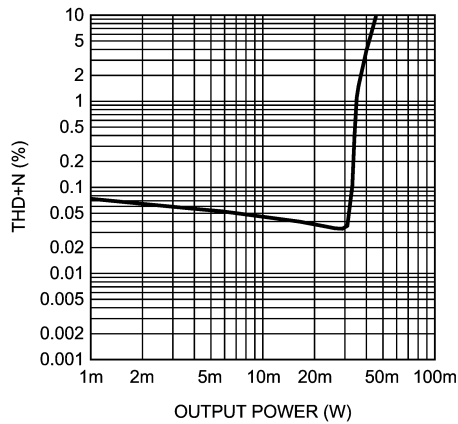
$AV_{DD} = 3.3V$ , OCL 1.2V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341J0

**Headphone THD+N vs Output Power**

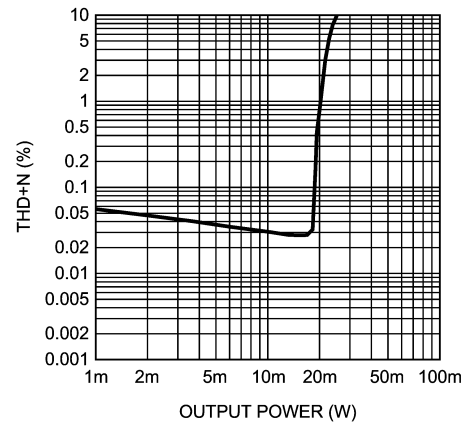
$AV_{DD} = 5V$ , OCL 1.2V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341J1

**Headphone THD+N vs Output Power**

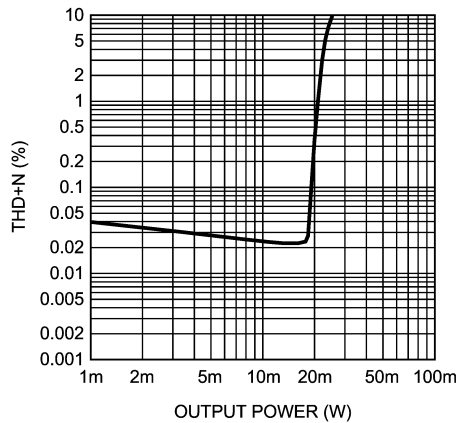
$AV_{DD} = 3.3V$ , OCL 1.2V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341J2

**Headphone THD+N vs Output Power**

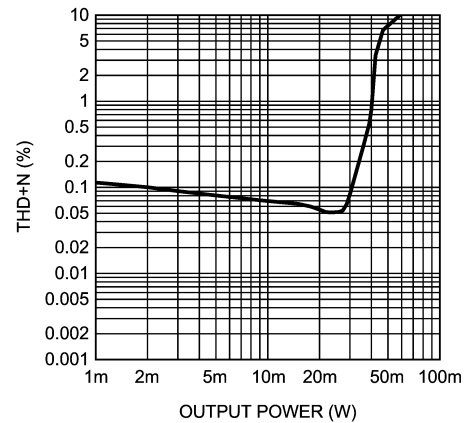
$AV_{DD} = 5V$ , OCL 1.2V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341J3

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , OCL 1.5V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$

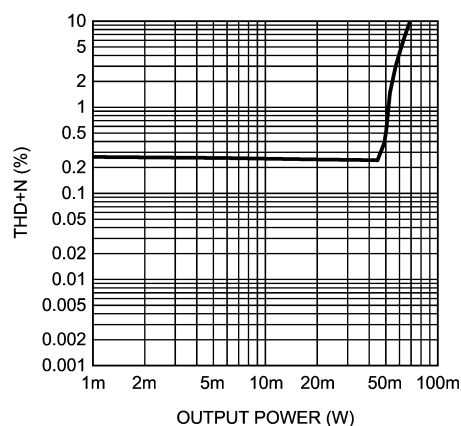


201341J4



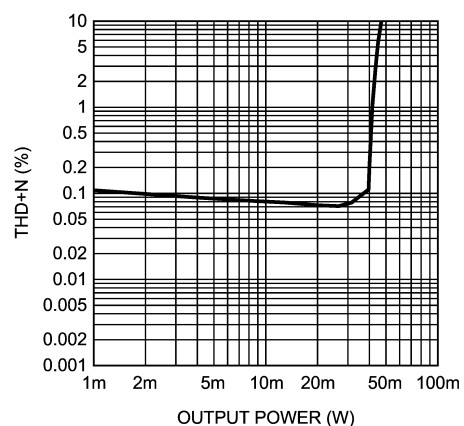
## 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , OCL 1.5V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



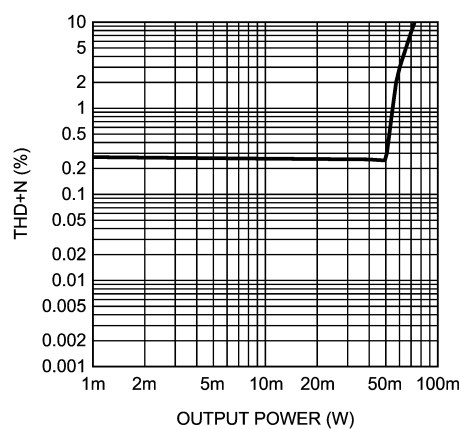
201341J5

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 5V$ , OCL 1.5V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



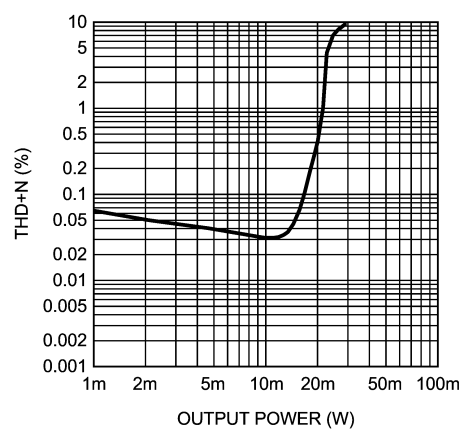
201341J6

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 5V$ , OCL 1.5V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



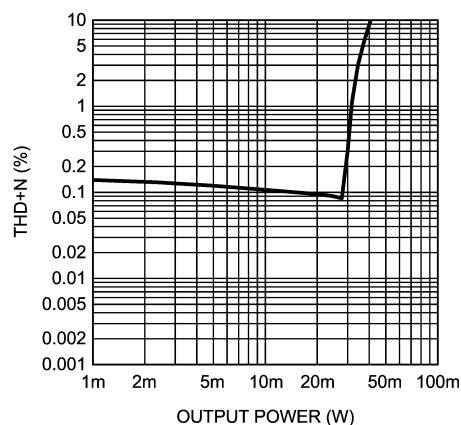
201341J7

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , OCL 1.5V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



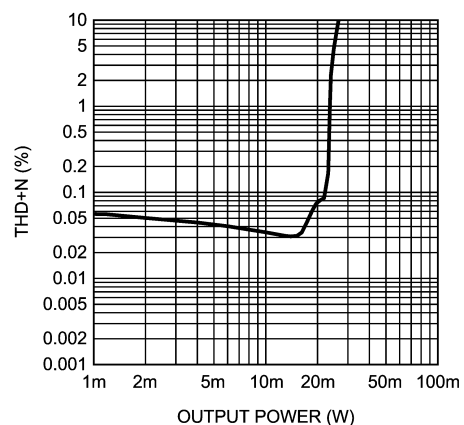
201341J8

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , OCL 1.5V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341J9

**Headphone THD+N vs Output Power**  
 $AV_{DD} = 5V$ , OCL 1.5V, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$

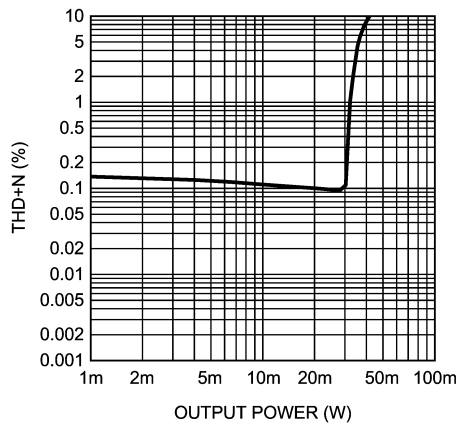


201341K0

# 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**

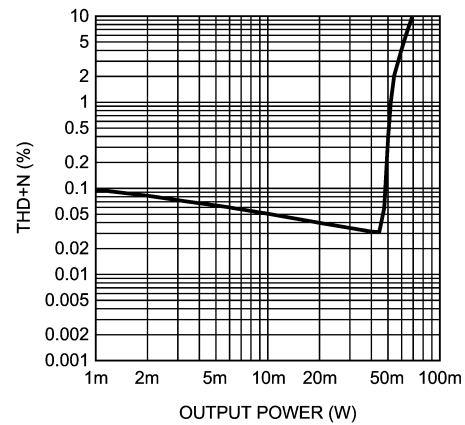
$AV_{DD} = 5V$ , OCL 1.5V, 12dB AUX  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341K1

**Headphone THD+N vs Output Power**

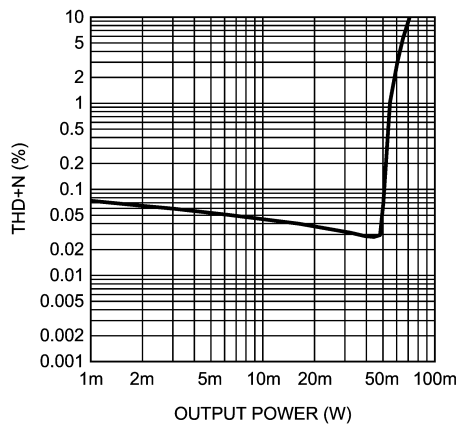
$AV_{DD} = 3.3V$ , OCL 1.5V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341K2

**Headphone THD+N vs Output Power**

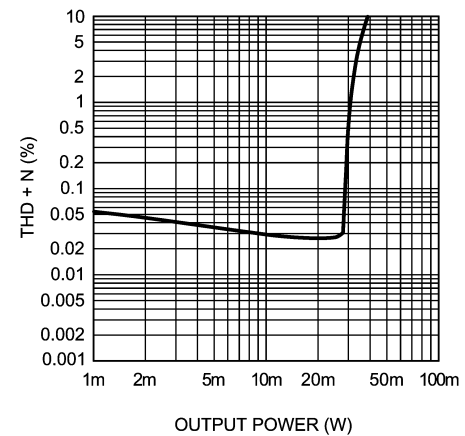
$AV_{DD} = 5V$ , OCL 1.5V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



201341K3

**Headphone THD+N vs Output Power**

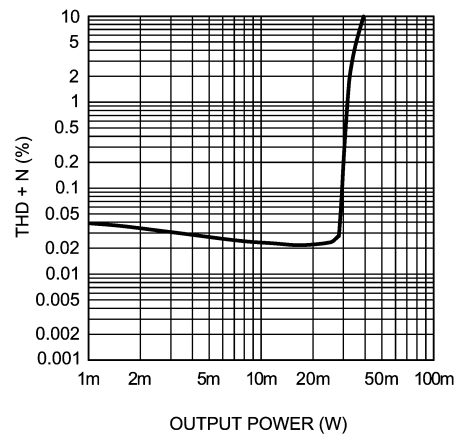
$AV_{DD} = 3.3V$ , OCL 1.5V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341N2

**Headphone THD+N vs Output Power**

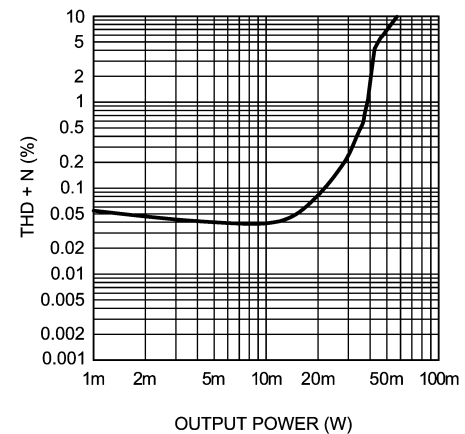
$AV_{DD} = 5V$ , OCL 1.5V, 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $32\Omega$



201341N3

**Headphone THD+N vs Output Power**

$AV_{DD} = 3.3V$ , SE, 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $16\Omega$



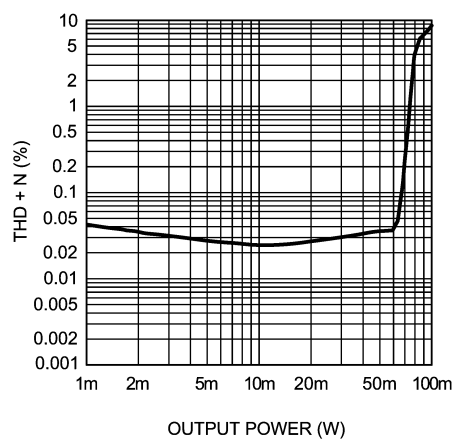
201341N4

# 13.0 Typical Performance Characteristics (Continued)

Headphone THD+N vs Output Power

$AV_{DD} = 5V$ , SE, 0dB AUX

$f_{OUT} = 1kHz$ ,  $16\Omega$

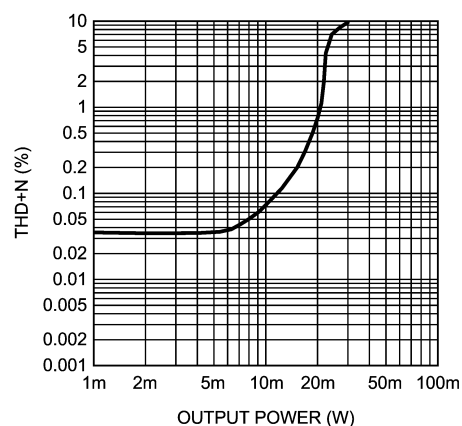


201341N5

Headphone THD+N vs Output Power

$AV_{DD} = 3.3V$ , SE, 0dB AUX

$f_{OUT} = 1kHz$ ,  $32\Omega$

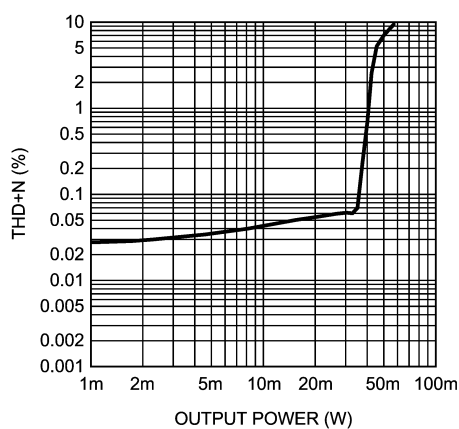


201341K4

Headphone THD+N vs Output Power

$AV_{DD} = 5V$ , SE, 0dB AUX

$f_{OUT} = 1kHz$ ,  $32\Omega$

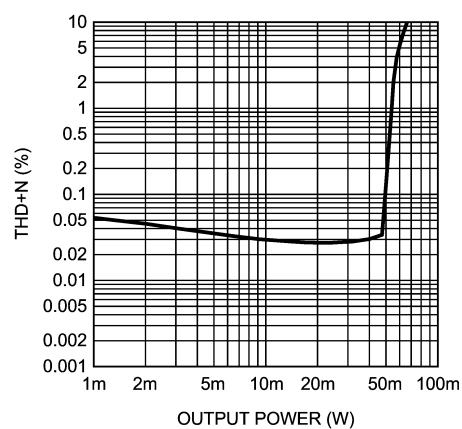


201341K5

Headphone THD+N vs Output Power

$AV_{DD} = 3.3V$ , SE, 0dB CPI

$f_{OUT} = 1kHz$ ,  $16\Omega$

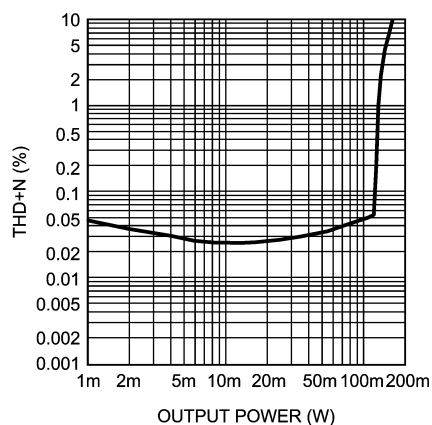


201341K6

Headphone THD+N vs Output Power

$AV_{DD} = 5V$ , SE, 0dB CPI

$f_{OUT} = 1kHz$ ,  $16\Omega$

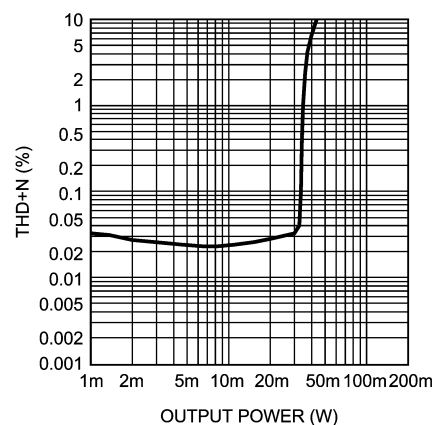


201341K7

Headphone THD+N vs Output Power

$AV_{DD} = 3.3V$ , SE, 0dB CPI

$f_{OUT} = 1kHz$ ,  $32\Omega$



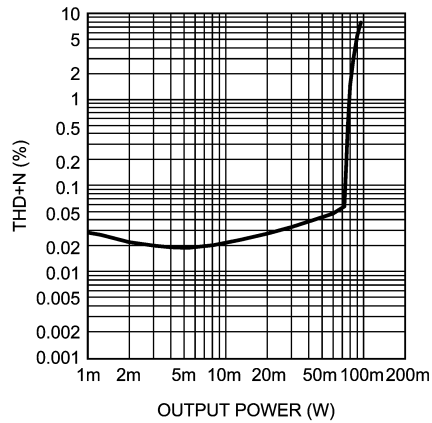
201341K8

# 13.0 Typical Performance Characteristics (Continued)

**Headphone THD+N vs Output Power**

$AV_{DD} = 5V$ , SE, 0dB CPI

$f_{OUT} = 1kHz$ ,  $32\Omega$

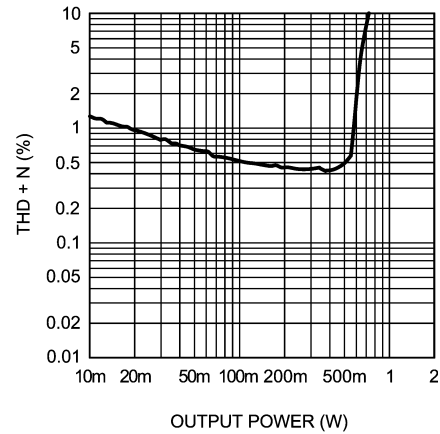


201341K9

**Loudspeaker THD+N vs Output Power**

$AV_{DD} = 3.3V$ , 0dB AUX

$f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$

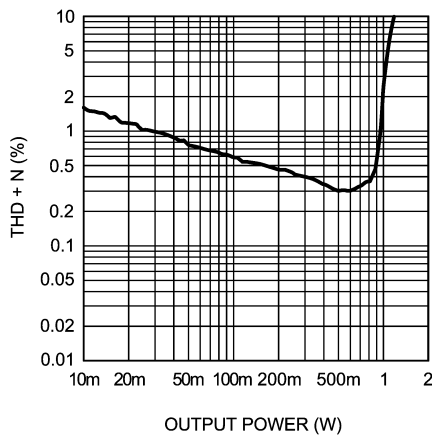


201341O4

**Loudspeaker THD+N vs Output Power**

$AV_{DD} = 4.2V$ , 0dB AUX

$f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$

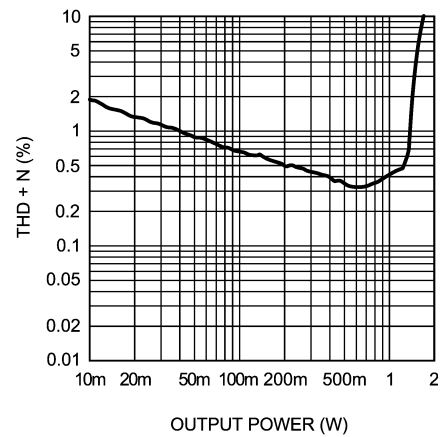


201341O5

**Loudspeaker THD+N vs Output Power**

$AV_{DD} = 5V$ , 0dB AUX

$f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$

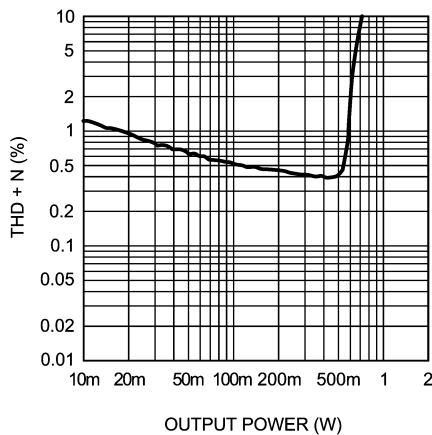


201341O6

**Loudspeaker THD+N vs Output Power**

$AV_{DD} = 3.3V$ , 0dB CPI

$f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$

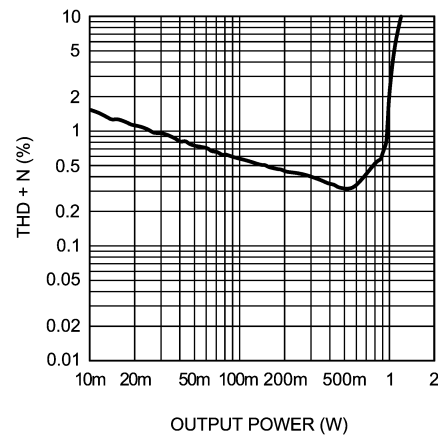


201341O7

**Loudspeaker THD+N vs Output Power**

$AV_{DD} = 4.2V$ , 0dB CPI

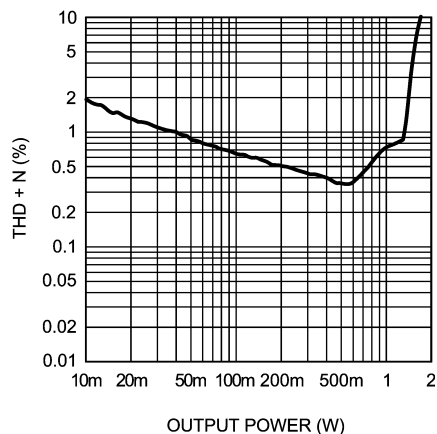
$f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$



201341O8

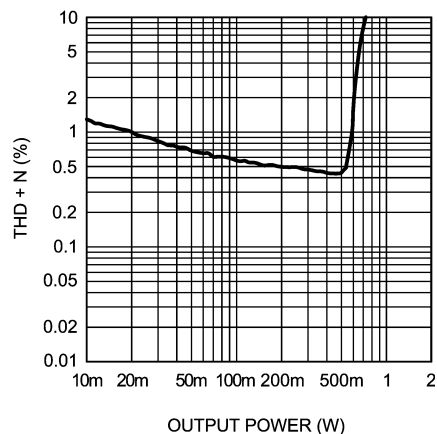
# 13.0 Typical Performance Characteristics (Continued)

**Loudspeaker THD+N vs Output Power**  
 $AV_{DD} = 5V$ , 0dB CPI  
 $f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$



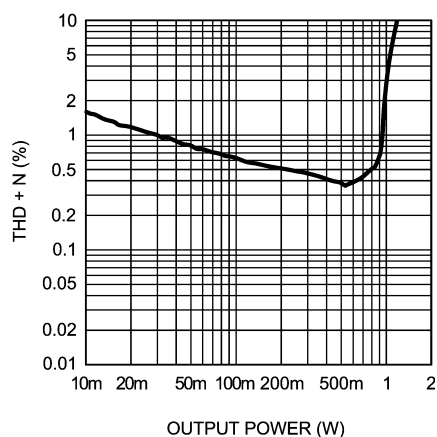
201341O9

**Loudspeaker THD+N vs Output Power**  
 $AV_{DD} = 3.3V$ , 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$



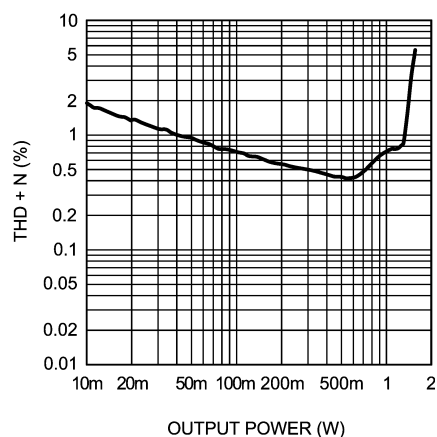
201341P0

**Loudspeaker THD+N vs Output Power**  
 $AV_{DD} = 4.2V$ , 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$



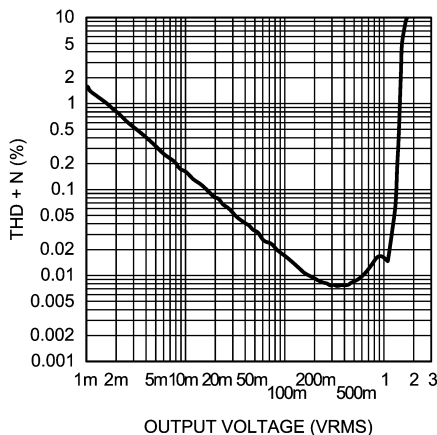
201341P1

**Loudspeaker THD+N vs Output Power**  
 $AV_{DD} = 5V$ , 0dB DAC  
 $f_{OUT} = 1kHz$ ,  $15\mu H + 8\Omega + 15\mu H$



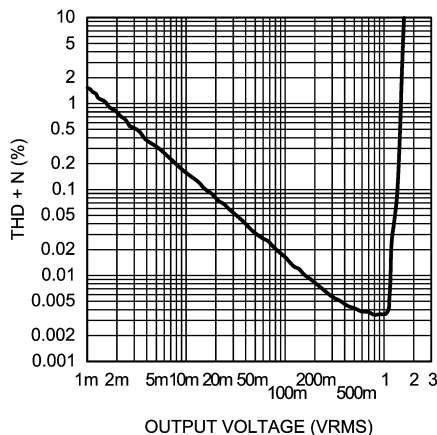
201341P2

**AUXOUT THD+N vs Output Voltage**  
 $AV_{DD} = 3.3V$ , 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $5k\Omega$



201341L0

**AUXOUT THD+N vs Output Voltage**  
 $AV_{DD} = 5V$ , 0dB AUX  
 $f_{OUT} = 1kHz$ ,  $5k\Omega$



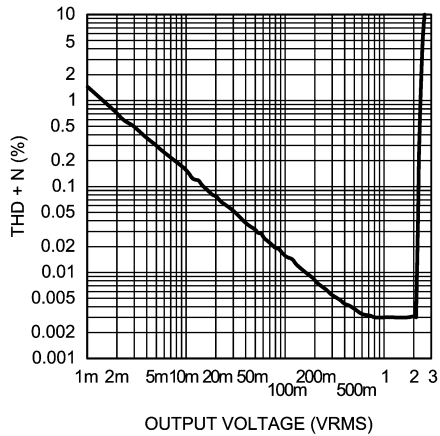
201341L1

# 13.0 Typical Performance Characteristics (Continued)

**AUXOUT THD+N vs Output Voltage**

$AV_{DD} = 3.3V$ , 0dB CPI

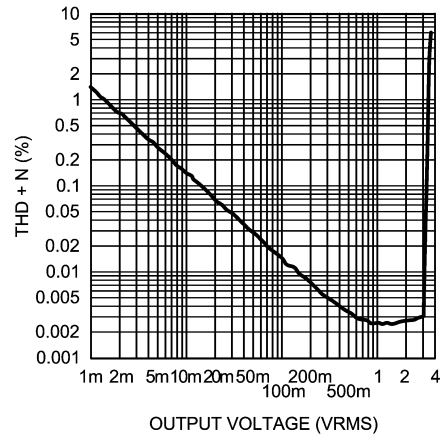
$f_{OUT} = 1kHz$ ,  $5k\Omega$



**AUXOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 0dB CPI

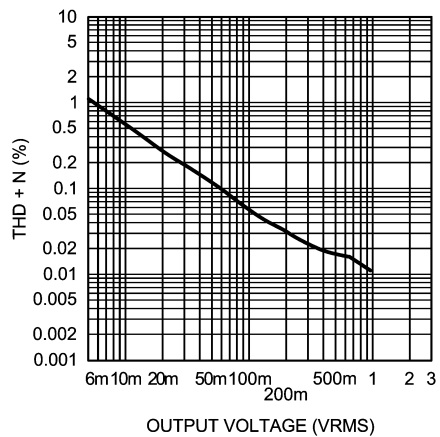
$f_{OUT} = 1kHz$ ,  $5k\Omega$



**AUXOUT THD+N vs Output Voltage**

$AV_{DD} = 3.3V$ , 0dB DAC

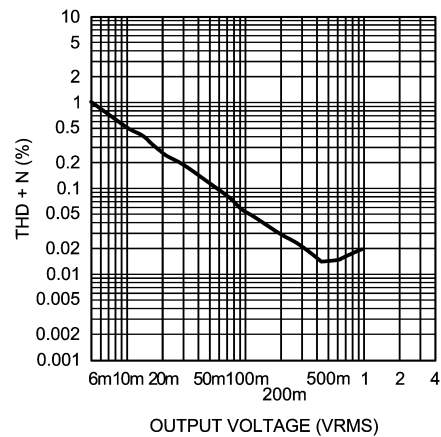
$f_{OUT} = 1kHz$ ,  $5k\Omega$



**AUXOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 0dB DAC

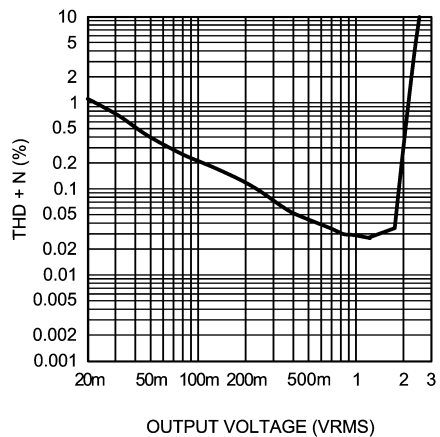
$f_{OUT} = 1kHz$ ,  $5k\Omega$



**AUXOUT THD+N vs Output Voltage**

$AV_{DD} = 3.3V$ , 12dB DAC

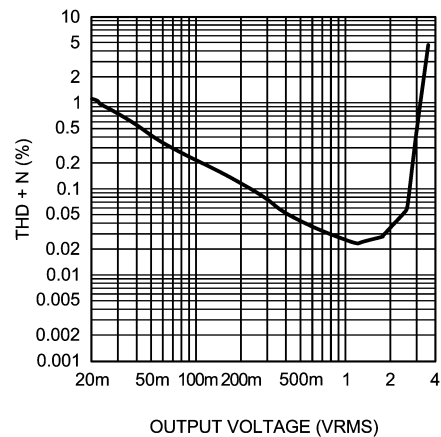
$f_{OUT} = 1kHz$ ,  $5k\Omega$



**AUXOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 12dB DAC

$f_{OUT} = 1kHz$ ,  $5k\Omega$

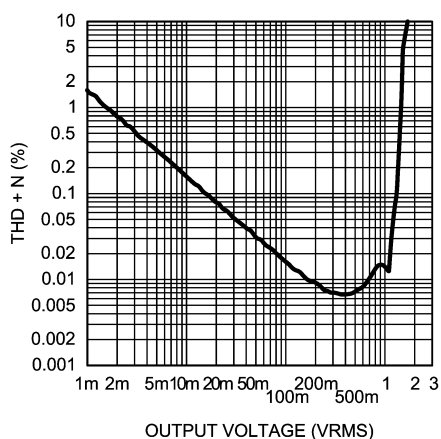


# 13.0 Typical Performance Characteristics (Continued)

**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 3.3V$ , 0dB AUX

$f_{OUT} = 1kHz$ ,  $5k\Omega$

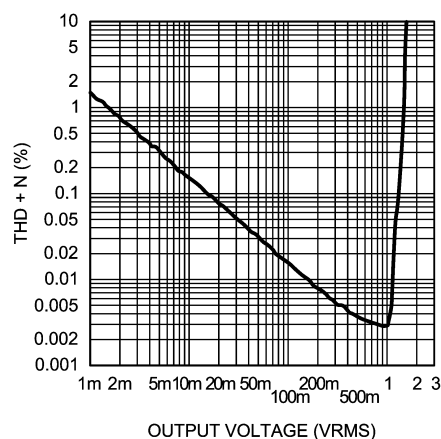


201341L8

**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 0dB AUX

$f_{OUT} = 1kHz$ ,  $5k\Omega$

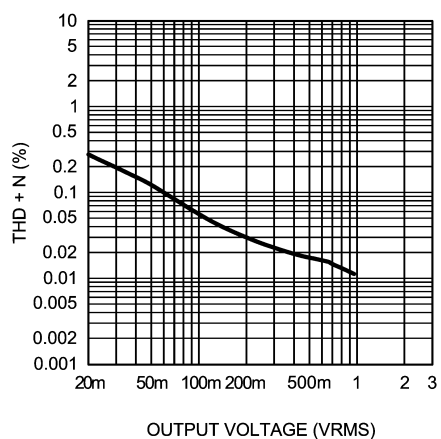


201341L9

**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 3.3V$ , 0dB DAC

$f_{OUT} = 1kHz$ ,  $5k\Omega$

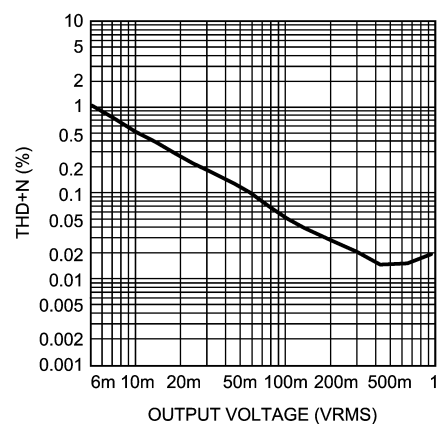


201341M0

**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 0dB DAC

$f_{OUT} = 1kHz$ ,  $5k\Omega$

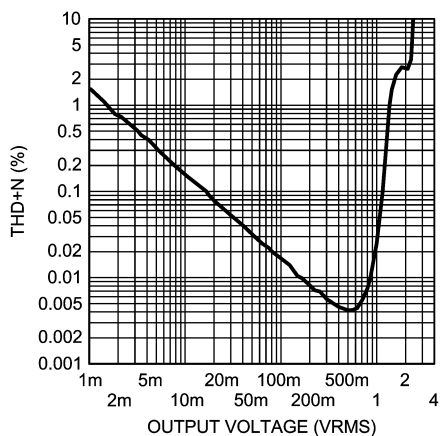


201341M1

**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 3.3V$ , 6dB MIC

$f_{OUT} = 1kHz$ ,  $5k\Omega$

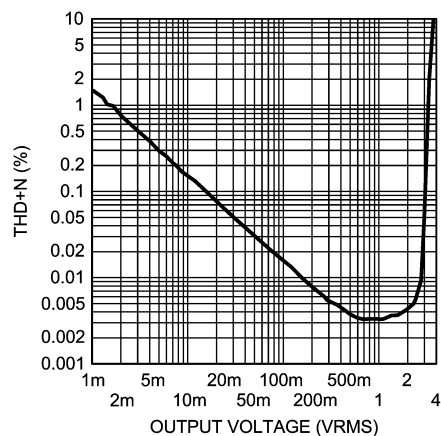


201341M2

**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 6dB MIC

$f_{OUT} = 1kHz$ ,  $5k\Omega$

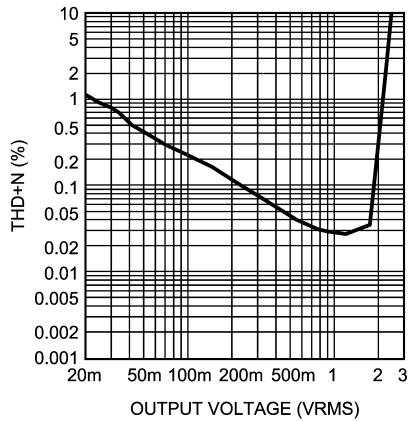


201341M3

# 13.0 Typical Performance Characteristics (Continued)

**CPOUT THD+N vs Output Voltage**

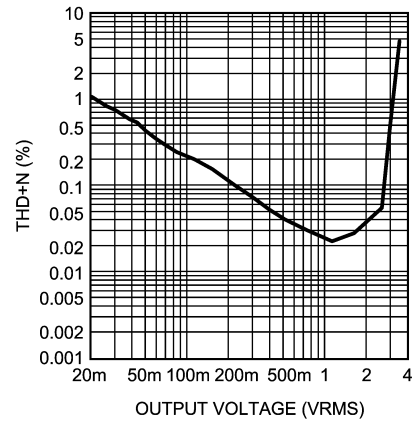
$AV_{DD} = 3.3V$ , 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $5k\Omega$



201341M4

**CPOUT THD+N vs Output Voltage**

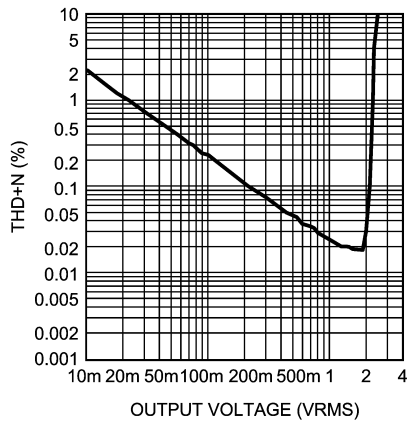
$AV_{DD} = 5V$ , 12dB DAC  
 $f_{OUT} = 1kHz$ ,  $5k\Omega$



201341M5

**CPOUT THD+N vs Output Voltage**

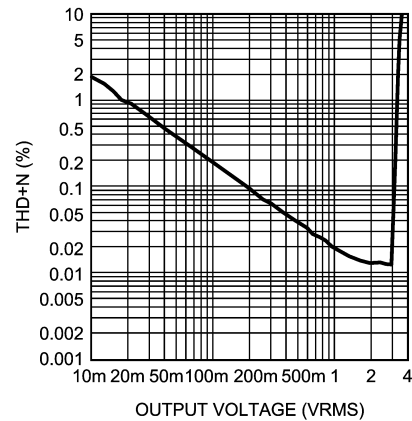
$AV_{DD} = 3.3V$ , 36dB MIC  
 $f_{OUT} = 1kHz$ ,  $5k\Omega$



201341M6

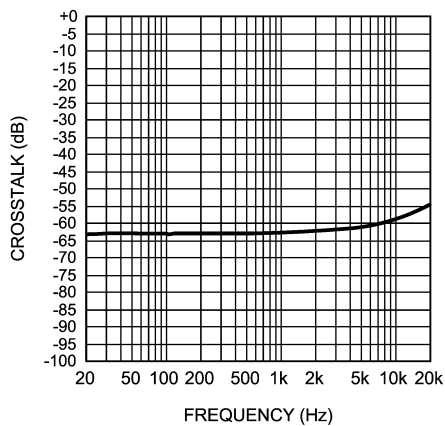
**CPOUT THD+N vs Output Voltage**

$AV_{DD} = 5V$ , 36dB MIC  
 $f_{OUT} = 1kHz$ ,  $5k\Omega$



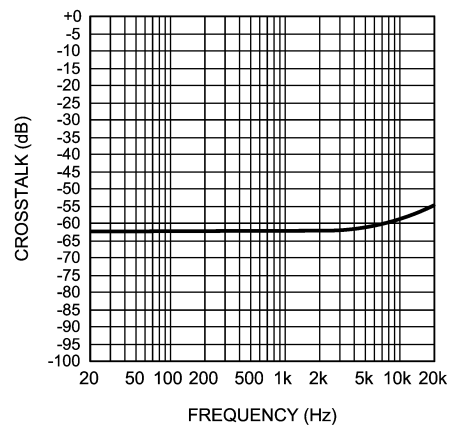
201341M7

**Headphone Crosstalk vs Frequency**  
 OCL 1.2V, 0dB AUX,  $32\Omega$



201341M8

**Headphone Crosstalk vs Frequency**  
 OCL 1.5V, 0dB AUX,  $32\Omega$

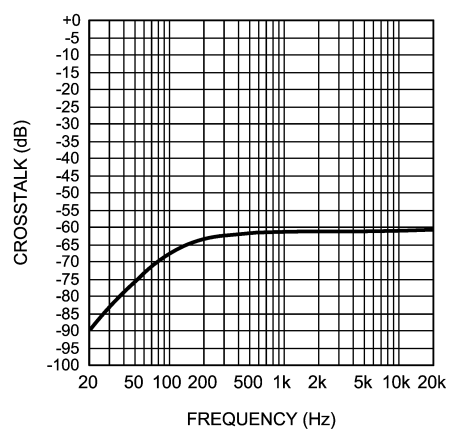


201341M9



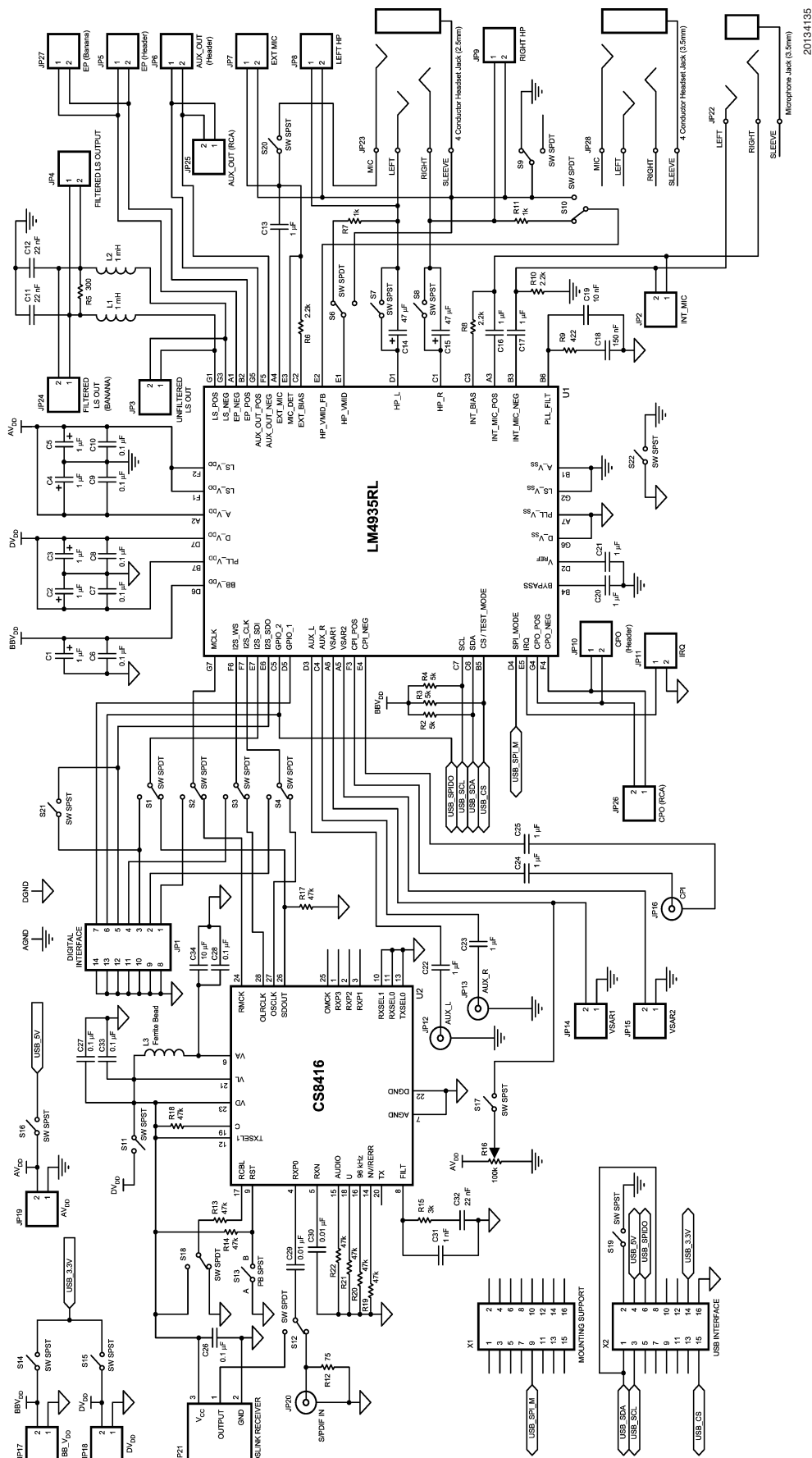
## 13.0 Typical Performance Characteristics (Continued)

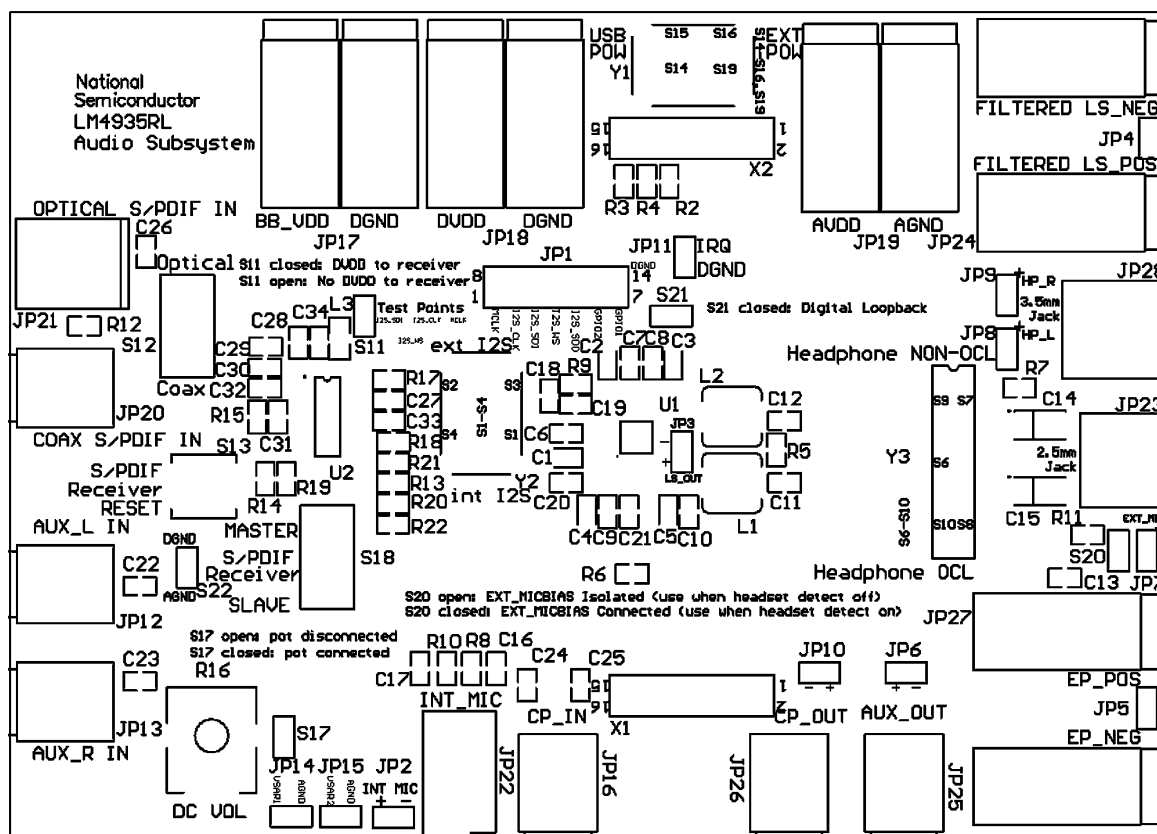
Headphone Crosstalk vs Frequency  
SE, 0dB AUX, 32 $\Omega$



201341N0

# 14.0 LM4935 Demonstration Board Schematic Diagram

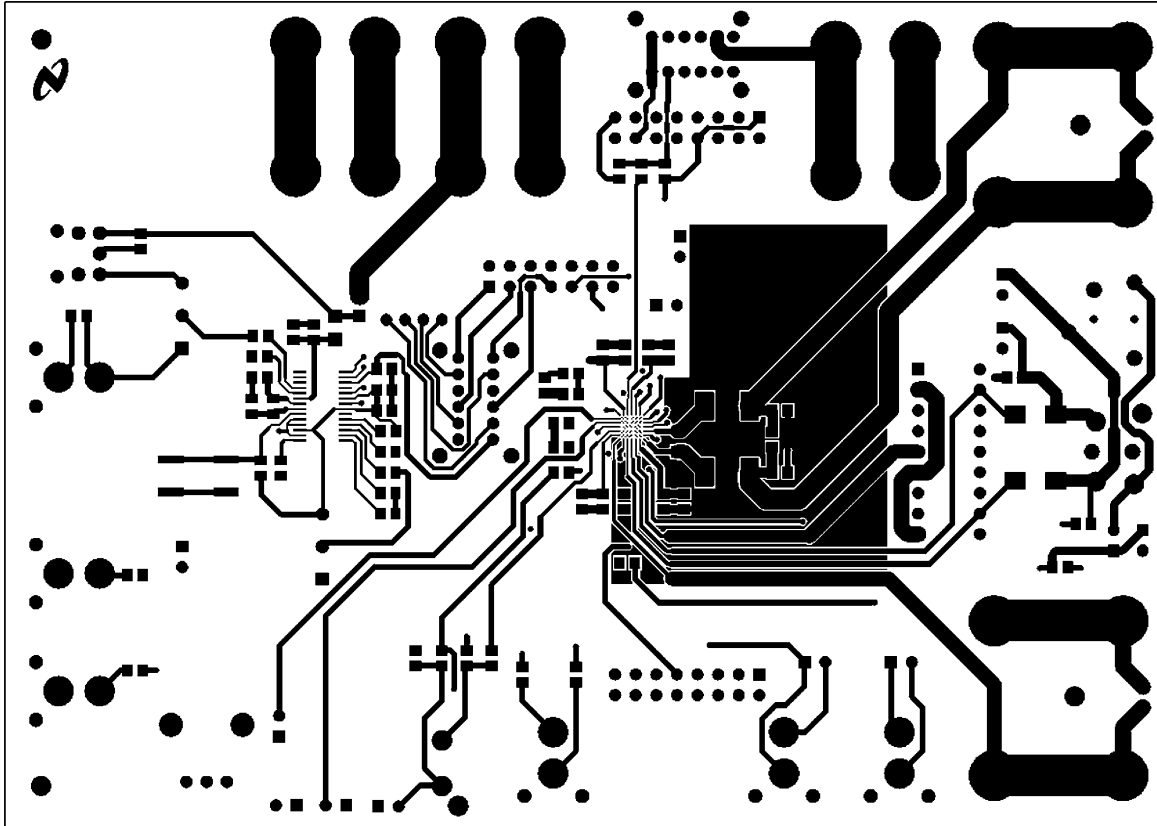




## Top Silkscreen

20134132

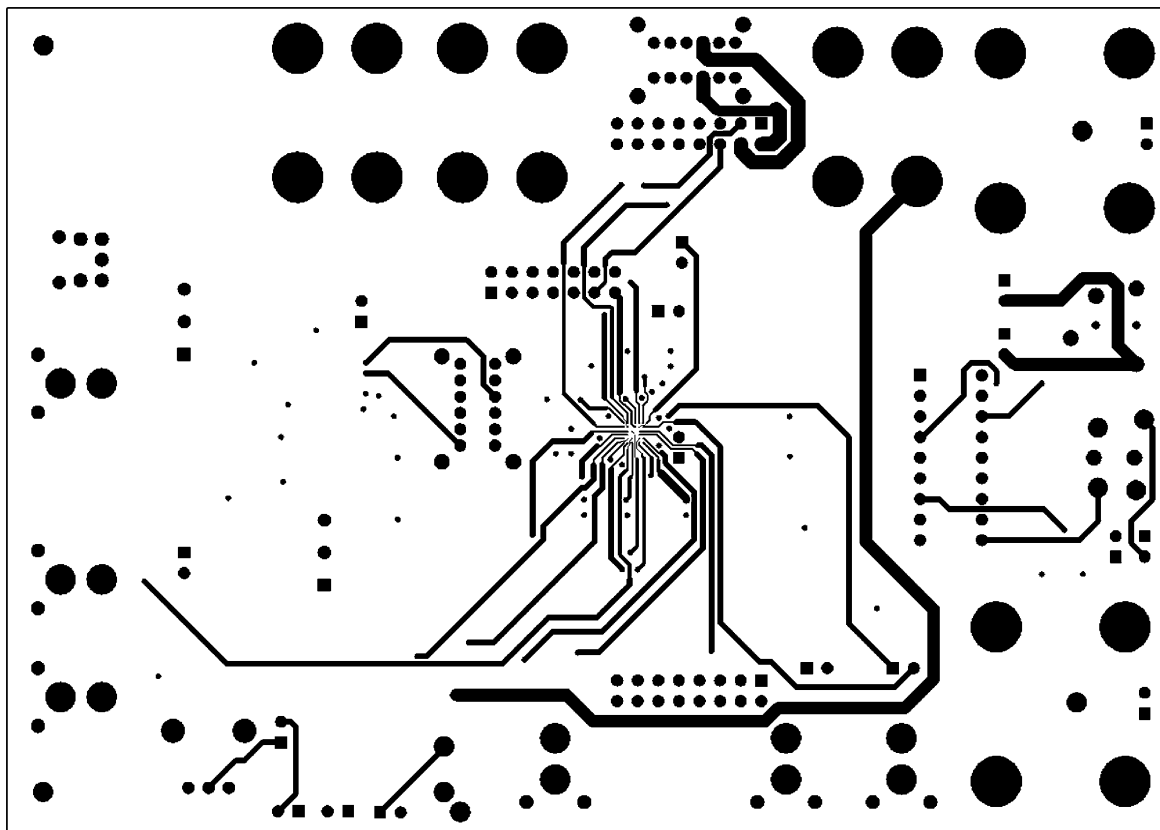
## 15.0 Demoboard PCB Layout (Continued)



Top Layer

20134131

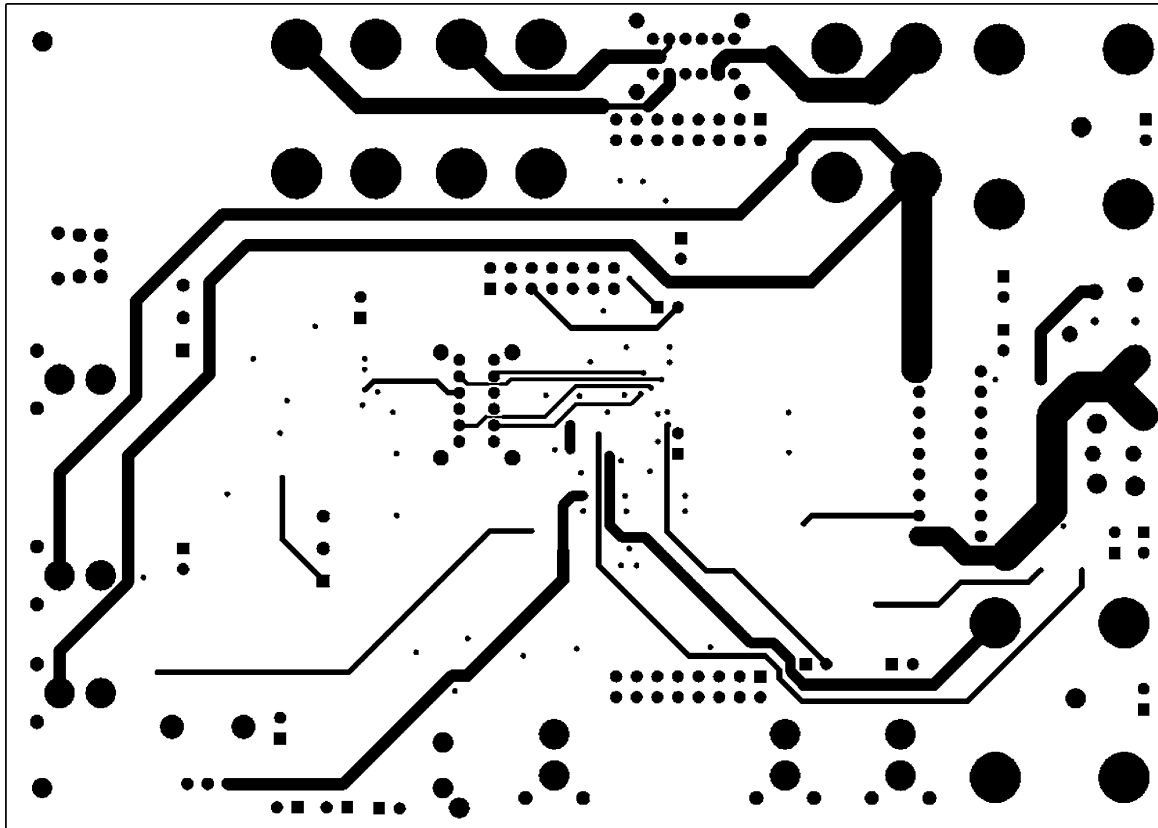
## 15.0 Demoboard PCB Layout (Continued)



Mid Layer 1

20134129

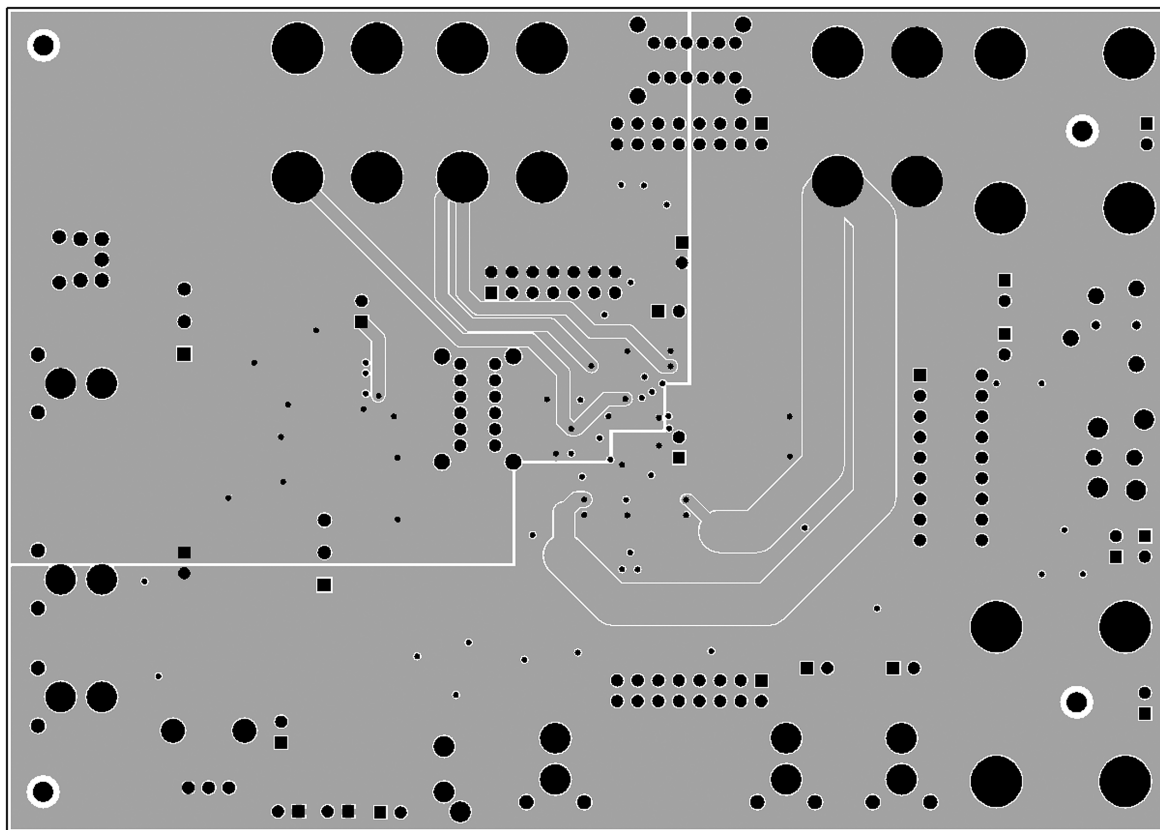
## 15.0 Demoboard PCB Layout (Continued)



Mid Layer 2

20134130

## 15.0 Demoboard PCB Layout (Continued)



Bottom Layer

20134128

## 16.0 Product Status Definitions

| Datasheet Status        | Product Status         | Definition                                                                                                                                                                                                                                                         |
|-------------------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance Information     | Formative or in Design | This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.                                                                                                                                |
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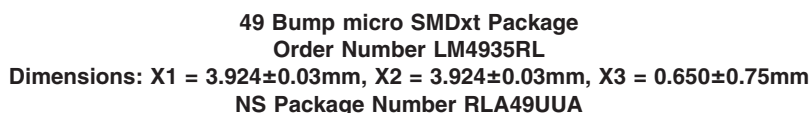
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## 17.0 Revision History

| Rev | Date     | Description                                                                                                                   |
|-----|----------|-------------------------------------------------------------------------------------------------------------------------------|
| 1.0 | 5/11/05  | Filled in the actual limits (for TBDs) under Limit and edited few Typical values, all under the EC table. Edits from Alvin F. |
| 1.1 | 7/29/05  | Input more edits. Replaced the correct boards. Replaced the Schematic Diagram (pg 60).                                        |
| 1.2 | 9/8/05   | Added the 1st set of Typ Perf curves.                                                                                         |
| 1.3 | 9/21/05  | Added a couple of tables.                                                                                                     |
| 1.4 | 9/30/05  | Input text edits.                                                                                                             |
| 1.5 | 10/5/05  | Input more edits.                                                                                                             |
| 1.6 | 10/11/05 | More edits.                                                                                                                   |
| 1.7 | 10/12/05 | First D/S WEB release.                                                                                                        |
| 1.8 | 10/14/5  | Input more text edits after the 1st released.                                                                                 |
| 1.9 | 10/17/05 | Input some text edits, then re-released D/S to the WEB.                                                                       |
| 2.0 | 10/18/05 | More text edits. Also used graphic 20134107 back.                                                                             |
| 2.1 | 12/19/05 | Added the RL package                                                                                                          |
| 2.2 | 12/20/05 | Deleted the WL pkg and replaced with the RL pkg.                                                                              |
| 2.3 | 1/19/06  | Fixed 20134132(top silkscreen) and 35 (schem layout) plus few text edits.                                                     |
| 2.4 | 1/25/06  | Fixed the value on X3 (mktg outline).<br>Re-released D/S to the WEB.                                                          |

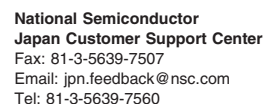
# LM4935 Audio Sub-System with Dual-Mode Stereo Headphone & Mono High Efficiency Loudspeaker Amplifiers and Multi-Purpose ADC



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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|                               |                                                                                          |
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