

# LMH6505

*LMH6505 Wideband, Low Power, Linear-in-dB, Variable Gain Amplifier*



Literature Number: SNOSAT4D

# LMH6505

## Wideband, Low Power, Linear-in-dB, Variable Gain Amplifier

### General Description

The LMH6505 is a wideband DC coupled voltage controlled gain stage followed by a high speed current feedback operational amplifier which can directly drive a low impedance load. The gain adjustment range is 80 dB for up to 10 MHz which is accomplished by varying the gain control input voltage,  $V_G$ .

Maximum gain is set by external components, and the gain can be reduced all the way to cutoff. Power consumption is 110 mW with a speed of 150 MHz and a gain control bandwidth (BW) of 100 MHz. Output referred DC offset voltage is less than 55 mV over the entire gain control voltage range. Device-to-device gain matching is within  $\pm 0.5$  dB at maximum gain. Furthermore, gain is tested and guaranteed over a wide range. The output current feedback op amp allows high frequency large signals (Slew Rate = 1500 V/ $\mu$ s) and can also drive a heavy load current (60 mA) guaranteed. Near ideal input characteristics (i.e. low input bias current, low offset, low pin 3 resistance) enable the device to be easily configured as an inverting amplifier as well.

To provide ease of use when working with a single supply, the  $V_G$  range is set to be from 0V to +2V relative to the ground pin potential (pin 4).  $V_G$  input impedance is high in order to ease drive requirement. In single supply operation, the ground pin is tied to a "virtual" half supply.

The LMH6505's gain control is linear in dB for a large portion of the total gain control range from 0 dB down to -85 dB at 25°C, as shown below. This makes the device suitable for AGC applications. For linear gain control applications, see the LMH6503 datasheet.

The LMH6505 is available in either the 8-Pin SOIC or the 8-Pin MSOP package. The combination of minimal external components and small outline packages allows the LMH6505 to be used in space-constrained applications.

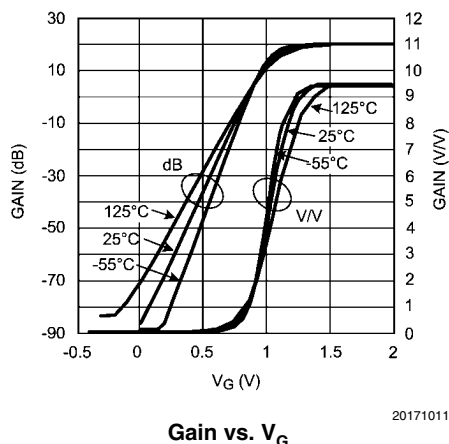
### Features

$V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $R_L = 100\Omega$ ,  $A_V = A_{VMAX} = 9.4\text{ V/V}$ , Typical values unless specified.

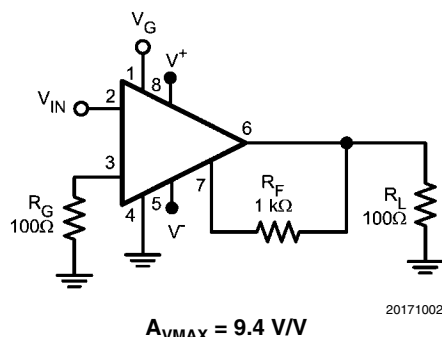
■ -3 dB BW	150 MHz
■ Gain control BW	100 MHz
■ Adjustment range (<10 MHz)	80 dB
■ Gain matching (limit)	$\pm 0.50$ dB
■ Supply voltage range	7V to 12V
■ Slew rate (inverting)	1500 V/ $\mu$ s
■ Supply current (no load)	11 mA
■ Linear output current	$\pm 60$ mA
■ Output voltage swing	$\pm 2.4V$
■ Input noise voltage	4.4 nV/ $\sqrt{\text{Hz}}$
■ Input noise current	2.6 pA/ $\sqrt{\text{Hz}}$
■ THD (20 MHz, $R_L = 100\Omega$ , $V_O = 2\text{ V}_{PP}$ )	-45 dBc

### Applications

- Variable attenuator
- AGC
- Voltage controlled filter
- Video imaging processing



### Typical Application



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 6)	
Human Body Model	2000V
Machine Model	200V
Input Current	±10 mA
Output Current (Note 3)	120 mA
Supply Voltages (V <sup>+</sup> - V <sup>-</sup> )	12.6V
Voltage at Input/ Output pins	V <sup>+</sup> +0.8V, V <sup>-</sup> -0.8V
Storage Temperature Range	-65°C to 150°C

Junction Temperature	150°C
Soldering Information:	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C

**Operating Ratings** (Note 1)

Supply Voltages (V <sup>+</sup> - V <sup>-</sup> )	7V to 12V
Temperature Range (Note 5)	-40°C to +85°C
Thermal Resistance:	( $\theta_{JC}$ ) ( $\theta_{JA}$ )
8 -Pin SOIC	60 165
8-Pin MSOP	65 235

**Electrical Characteristics** (Note 2)

Unless otherwise specified, all limits are guaranteed for T<sub>J</sub> = 25°C, V<sub>S</sub> = ±5V, A<sub>VMAX</sub> = 9.4 V/V, R<sub>F</sub> = 1 kΩ, R<sub>G</sub> = 100Ω, V<sub>IN</sub> = ±0.1V, R<sub>L</sub> = 100Ω, V<sub>G</sub> = +2V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Frequency Domain Response						
BW	−3 dB Bandwidth	V <sub>OUT</sub> < 1 V <sub>PP</sub>		150		MHz
		V <sub>OUT</sub> < 4 V <sub>PP</sub> , A <sub>VMAX</sub> = 100		38		
GF	Gain Flatness	V <sub>OUT</sub> < 1 V <sub>PP</sub> 0.9V ≤ V <sub>G</sub> ≤ 2V, ±0.2 dB		40		MHz
Att Range	Flat Band (Relative to Max Gain) Attenuation Range (Note 15)	±0.2 dB Flatness, f < 30 MHz		26		dB
		±0.1 dB Flatness, f < 30 MHz		9.5		
BW Control	Gain control Bandwidth	V <sub>G</sub> = 1V (Note 4)		100		MHz
CT (dB)	Feed-through	V <sub>G</sub> = 0V, 30 MHz (Output/Input)		−51		dB
GR	Gain Adjustment Range	f < 10 MHz		80		dB
		f < 30 MHz		71		
Time Domain Response						
t <sub>r</sub> , t <sub>f</sub>	Rise and Fall Time	0.5V Step		2.1		ns
OS %	Overshoot			10		%
SR	Slew Rate (Note 7)	Non Inverting		900		V/μs
		Inverting		1500		
Distortion & Noise Performance						
HD2	2 <sup>nd</sup> Harmonic Distortion	2V <sub>PP</sub> , 20 MHz		−47		dBc
HD3	3 <sup>rd</sup> Harmonic Distortion			−61		
THD	Total Harmonic Distortion			−45		
En tot	Total Equivalent Input Noise	f > 1 MHz, R <sub>SOURCE</sub> = 50Ω		4.4		nV/√Hz
I <sub>N</sub>	Input Noise Current	f > 1 MHz		2.6		pA/√Hz
DG	Differential Gain	f = 4.43 MHz, R <sub>L</sub> = 100Ω		0.30		%
DP	Differential Phase			0.15		deg
DC & Miscellaneous Performance						
GACCU	Gain Accuracy (See Application Information)	V <sub>G</sub> = 2.0V		0	±0.50	dB
		0.8V < V <sub>G</sub> < 2V		+0.1/−0.53	+4.3/−3.9	
G Match	Gain Matching (See Application Information)	V <sub>G</sub> = 2.0V		—	±0.50	dB
		0.8V < V <sub>G</sub> < 2V		—	+4.2/−4.0	
K	Gain Multiplier (See Application Information)		0.890 0.830	0.940	0.990 1.04	V/V

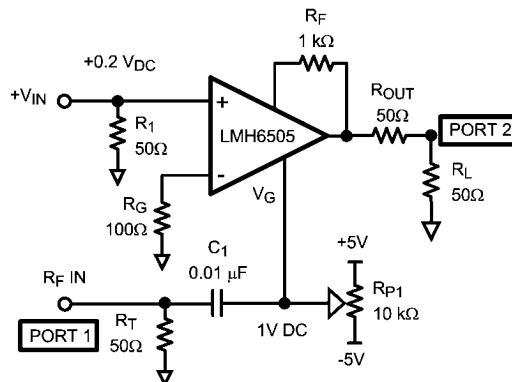
Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
$V_{IN\ NL}$	Input Voltage Range	$R_G$ Open		$\pm 3$		V
$V_{IN\ L}$		$R_G = 100\Omega$	$\pm 0.60$ <b><math>\pm 0.50</math></b>	$\pm 0.74$		
$I_{RG\_MAX}$	$R_G$ Current	Pin 3	$\pm 6.0$ <b><math>\pm 5.0</math></b>	$\pm 7.4$		mA
$I_{BIAS}$	Bias Current	Pin 2 (Note 10)		-0.6	-2.5 <b>-2.6</b>	$\mu A$
$TC\ I_{BIAS}$	Bias Current Drift	Pin 2 (Note 11)		1.28		nA/ $^{\circ}C$
$R_{IN}$	Input Resistance	Pin 2		7		M $\Omega$
$C_{IN}$	Input Capacitance	Pin 2		2.8		pF
$I_{VG}$	$V_G$ Bias Current	Pin 1, $V_G = 2V$ (Note 10)		0.9		$\mu A$
$TC\ I_{VG}$	$V_G$ Bias Drift	Pin 1 (Note 11)		10		pA/ $^{\circ}C$
$R_{VG}$	$V_G$ Input Resistance	Pin 1		25		M $\Omega$
$C_{VG}$	$V_G$ Input Capacitance	Pin 1		2.8		pF
$V_{OUT\ L}$	Output Voltage Range	$R_L = 100\Omega$	$\pm 2.1$ <b><math>\pm 1.9</math></b>	$\pm 2.4$		V
$V_{OUT\ NL}$		$R_L = \text{Open}$		$\pm 3.1$		
$R_{OUT}$	Output Impedance	DC		0.12		$\Omega$
$I_{OUT}$	Output Current	$V_{OUT} = \pm 4V$ from Rails	$\pm 60$ <b><math>\pm 40</math></b>	$\pm 80$		mA
$V_{O\ OFFSET}$	Output Offset Voltage	$0V < V_G < 2V$		$\pm 10$	$\pm 55$ <b><math>\pm 70</math></b>	mV
+PSRR	+Power Supply Rejection Ratio (Note 12)	Input Referred, 1V change, $V_G = 2.2V$	-65	-72		dB
-PSRR	-Power Supply Rejection Ratio (Note 12)	Input Referred, 1V change, $V_G = 2.2V$	-65	-75		dB
$I_S$	Supply Current	No Load	9.5 <b>7.5</b>	11	14 <b>16</b>	mA

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics.

**Note 2:** Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No guarantee of parametric performance is indicated in the Electrical Tables under conditions of internal self-heating where  $T_J > T_A$ .

**Note 3:** The maximum output current ( $I_{OUT}$ ) is determined by device power dissipation limitations or value specified, whichever is lower.

**Note 4:** Gain control frequency response schematic:



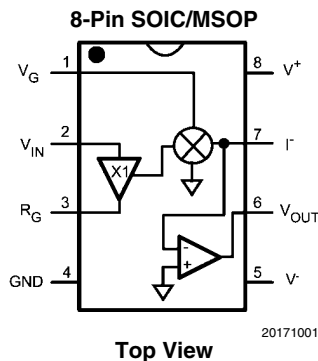
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**Note 5:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

**Note 6:** Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

- Note 7:** Slew rate is the average of the rising and falling slew rates.
- Note 8:** Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- Note 9:** Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
- Note 10:** Positive current corresponds to current flowing into the device.
- Note 11:** Drift is determined by dividing the change in parameter distribution at temperature extremes by the total temperature change.
- Note 12:** +PSRR definition:  $[\Delta V_{OUT}/\Delta V^+ / A_V]$ , -PSRR definition:  $[\Delta V_{OUT}/\Delta V^- / A_V]$  with 0.1V input voltage.  $\Delta V_{OUT}$  is the change in output voltage with offset shift subtracted out.
- Note 13:** Gain/Phase normalized to low frequency value at 25°C.
- Note 14:** Gain/Phase normalized to low frequency value at each setting.
- Note 15:** Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either  $\pm 0.2$  dB or  $\pm 0.1$  dB), relative to  $A_{VMAX}$  gain. For example, for  $f < 30$  MHz, here are the Flat Band Attenuation ranges:  
 $\pm 0.2$  dB: 19.7 dB down to -6.3 dB = 26 dB range  
 $\pm 0.1$  dB: 19.7 dB down to 10.2 dB = 9.5 dB range

Connection Diagram



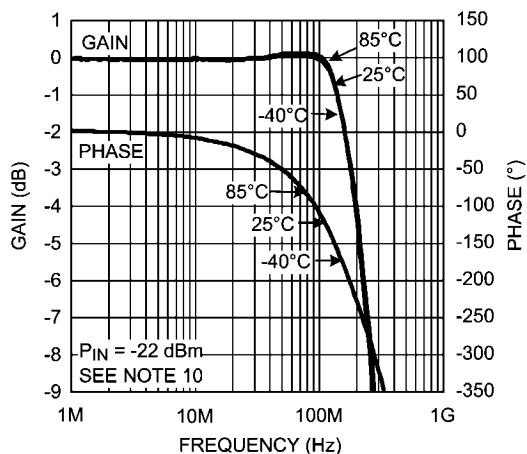
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6505MA	LMH6505MA	95 Units/Rail	M08A
	LMH6505MAX		2.5k Units Tape and Reel	
8-Pin MSOP	LMH6505MM	AZ2A	1k Units Tape and Reel	MUA08A
	LMH6505MMX		3.5k Units Tape and Reel	

## Typical Performance Characteristics

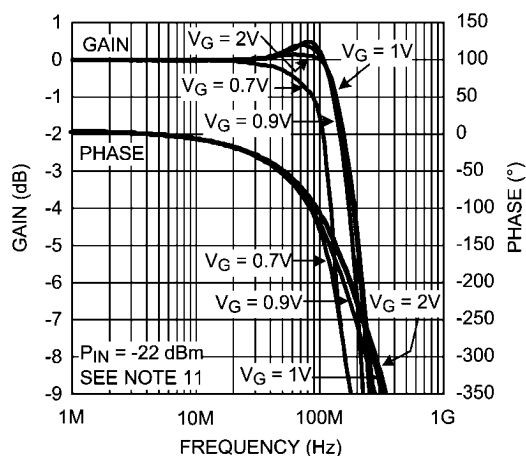
Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

### Frequency Response Over Temperature



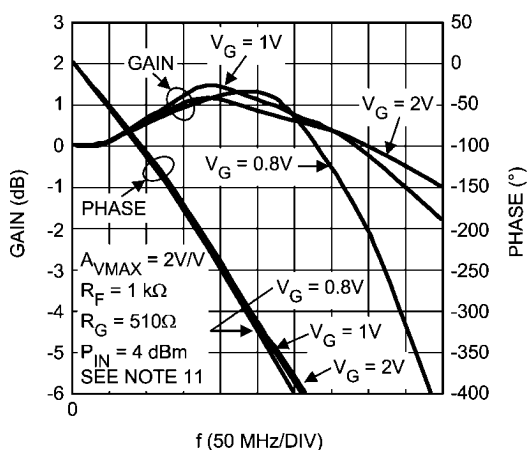
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### Frequency Response for Various $V_G$



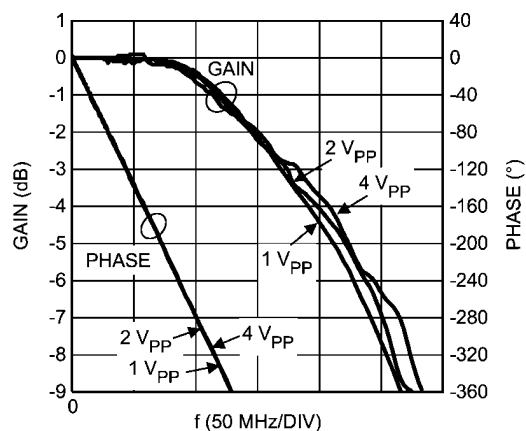
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### Frequency Response ( $A_{VMAX} = 2$ )



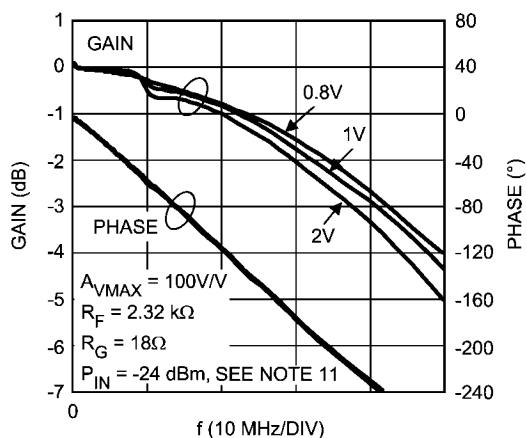
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### Inverting Frequency Response



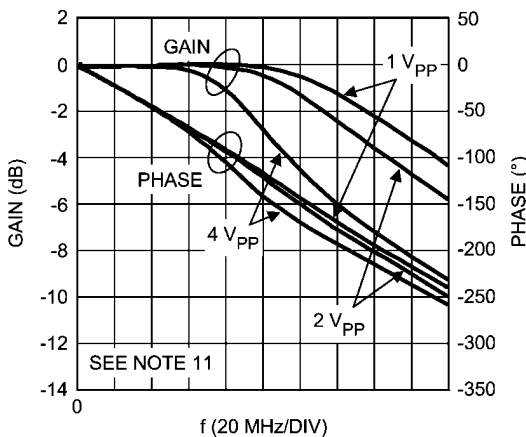
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### Frequency Response for Various $V_G$ ( $A_{VMAX} = 100$ ) (Large Signal)



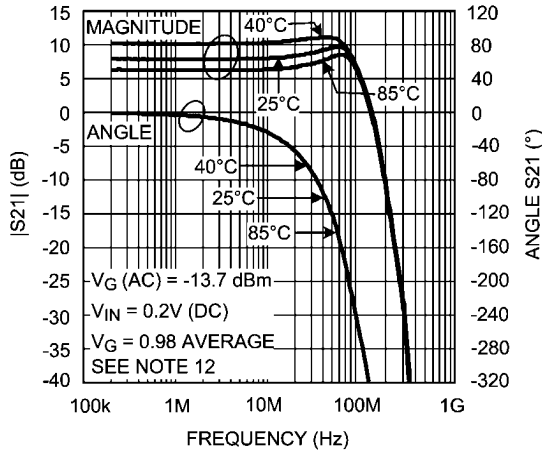
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### Frequency Response for Various Amplitudes



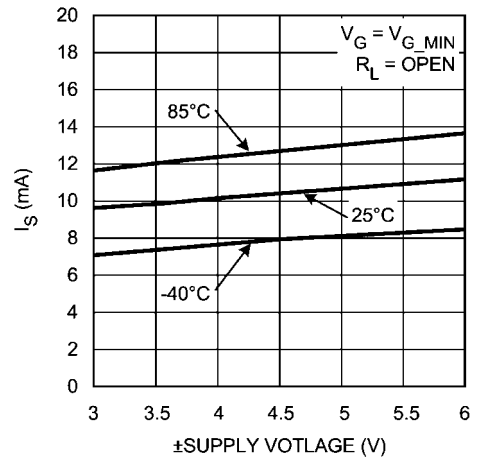
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Gain Control Frequency Response



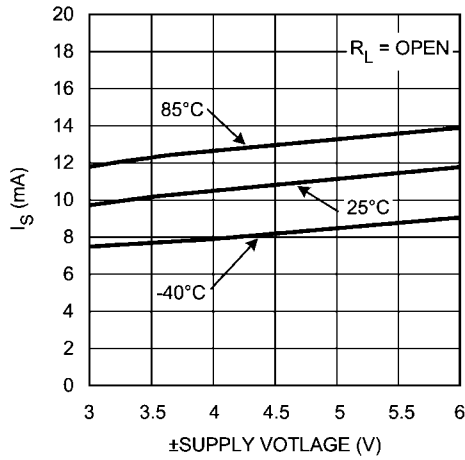
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$I_S$  vs.  $V_S$



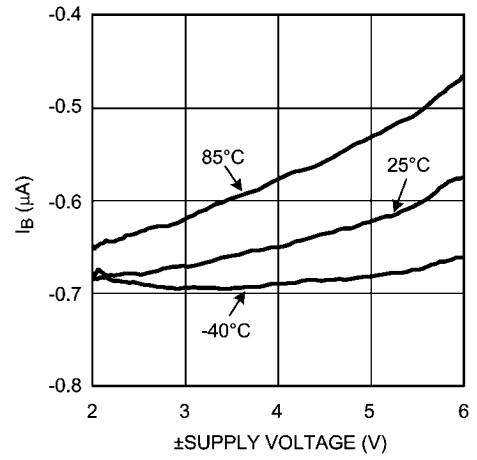
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$I_S$  vs.  $V_S$



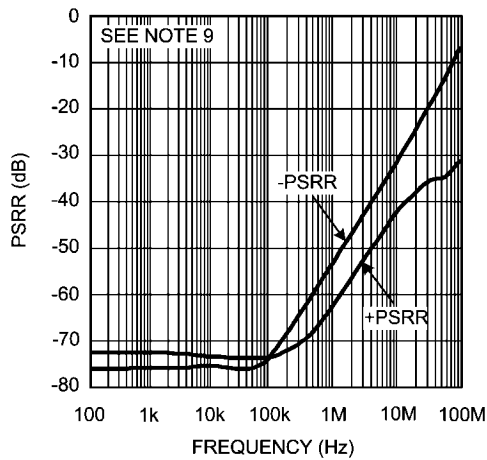
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Input Bias Current vs.  $V_S$



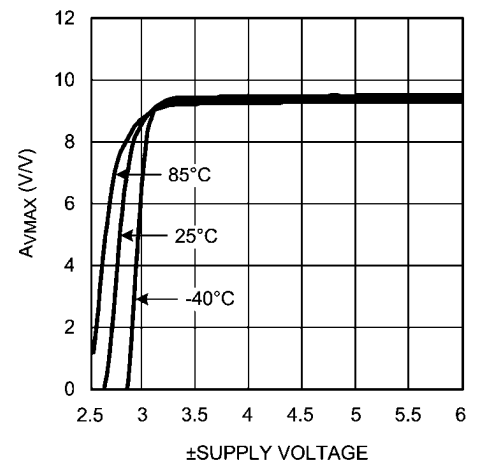
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PSRR

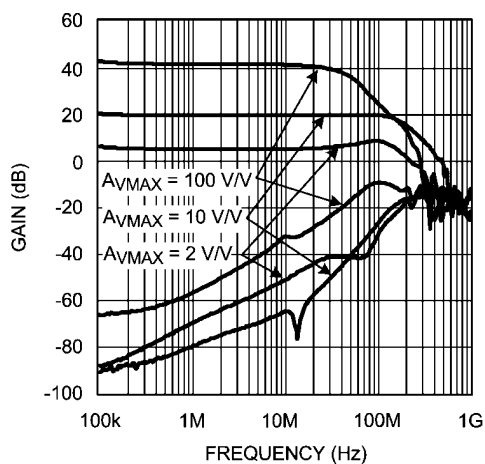


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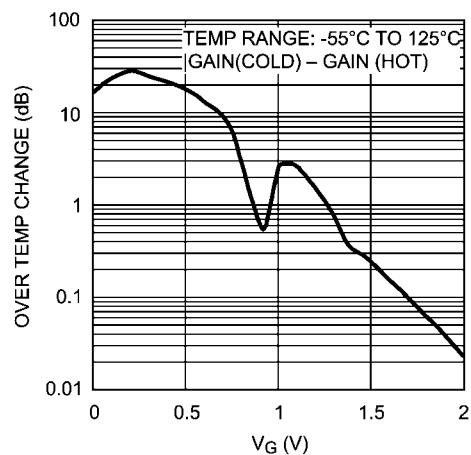
$A_{VMAX}$  vs. Supply Voltage



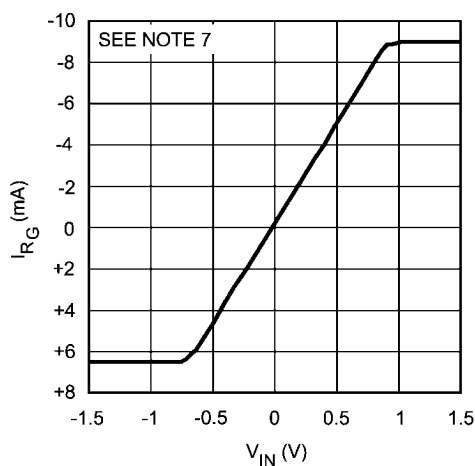
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Feed through Isolation for Various  $A_{VMAX}$ 

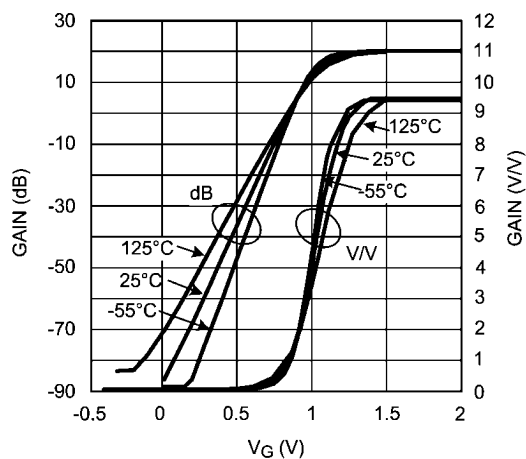
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Gain Variation Over entire Temp Range vs.  $V_G$ 

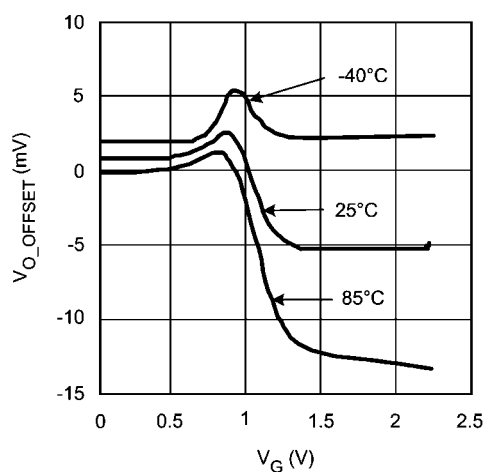
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 $I_{RG}$  vs.  $V_{IN}$ 

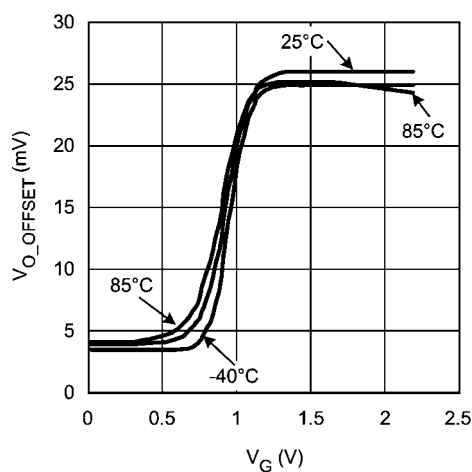
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Gain vs.  $V_G$ 

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Output Offset Voltage vs.  $V_G$  (Typical Unit #1)

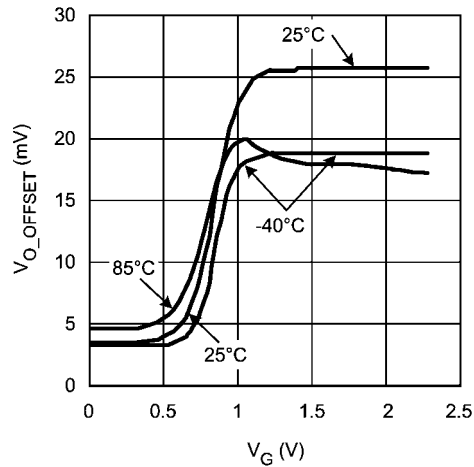
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Output Offset Voltage vs.  $V_G$  (Typical Unit #2)

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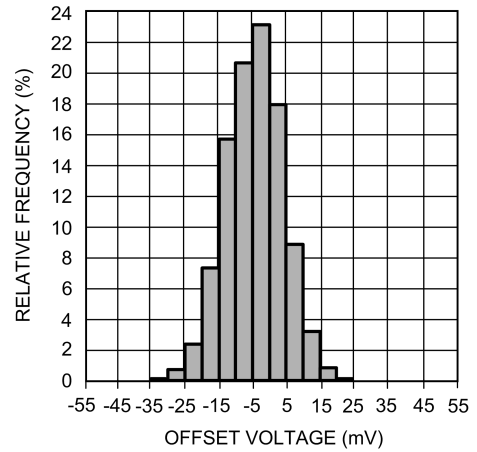


Output Offset Voltage vs.  $V_G$  (Typical Unit #3)



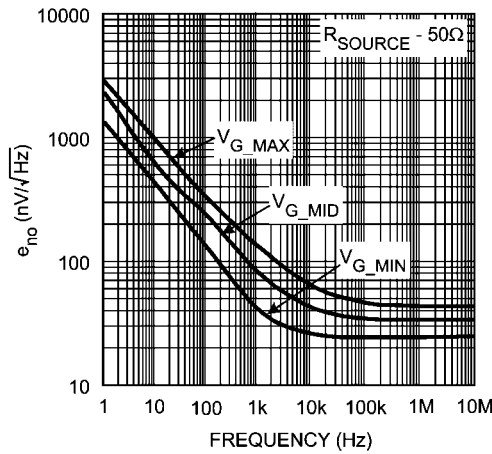
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Distribution of Output Offset Voltage



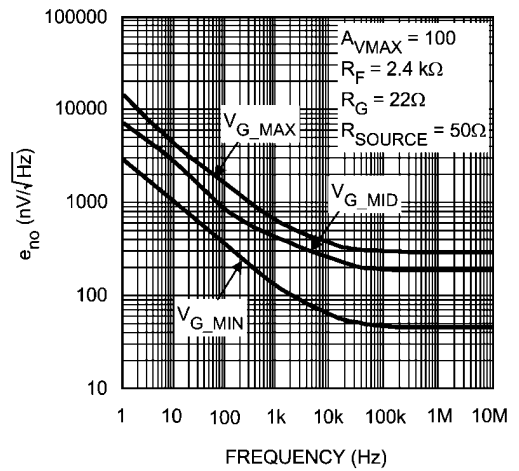
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Output Noise Density vs. Frequency



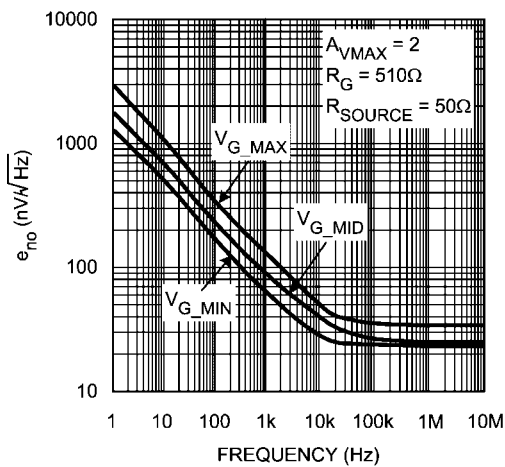
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Output Noise Density vs. Frequency



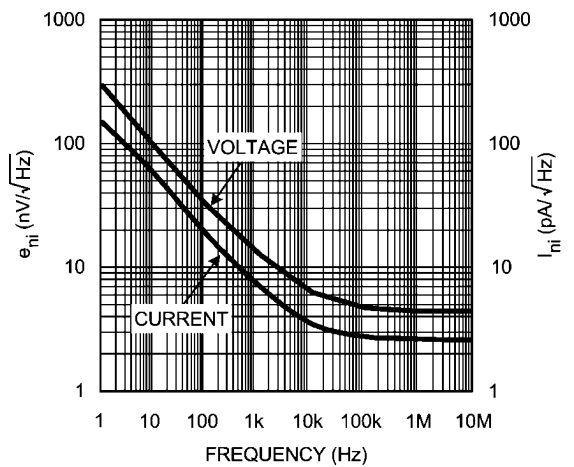
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Output Noise Density vs. Frequency



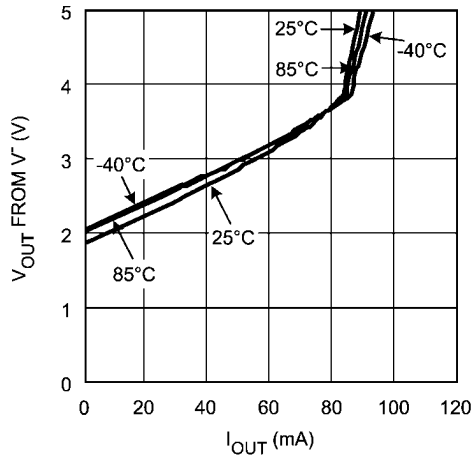
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Input Referred Noise Density vs. Frequency



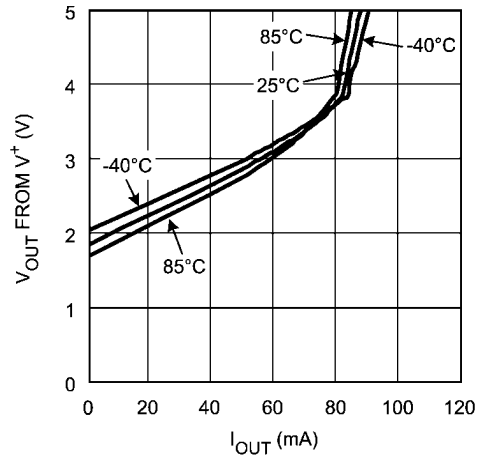
20171036

Output Voltage vs. Output Current (Sinking)



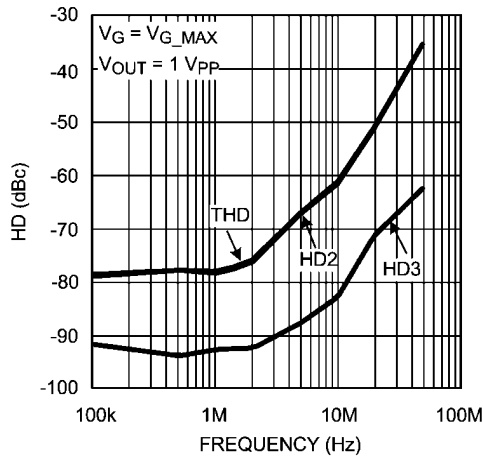
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Output Voltage vs. Output Current (Sourcing)



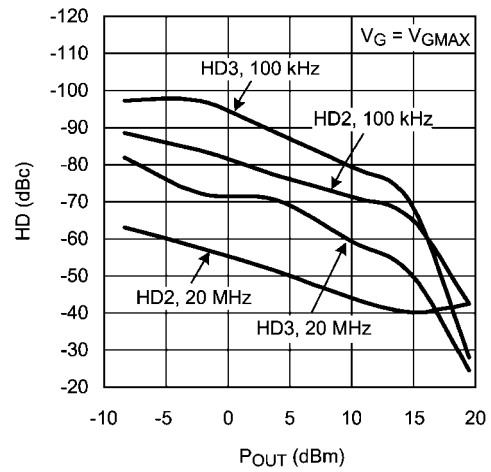
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Distortion vs. Frequency



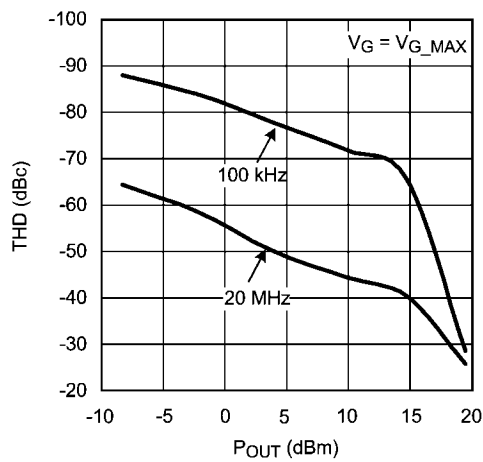
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HD vs.  $P_{OUT}$



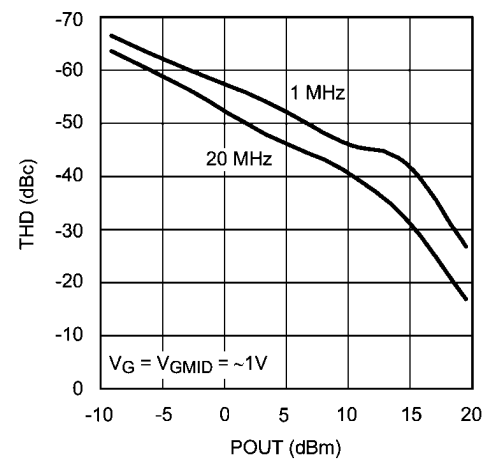
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THD vs.  $P_{OUT}$

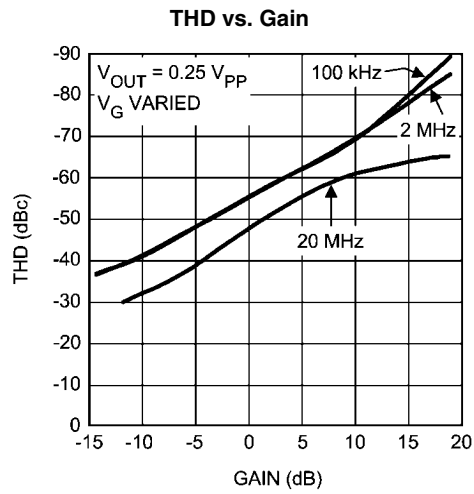


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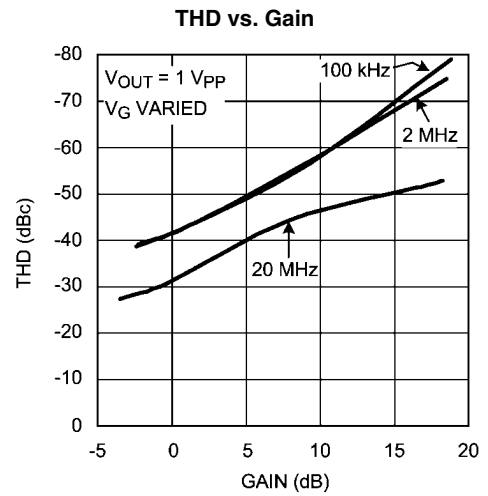
THD vs.  $P_{OUT}$



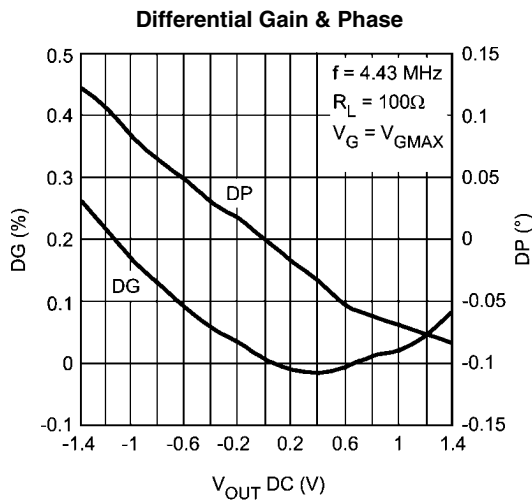
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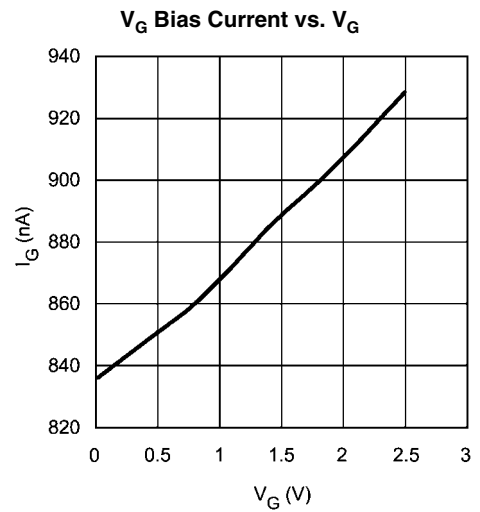
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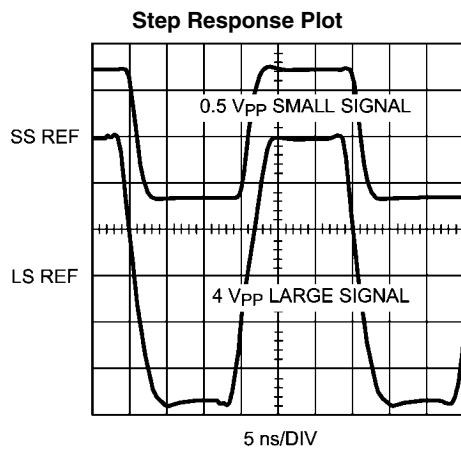
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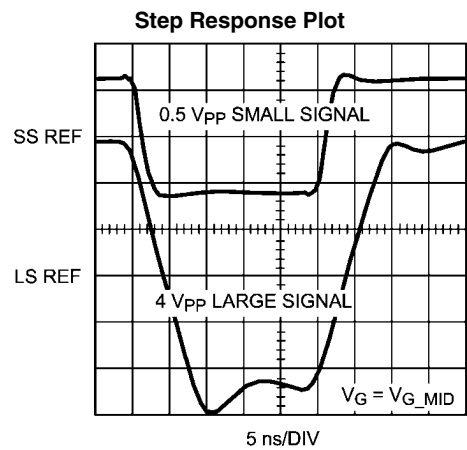
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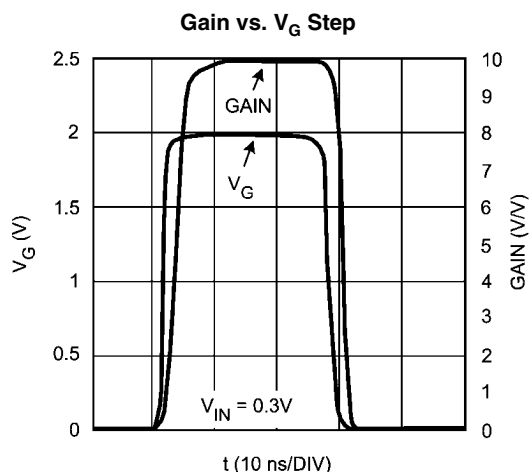
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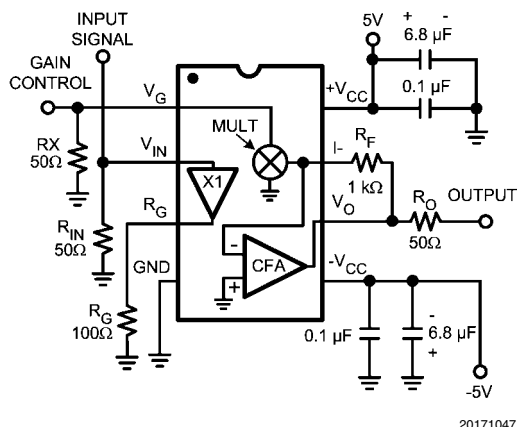
## Application Information

### GENERAL DESCRIPTION

The key features of the LMH6505 are:

- Low power
- Broad voltage controlled gain and attenuation range (from  $A_{VMAX}$  down to complete cutoff)
- Bandwidth independent, resistor programmable gain range ( $R_G$ )
- Broad signal and gain control bandwidths
- Frequency response may be adjusted with  $R_F$
- High impedance signal and gain control inputs

The LMH6505 combines a closed loop input buffer ("X1" Block in Figure 1), a voltage controlled variable gain cell ("MULT" Block) and an output amplifier ("CFA" Block). The input buffer is a transconductance stage whose gain is set by the gain setting resistor,  $R_G$ . The output amplifier is a current feedback op amp and is configured as a transimpedance stage whose gain is set by, and is equal to, the feedback resistor,  $R_F$ . The maximum gain,  $A_{VMAX}$ , of the LMH6505 is defined by the ratio:  $K \cdot R_F/R_G$  where "K" is the gain multiplier with a nominal value of 0.940. As the gain control input ( $V_G$ ) changes over its 0 to 2V range, the gain is adjusted over a range of about 80 dB relative to the maximum set gain.



20171047

FIGURE 1. LMH6505 Typical Application and Block Diagram

### SETTING THE LMH6505 MAXIMUM GAIN

$$A_{VMAX} = \frac{R_F}{R_G} \cdot K \quad (1)$$

Although the LMH6505 is specified at  $A_{VMAX} = 9.4$  V/V, the recommended  $A_{VMAX}$  varies between 2 and 100. Higher gains are possible but usually impractical due to output offsets, noise and distortion. When varying  $A_{VMAX}$  several tradeoffs are made:

$R_G$ : determines the input voltage range

$R_F$ : determines overall bandwidth

The amount of current which the input buffer can source/sink into  $R_G$  is limited and is given in the  $I_{RG\_MAX}$  specification. This sets the maximum input voltage:

$$V_{IN} (MAX) = I_{RG\_MAX} \cdot R_G \quad (2)$$

As the  $I_{RG\_MAX}$  limit is approached with increasing the input voltage or with the lowering of  $R_G$ , the device's harmonic distortion will increase. Changes in  $R_F$  will have a dramatic effect on the small signal bandwidth. The output amplifier of the LMH6505 is a current feedback amplifier (CFA) and its bandwidth is determined by  $R_F$ . As with any CFA, doubling the feedback resistor will roughly cut the bandwidth of the device in half. For more about CFAs, see the basic tutorial, OA-20, "Current Feedback Myths Debunked," or a more rigorous analysis, OA-13, "Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements."

### OTHER CONFIGURATIONS

#### 1) Single Supply Operation

The LMH6505 can be configured for use in a single supply environment. Doing so requires the following:

- Bias pin 4 and  $R_G$  to a "virtual half supply" somewhere close to the middle of  $V^+$  and  $V^-$  range. The other end of  $R_G$  is tied to pin 3. The "virtual half supply" needs to be capable of sinking and sourcing the expected current flow through  $R_G$ .
- Ensure that  $V_G$  can be adjusted from 0V to 2V above the "virtual half supply".
- Bias the input (pin 2) to make sure that it stays within the range of 2V above  $V^-$  to 2V below  $V^+$ . See the Input Voltage Range specification in the Electrical Characteristics table. This can be accomplished by either DC biasing the

input and AC coupling the input signal, or alternatively, by direct coupling if the output of the driving stage is also biased to half supply.

Arranged this way, the LMH6505 will respond to the current flowing through  $R_G$ . The gain control relationship will be similar to the split supply arrangement with  $V_G$  measured with reference to pin 4. Keep in mind that the circuit described above will also center the output voltage to the "virtual half supply voltage."

## 2) Arbitrarily Referenced Input Signal

Having a wide input voltage range on the input (pin 2) ( $\pm 3V$  typical), the LMH6505 can be configured to control the gain on signals which are not referenced to ground (e.g. Half Supply biased circuits). This node will be called the "reference node". In such cases, the other end of  $R_G$  which is the side not tied to pin 3 can be tied to this reference node so that  $R_G$  will "look at" the difference between the signal and this reference only. Keep in mind that the reference node needs to source and sink the current flowing through  $R_G$ .

### GAIN ACCURACY

Gain accuracy is defined as the actual gain compared against the theoretical gain at a certain  $V_G$ , the results of which are expressed in dB. (See Figure 2).

Theoretical gain is given by:

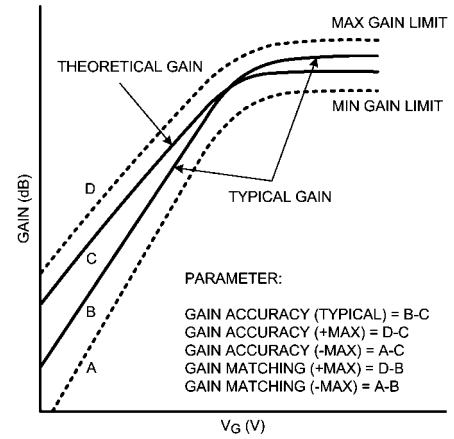
$$A(V/V) = K \times \frac{R_F}{R_G} \times \frac{1}{1 + e^{\left[ \frac{N - V_G}{V_C} \right]}} \quad (3)$$

Where  $K = 0.940$  (nominal)  $N = 1.01V$  &  $V_C = 79 \text{ mV}$  at room temperature

For a  $V_G$  range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the difference between the "Typical Gain" and the "Theoretical Gain." The "Max" value would be the worst case difference between the actual gain and the "Theoretical Gain" for the entire population.

### GAIN MATCHING

As Figure 2 shows, gain matching is the limit on gain variation at a certain  $V_G$ , expressed in dB, and is specified as " $\pm \text{Max}$ " only. There is no "Typical." For a  $V_G$  range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case difference between the actual gain and the typical gain for the entire population.

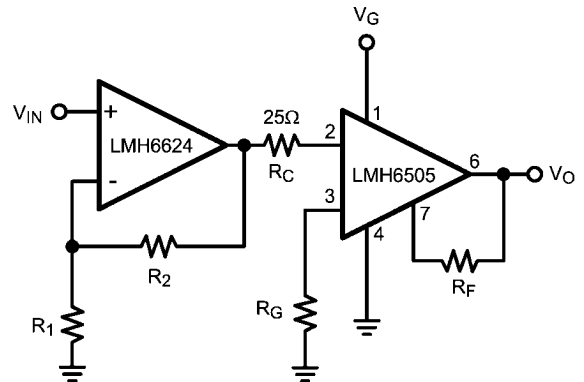


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FIGURE 2. LMH6505 Gain Accuracy & Gain Matching Defined

### GAIN PARTITIONING

If high levels of gain are needed, gain partitioning should be considered:



20171052

FIGURE 3. Gain Partitioning

The maximum gain range for this circuit is given by the following equation:

$$\text{MAXIMUM GAIN} = \left[ 1 + \frac{R_2}{R_1} \right] \cdot \left[ \frac{R_F}{R_G} \right] \cdot K \quad (4)$$

The LMH6624 is a low noise wideband voltage feedback amplifier. Setting  $R_2$  at  $909\Omega$  and  $R_1$  at  $100\Omega$  produces a gain of 20 dB. Setting  $R_F$  at  $1000\Omega$  as recommended and  $R_G$  at  $50\Omega$ , produces a gain of about 26 dB in the LMH6505. The total gain of this circuit is therefore approximately 46 dB. It is important to understand that when partitioning to obtain high levels of gain, very small signal levels will drive the amplifiers to full scale output. For example, with 46 dB of gain, a 20 mV signal at the input will drive the output of the LMH6624 to 200 mV and the output of the LMH6505 to 4V. Accordingly, the designer must carefully consider the contributions of each stage to the overall characteristics. Through gain partitioning the designer is provided with an opportunity to optimize the frequency response, noise, distortion, settling time, and loading effects of each amplifier to achieve improved overall performance.

## LMH6505 GAIN CONTROL RANGE AND MINIMUM GAIN

Before discussing Gain Control Range, it is important to understand the issues which limit it. The minimum gain of the LMH6505 is theoretically zero, but in practical circuits it is limited by the amount of feedthrough, here defined as the gain when  $V_G = 0V$ . Capacitive coupling through the board and package, as well as coupling through the supplies, will determine the amount of feedthrough. Even at DC, the input signal will not be completely rejected. At high frequencies feedthrough will get worse because of its capacitive nature. At frequencies below 10 MHz, the feed through will be less than  $-60$  dB and therefore, it can be said that with  $A_{VMAX} = 20$  dB, the gain control range is 80 dB.

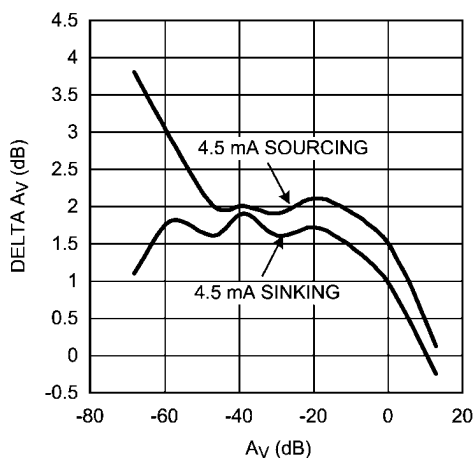
## LMH6505 GAIN CONTROL FUNCTION

In the plot, Gain vs.  $V_G$ , we can see the gain as a function of the control voltage. The "Gain (V/V)" plot, sometimes referred to as the S-curve, is the linear (V/V) gain. This is a hyperbolic tangent relationship and is given by Equation 3. The "Gain (dB)" plots the gain in dB and is linear over a wide range of gains. Because of this, the LMH6505 gain control is referred to as "linear-in-dB."

For applications where the LMH6505 will be used at the heart of a closed loop AGC circuit, the S-curve control characteristic provides a broad linear (in dB) control range with soft limiting at the highest gains where large changes in control voltage result in small changes in gain. For applications requiring a fully linear (in dB) control characteristic, use the LMH6505 at half gain and below ( $V_G \leq 1V$ ).

## GAIN STABILITY

The LMH6505 architecture allows complete attenuation of the output signal from full gain to complete cutoff. This is achieved by having the gain control signal  $V_G$  "throttle" the signal which gets through to the final stage and which results in the output signal. As a consequence, the  $R_G$  pin's (pin 3) average current (DC current) influences the operating point of this "throttle" circuit and affects the LMH6505's gain slightly. Figure 4 below, shows this effect as a function of the gain set by  $V_G$ .



20171066

**FIGURE 4. LMH6505 Gain Variation over  $R_G$  DC Current Capability vs. Gain**

This plot shows the expected gain variation for the maximum  $R_G$  DC current capability ( $\pm 4.5$  mA). For example, with gain ( $A_V$ ) set to  $-60$  dB, if the  $R_G$  pin DC current is increased to 4.5 mA sourcing, one would expect to see the gain increase by about 3 dB (to  $-57$  dB). Conversely, 4.5 mA DC sinking cur-

rent through  $R_G$  would increase gain by 1.75 dB (to  $-58.25$  dB). As you can see from Figure 4 above, the effect is most pronounced with reduced gain and is limited to less than 3.75 dB variation maximum.

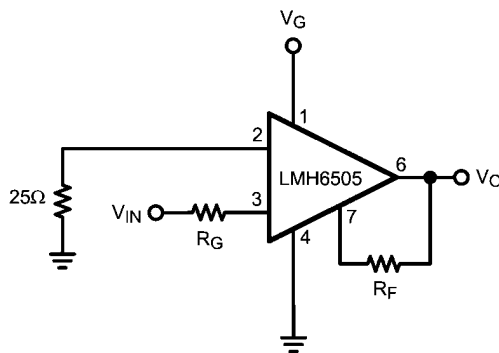
If the application is expected to experience  $R_G$  DC current variation and the LMH6505 gain variation is beyond acceptable limits, please refer to the LMH6502 (Differential Linear in dB variable gain amplifier) datasheet instead at <http://www.national.com/ds/LM/LMH6502.pdf>.

## AVOIDING OVERDRIVE OF THE LMH6505 GAIN CONTROL INPUT

There is an additional requirement for the LMH6505 Gain Control Input ( $V_G$ ):  $V_G$  must not exceed  $+2.3V$  (with  $\pm 5V$  supplies). The gain control circuitry may saturate and the gain may actually be reduced. In applications where  $V_G$  is being driven from a DAC, this can easily be addressed in the software. If there is a linear loop driving  $V_G$ , such as an AGC loop, other methods of limiting the input voltage should be implemented. One simple solution is to place a 2.2:1 resistive divider on the  $V_G$  input. If the device driving this divider is operating off of  $\pm 5V$  supplies as well, its output will not exceed 5V and through the divider  $V_G$  can not exceed 2.3V.

## IMPROVING THE LMH6505 LARGE SIGNAL PERFORMANCE

Figure 5 illustrates an inverting gain scheme for the LMH6505.



20171054

**FIGURE 5. Inverting Amplifier**

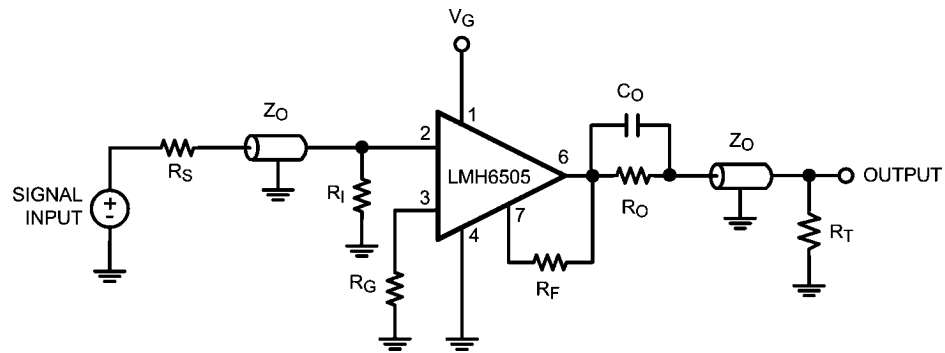
The input signal is applied through the  $R_G$  resistor. The  $V_{IN}$  pin should be grounded through a  $25\Omega$  resistor. The maximum gain range of this configuration is given in the following equation:

$$A_{VMAX} = - \left[ \frac{R_F}{R_G} \right] \cdot K \quad (5)$$

The inverting slew rate of the LMH6505 is much higher than that of the non-inverting slew rate. This  $\approx 2X$  performance improvement comes about because in the non-inverting configuration the slew rate of the overall amplifier is limited by the input buffer. In the inverting circuit, the input buffer remains at a fixed voltage and does not affect slew rate.

## TRANSMISSION LINE MATCHING

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows a typical circuit configuration for matching transmission lines.



20171056

FIGURE 6. Transmission Line Matching

The resistors  $R_S$ ,  $R_I$ ,  $R_O$ , and  $R_T$  are equal to the characteristic impedance,  $Z_O$ , of the transmission line or cable. Use  $C_O$  to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

#### MINIMIZING PARASITIC EFFECTS ON SMALL SIGNAL BANDWIDTH

The best way to minimize parasitic effects is to use surface mount components and to minimize lead lengths and component distance from the LMH6505. For designs utilizing through-hole components, specifically axial resistors, resistor self-capacitance should be considered. For example, the average magnitude of parasitic capacitance of RN55D 1% metal film resistors is about 0.15 pF with variations of as much as 0.1 pF between lots. Given the LMH6505's extended bandwidth, these small parasitic reactance variations can cause measurable frequency response variations in the highest octave. We therefore recommend the use of surface mount resistors to minimize these parasitic reactance effects.

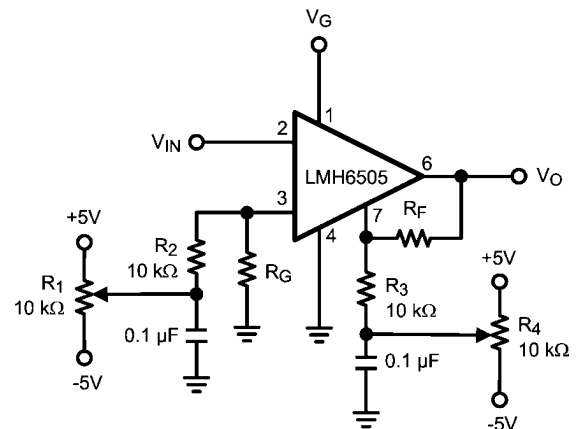
#### RECOMMENDATIONS

Here are some recommendations to avoid problems and to get the best performance:

- Do not place a capacitor across  $R_F$ . However, an appropriately chosen series RC combination can be used to shape the frequency response.
- Keep traces connecting  $R_F$  separated and as short as possible.
- Place a small resistor (20-50 $\Omega$ ) between the output and  $C_L$ .
- Cut away the ground plane, if any, under  $R_G$ .
- Keep decoupling capacitors as close as possible to the LMH6505.
- Connect pin 2 through a minimum resistance of 25 $\Omega$ .

#### ADJUSTING OFFSETS AND DC LEVEL SHIFTING

Offsets can be broken into two parts: an input-referred term and an output-referred term. These errors can be trimmed using the circuit in Figure 7. First set  $V_G$  to 0V and adjust the trim pot  $R_4$  to null the offset voltage at the output. This will eliminate the output stage offsets. Next set  $V_G$  to 2V and adjust the trim pot  $R_1$  to null the offset voltage at the output. This will eliminate the input stage offsets.



20171057

FIGURE 7. Offset Adjust Circuit

#### DIGITAL GAIN CONTROL

Digitally variable gain control can be easily realized by driving the LMH6505 gain control input with a digital-to-analog converter (DAC). Figure 8 illustrates such an application. This circuit employs National Semiconductor's eight-bit DAC0830, the LMC8101 MOS input op amp (Rail-to-Rail Input/Output), and the LMH6505 VGA. With  $V_{REF}$  set to 2V, the circuit provides up to 80 dB of gain control in 256 steps with up to 0.05% full scale resolution. The maximum gain of this circuit is 20 dB.

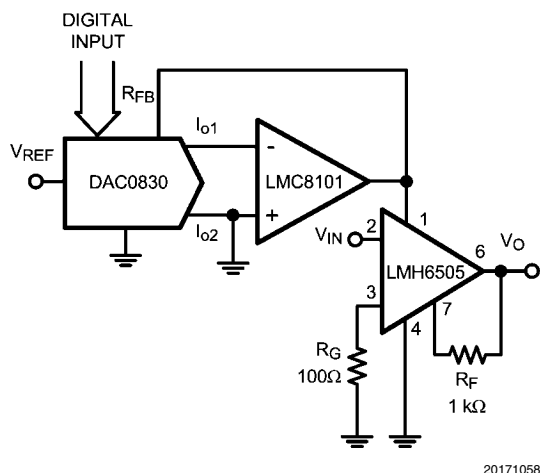


FIGURE 8. Digital Gain Control

### USING THE LMH6505 IN AGC APPLICATIONS

In AGC applications, the control loop forces the LMH6505 to have a fixed output amplitude. The input amplitude will vary over a wide range and this can be the issue that limits dynamic range. At high input amplitudes, the distortion due to the input buffer driving  $R_G$  may exceed that which is produced by the output amplifier driving the load. In the plot, THD vs. Gain, total harmonic distortion (THD) is plotted over a gain range of nearly 35 dB for a fixed output amplitude of  $0.25 V_{PP}$  in the specified configuration,  $R_F = 1 k\Omega$ ,  $R_G = 100\Omega$ . When the gain is adjusted to  $-15$  dB (i.e. 35 dB down from  $A_{VMAX}$ ), the input

amplitude would be  $1.41 V_{PP}$  and we can see the distortion is at its worst at this gain. If the output amplitude of the AGC were to be raised above  $0.25 V_{PP}$ , the input amplitudes for gains 40 dB down from  $A_{VMAX}$  would be even higher and the distortion would degrade further. It is for this reason that we recommend lower output amplitudes if wide gain ranges are desired. Using a post-amp like the LMH6714/LMH6720/LMH6722 family or the LMH6702 would be the best way to preserve dynamic range and yield output amplitudes much higher than  $100 mV_{PP}$ . Another way of addressing distortion performance and its limitations on dynamic range, would be to raise the value of  $R_G$ . Just like any other high-speed amplifier, by increasing the load resistance, and therefore decreasing the demanded load current, the distortion performance will be improved in most cases. With an increased  $R_G$ ,  $R_F$  will also have to be increased to keep the same  $A_{VMAX}$  and this will decrease the overall bandwidth. It may be possible to insert a series RC combination across  $R_F$  in order to counteract the negative effect on BW when a large  $R_F$  is used.

### AUTOMATIC GAIN CONTROL (AGC)

#### Fast Response AGC Loop

The AGC circuit shown in Figure 9 will correct a 6 dB input amplitude step in 100 ns. The circuit includes a two op amp precision rectifier amplitude detector (U1 and U2), and an integrator (U3) to provide high loop gain at low frequencies. The output amplitude is set by  $R_G$ . The following are some suggestions for building fast AGC loops: Precision rectifiers work best with large output signals. Accuracy is improved by blocking DC offsets, as shown in Figure 9.

INCLUDES SCOPE  
PROBE CAPACITANCE

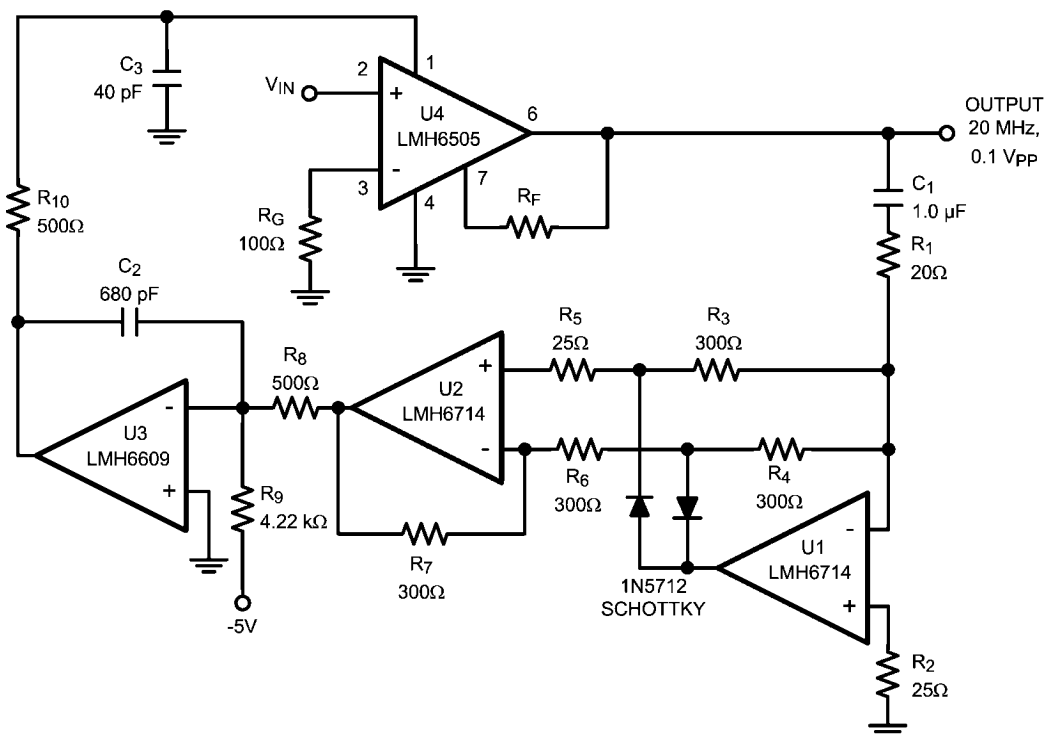


FIGURE 9. Automatic Gain Control Circuit



Signal frequencies must not reach the gain control port of the LMH6505, or the output signal will be distorted (modulated by itself). A fast settling AGC needs additional filtering beyond the integrator stage to block signal frequencies. This is provided in *Figure 9* by a simple R-C filter ( $R_{10}$  and  $C_3$ ); better distortion performance can be achieved with a more complex filter. These filters should be scaled with the input signal frequency. Loops with slower response time, which means longer integration time constants, may not need the  $R_{10} - C_3$  filter.

Checking the loop stability can be done by monitoring the  $V_G$  voltage while applying a step change in input signal amplitude. Changing the input signal amplitude can be easily done with an arbitrary waveform generator.

#### CIRCUIT LAYOUT CONSIDERATIONS & EVALUATION BOARDS

A good high frequency PCB layout including ground plane construction and power supply bypassing close to the package is critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the I<sup>-</sup> input (pin 7) so it is best to keep the node trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect. Capacitance to ground should be minimized by removing the ground plane from under the body of  $R_G$ . Parasitic or load capacitance directly on the output (pin 6) degrades phase margin leading to frequency response peaking.

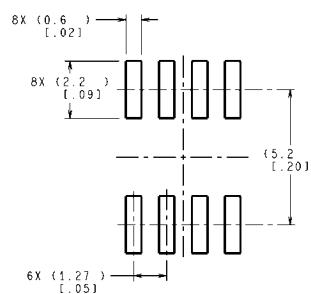
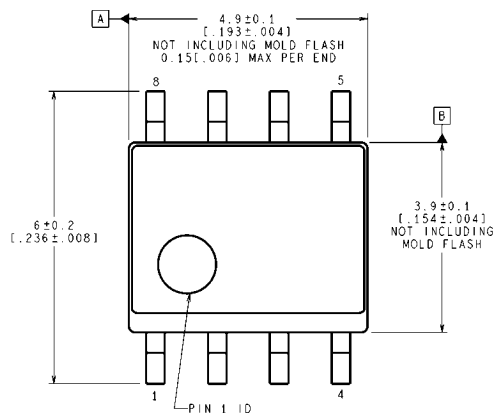
The LMH6505 is fully stable when driving a  $100\Omega$  load. With reduced load (e.g. 1k.) there is a possibility of instability at very high frequencies beyond 400 MHz especially with a capacitive load. When the LMH6505 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g.  $100\Omega$  and 39 pF in series tied between the LMH6505 output and ground).  $C_L$  can also be isolated from the output by placing a small resistor in series with the output (pin 6).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

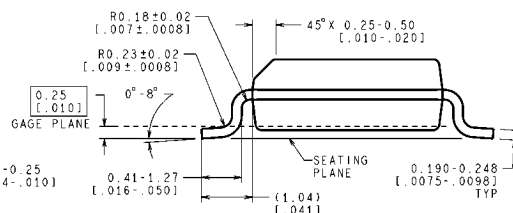
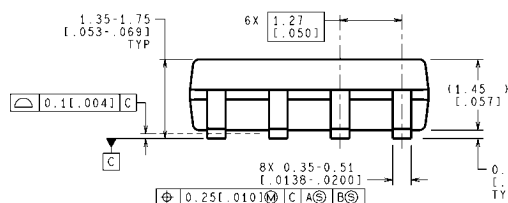
National Semiconductor suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6505	SOIC	LMH730066

The evaluation board can be shipped when a device sample request is placed with National Semiconductor. Evaluation board documentation can be found in the LMH6505 product folder at [www.National.com](http://www.National.com).

**Physical Dimensions** inches (millimeters) unless otherwise noted

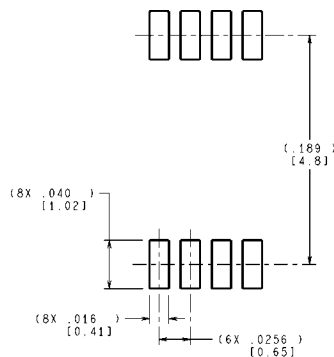
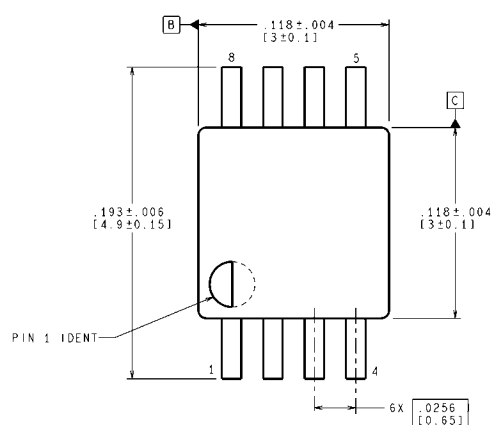
### RECOMMENDED LAND PATTERN



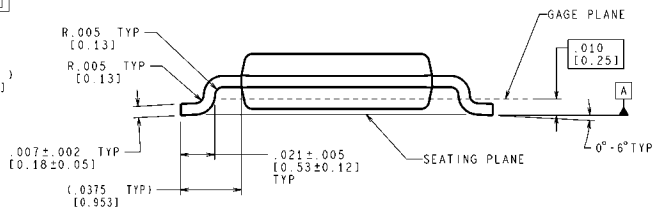
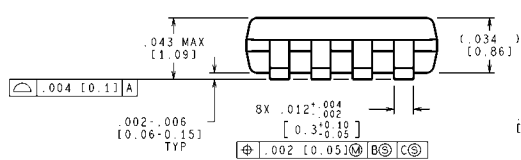
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**8-Pin SOIC**  
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LDOs	<a href="http://www.national.com/ldo">www.national.com/ldo</a>		
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