LMH6518

LMH6518 900 MHz, Digitally Controlled, Variable Gain Amplifier

Literature Number: SNOSB21A

National Semiconductor

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LMH6518
900 MHz, Digitally Controlled, Variable Gain Amplifier

General Description

The LMH6518 is a digitally controlled variable gain amplifier whose total gain can be varied from –1.16 dB to 38.8 dB for a 40 dB range in 2 dB steps. The –3 dB bandwidth is 900 MHz at all gains. Gain accuracy at each setting is typically 0.1 dB. When used in conjunction with a National Semiconductor Gsample/second (Gsps) ADC with adjustable full scale (FS) range, the LMH6518 gain adjustment will accommodate full scale input signals from 6.8 mV_{PP} to 920 mV_{PP} to get 700 mV_{PP} nominal at the ADC input. The Auxiliary output ("+OUT Aux" and "–OUT Aux") follows the Main output and is intended for use in Oscilloscope trigger function circuitry but may have other uses in other applications.

The LMH6518 gain is programmed via a SPI-1 compatible serial bus. A signal path combined gain resolution of 8.5 mdB can be achieved when the LMH6518's gain and the Gsps ADC's FS input are both manipulated. Inputs and outputs are DC-coupled. The outputs are differential with individual Common Mode (CM) voltage control (for Main and Auxiliary outputs) and have a selectable bandwidth limiting circuitry (common to both Main and Auxiliary) of 20, 100, 200, 350, 650, 750 MHz or full bandwidth.

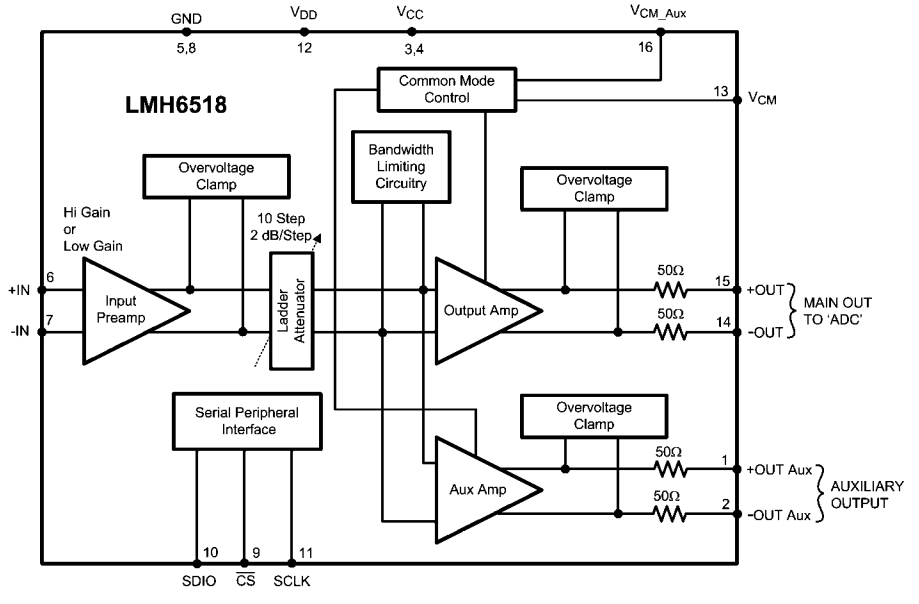
Features

- Gain range 40 dB
- Gain step size 2 dB
- Combined gain resolution with Gsample/second ADC's 8.5 mdB
- Min gain –1.16 dB
- Max gain 38.8 dB
- –3 dB BW 900 MHz
- Rise/fall time <500 ps
- Recovery time <5 ns
- Propagation delay variation 100 ps
- HD2 @ 100 MHz –50 dBc
- HD3 @ 100 MHz –53 dBc
- Input-referred noise (max gain) 0.98 nV/√Hz
- Over-voltage clamps for fast recovery
- Power consumption 1.1W
  - — Auxiliary turned off 0.75W

Applications

- Oscilloscope programmable gain amplifier
- Differential ADC drivers
- High frequency single-ended input to differential conversion
- Precision gain control applications
- Medical applications
- RF/IF applications

Functional Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
Supply Voltage	
V_{CC} (5V nominal)	5.5V
V_{DD} (3.3V nominal)	3.6V
Differential Input	±1V
Input Common Mode Voltage	1V to 4V
V_{CM} and V_{CM_Aux}	2V
SPI Inputs	3.6V
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to 150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings (Note 1)

Supply Voltage	V_{CC} = 5V (±5%)
	V_{DD} = 3.3V (±5%)
Temperature Range	−40°C to 85°C

Thermal Properties

Temperature Range (Note 4)	−40°C to 85°C
Junction-to-Ambient	
Thermal Resistance (θJ_A), LLP (Note 4)	40°C/W

Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Input CM = 2.5V, V_{CM} = 1.2V, V_{CM_Aux} = 1.2V, Single-ended input drive, V_{CC} = 5V, V_{DD} = 3.3V, R_L = 100Ω differential (both Main & Auxiliary Outputs), V_{OUT} = 0.7 V_{PP} differential (both Main & Auxiliary Outputs), both Main and Auxiliary Output Specifications, full bandwidth setting, gain = 18.8 dB (Preamp LG, 0 dB ladder attenuation), Full Power setting (Note 11). See "*Definition of Terms and Specifications*" section for abbreviations used in the datasheet. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Dynamic Performance						
LSBW	−3 dB Bandwidth	All Gains		900		MHz
Peaking	Peaking	All Gains		1		dB
GF_0.1 dB	±0.1 dB Gain Flatness	All Gains		150		MHz
GF_1 dB	±1 dB Gain Flatness	All Gains		400		MHz
TRS	Rise Time			460		ps
TRL	Fall Time			450		
OS	Overshoot	Main Output		9		%
t_{s_1}	Settling Time	Main Output, ±0.5%		10		ns
t_{s_2}		Main Output, ±0.05%		14		
t_recover	Recovery Time (Note 6)	All Gains		<5		ns
P_D	Propagation Delay	V_{OUT} = 0.7 V_{PP}, All Gains		1.2		ns
P_{D_VAR}	Propagation Delay Variation	Gain Varied		100		ps
Noise, Distortion, and RF Specifications						
e_{n_1}	Input Noise Spectral Density	Max Gain, 10 MHz		0.98		$nV/\sqrt{Hz}$
e_{n_2}		Preamp LG and 0 dB Ladder, 10 MHz		4.1		
e_{no_1}	RMS Output Noise	Max Gain, 100 Hz to 400 MHz		1.7		mV
e_{no_2}		Preamp LG, 0 dB Ladder, 100 Hz to 400 MHz		940		µV
NF_1	Noise Figure	Max Gain, R_S = 50Ω each Input, 10 MHz		3.8		dB
NF_2		Preamp LG, 0 dB Ladder, R_S = 50Ω each Input, 10 MHz		13.5		
HD2/ HD3_1	2nd/ 3rd Harmonic Distortion (Note 12)	Main Output, 100 MHz, All Gains		−50/ −53		dBc
HD2/ HD3_2		Auxiliary Output, 100 MHz, All Gains		−48/ −50		
HD2/ HD3_3		Main Output, 250 MHz, All Gains		−44/ −50		
HD2/ HD3_4		Auxiliary Output, 250 MHz, All Gains		−42/ −42		

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
IMD3	Intermodulation Distortion (Note 12)	f = 250 MHz, Main output		–65		dBc
OIP3_1	Intermodulation Intercept (Note 12)	Main Output, 250 MHz		26		dBm
P_1dB_main	–1 dB Compression	Main Output, 250 MHz, 0 dB Ladder		1.8		V_{PP}
		Main Output, 250 MHz, 20 dB Ladder		1.0		
P_1dB_aux		Auxiliary Output, 250 MHz, 0 dB Ladder		1.65		
		Auxiliary Output, 250 MHz, 20 dB Ladder		1.0		
Gain Parameters						
$A_{V\_DIFF\_MAX}$	Max Gain		38.1	38.8	39.5	dB
$A_{V\_DIFF\_MIN}$	Min Gain		–1.91	–1.16	–0.40	dB
Gain_Step	Gain Step Size	All Gains including Preamp Step	1.8	2	2.2	dB
	Gain Step Size with ADC (See Application Information section)	ADC FS Adjusted		8.5		mdB
Gain_Range	Gain Range		39	40	41	dB
$TC\_A_{V\_DIFF}$	Gain Temp Coefficient (Note 9)	All Gains		–0.8		mdB/°C
$Gain\_A_{CC}$	Absolute Gain Accuracy	Compared to theoretical from Max Gain in 2 dB steps	0.75	—	+0.75	dB
Matching						
Gain_match	Gain Matching Main/Auxiliary	All Gains		±0.1	±0.2	dB
BW_match	–3 dB Bandwidth Matching Main/ Auxiliary	All Gains		5		%
RT_match	Rise Time Matching Main/ Auxiliary	All Gains		5		%
PD_match	Propagation Delay Matching Main/ Auxiliary	All Gains		100		ps
Analog I/O						
CMRR_1	CM Rejection Ratio (see definition)	Preamp HG, 0 dB Ladder, 1.9V < CMVR < 3.1V	45	86		dB
CMRR_2		Preamp LG, 0 dB Ladder, 1.9V < CMVR < 3.1V	40	55		
CMVR_1	Input Common Mode Voltage Range	Preamp HG, All Ladder Steps, CMRR ≥ 45 dB	1.9	—	3.1	V
CMVR_2		Preamp LG, , All Ladder Steps, CMRR ≥ 40 dB	1.9	—	3.1	
$\lvert\Delta V_{O\_CM}\rvert\Delta_{I\_CM}\rvert$		All Gains, 2V < CMVR < 3V	–60	–100		dB
CMRR_CM	CM Rejection Ratio relative to VCM (see definition)	Preamp LG, 0 dB		101		dB
Z_{in_diff}	Differential Input Impedance	All Gains		150||1.5		KΩ || pF
Z_{in_CM}	CM Input impedance	Preamp HG		420||1.7		
		Preamp LG		900||1.7		
FS_{OUT1}	Full Scale Voltage Swing	Main Output, THD @ 100 MHz ≤ –40 dBc, All Gains	770 (Note 3)	800		mV_{PP}
FS_{OUT2}		Main Output, Clamped, 0 dB Ladder		1800	1960	
FS_{OUT3}		Auxiliary Output, THD @ 100 MHz ≤ –40 dBc All Gains	770 (Note 3)	800		
FS_{OUT4}		Auxiliary Output, Clamped, 0 dB Ladder		1600	1760	

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
V_{OUT_MAX1}	Voltage range at each output pin (clamped)	Main Output, All gains, V_{CM} = 1.2V	0.5		1.8	V
V_{OUT_MAX2}		Auxiliary Output, All Gains, V_{CM} = 1.2V	0.8		2.2	
V_{OUT_MAX3}		Main Output, All Gains, V_{CM} = 1.45V			2.05	
V_{OUT_MAX4}		Auxiliary output, All gains, V_{CM} = 1.45V			2.45	
Z_{OUT_DIFF}	Differential Output Impedance	All Gains	92	100	108	Ω
V_{OOS}	Output Offset Voltage	All Gains		±15	±40	mV
V_{OOS_shift1}	Output Offset Voltage Shift	Preamp LG to Preamp HG		13.7		mV
V_{OOS_shift2}		All Gains, Excluding Preamp Step		12.7		
TCV_{OOS}	Output Offset Voltage Drift (Note 9)	Preamp HG, 0 dB Ladder		–24		µV/°C
		Preamp LG, 0 dB Ladder		–7		
I_B	Input Bias Current (Note 10)			+40	+100 **+140**	µA
V_{OCM}	Output CM Voltage Range	All Gains	**0.95**	1.20	**1.45**	V
V_{OS_CM}	Output CM Offset Voltage	All Gains		±15	±30	mV
$TC\_V_{OS\_CM}$	CM Offset Voltage Temp Coefficient	All Gains		+55		µV/°C
BAL_Error_DC	Output Gain Balance Error	DC, $\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$		–78		dB
BAL_Error_AC		250 MHz, $\frac{v_{O\_CM}}{v_{OUT}}$		–45		
PB	Phase Balance Error (See Definition)	250 MHz		±0.8		deg
PSRR	Differential Power Supply Rejection (see Definition)	Preamp HG, 0 dB Ladder	–60	–87		dB
		Preamp HG, 0 dB Ladder	–50	–70		
PSRR_CM	CM Power Supply Rejection (see Definition)	Preamp LG, 0 dB	–55	–71		dB
V_{CM_I}	V_{CM} Input Bias Current (Note 10)	All Gains		±1	±10 **±20**	nA
$V_{CM\_AUX\_I}$	V_{CM_AUX} Input Bias Current (Note 10)	All Gains		±1	±10 **±20**	nA
Digital I/O & Timing						
V_{IH}	Input Logic High		**V_{DD}-0.6**			V
V_{IL}	Input Logic Low				**0.5**	V
V_{OH}	Output Logic High			V_{DD}		V
V_{OL}	Output Logic Low			0		V
R_{Hi_Z}	Output Resistance	High Impedance Mode		5		MΩ
I_in	Input Bias Current			<1		µA
F_{SCLK}	SCLK Rate				10	MHz
F_{SCLK_DT}	SCLK Duty Cyle		45	50	55	%
T_S	SDIO Setup Time		25			ns
T_H	SDIO Hold Time		25			ns
T_{CES}	$\overline{CS}$ Enable Setup Time	From $\overline{CS}$ asserted to rising edge of SCLK	25			ns
t_{CDS}	$\overline{CS}$ Disable Setup Time	From $\overline{CS}$ de-asserted to rising edge of SCLK	25			ns
T_{IAG}	Inter-Acess Gap		3			Cycles of SCLK

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Power Requirements						
I_{S1}	Supply Current	V_{CC}	195	210	225 **230**	mA
I_{S1_off}		V_{CC} Aux off		150	165 **170**	mA
I_{DD}		V_{DD}		180	350 **400**	µA
Bandwidth Limiting Filter Specifications						
Filter	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Units**
20 MHz	Pass Band Tolerance (All Gains)	–3 dB Bandwidth		–0, +20		%
100 MHz	Pass Band Tolerance (All Gains)	–3 dB Bandwidth		–0, +20		%
200 MHz	Pass Band Tolerance (All Gains)	–3 dB Bandwidth		–0, +20		%
350 MHz	Pass Band Tolerance (Preamp LG, 0 dB Ladder)	–3 dB Bandwidth		±10		%
	Pass Band Tolerance (All Gains)			±25		
650 MHz	Pass Band Tolerance (Preamp LG, 0 dB Ladder)	–3 dB Bandwidth		±10		%
	Pass Band Tolerance (All Gains)			±25		
750 MHz	Pass Band Tolerance (Preamp LG, 0 dB Ladder)	–3 dB Bandwidth		±10		%
	Pass Band Tolerance (All Gains)			±25		

Definition of Terms and Specifications

1.	A_{V_CM} (dB)	Change in output offset voltage (ΔV_{OOS}) with respect to the change in input common mode voltage (ΔV_{I_CM})
2.	A_{V_DIFF} (dB)	Gain with 100Ω differential load
3.	CM	Common Mode
4.	CMRR (dB)	Common Mode rejection defined as: A_{V_DIFF} (dB) - A_{V_CM} (dB)
5.	CMRR_CM	Common Mode rejection relative to V_{CM} defined as: $\Delta V_{OOS} / \Delta V_{CM}$
6.	HG	Preamp High Gain
7.	Ladder	Ladder Attenuator setting (0-20 dB)
8.	LG	Preamp Low Gain
9.	Max Gain	Gain = 38.8 dB
10.	Min Gain	Gain = –1.16 dB
11.	+Out	Positive Main Output
12.	–Out	Negative Main Output
13.	+Out Aux	Positive Auxiliary Output
14.	–Out Aux	Negative Auxiliary Output
15.	PB	Phase Balance defined as the phase difference between the complimentary outputs relative to 180°
16.	PSRR	Input referred V_{OOS} shift divided by change in V_{CC}
17.	PSRR_CM	Output common mode voltage change (ΔV_{O_CM}) with respect to V_{CC} voltage change (ΔV_{CC})
18.	V_{CM}	Input pin voltage that sets Main output CM
19.	V_{CM_Aux}	Input pin voltage that sets Auxiliary output CM
20.	V_{I_CM}	Input CM voltage (average of +IN and –IN)
21.	ΔV_{IN} (V)	Differential voltage across device inputs

22.	V_{OOS}	DC offset voltage. Differential output voltage measured with inputs shorted together to $V_{CC}/2$
23.	V_{O_CM}	Output common mode voltage (DC average of V_{+OUT} and V_{-OUT})
24.	V_{OS_CM}	CM offset voltage: V_{O_CM} - V_{CM}
25.	ΔV_{O_CM}	Variation in output common mode voltage (V_{O_CM})
26.	$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$	Balance Error. Measure of the output swing balance of "+OUT" and "–OUT", as reflected on the output common mode voltage (V_{O_CM}), relative to the differential output swing (V_{OUT}). Calculated as output common mode voltage change (ΔV_{O_CM}) divided by the output differential voltage change (ΔV_{OUT}, which is nominally around 700 mV_{PP})
27.	ΔV_{OUT}	Change in differential output voltage (Corrected for DC offset (V_{OOS}))

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: Guaranteed by design.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow. Package should be soldered unto a 6.8 mm^2 copper area as shown in the "recommended land pattern" shown in the package drawing.

Note 5: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 6: Recovery time" is the slower of the Main and Auxiliary outputs. Output swing of 700 mV_{PP} shifted up or down by 50% (0.35V) by introducing an offset. Measured values correspond to the time it takes to return to within ±1% of 0.7 V_{PP} (±7 mV).

Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 8: Limits are 100% production tested at 25°C unless otherwise specified. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 10: Positive current is current flowing into the device.

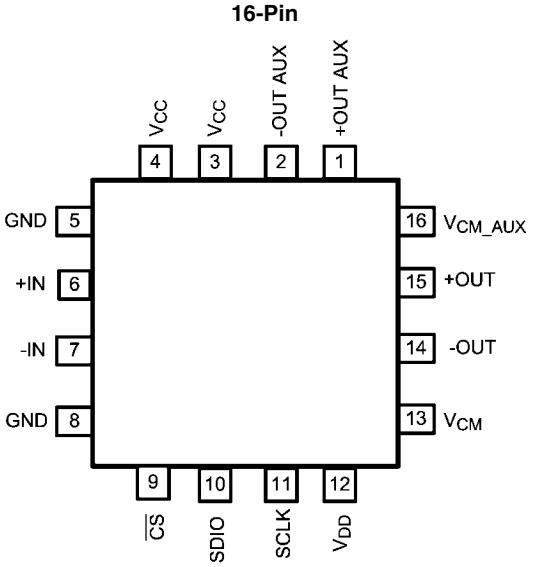
Note 11: "Full Power" setting is with Auxiliary output turned on.

Note 12: Distortion data taken under single ended input condition.

Pin Out

Pin Out	Function
P1 = +OUT Aux	Auxiliary positive output
P2 = –OUT Aux	Auxiliary negative output
P3 = V_{CC} (5V)	Analog power supply
P4 = V_{CC} (5V)	Analog power supply
P5 = GND	Ground, electrically connected to the LLP heat sink
P6 = +IN	Positive Input
P7 = –IN	Negative Input
P8 = GND	Ground, electrically connected to the LLP heat sink
P9 = $\overline{CS}$	SPI interface, Chip Select, Active low
P10 = SDIO	SPI interface, Serial Data Input/Output
P11 = SCLK	SPI interface, Clock
P12 = V_{DD} (3.3V)	Digital power supply
P13 = V_{CM}	Input from ADC to control main output CM
P14 = –OUT	Main negative output
P15 = +OUT	Main positive output
P16 = V_{CM_Aux}	Input to control auxiliary output CM

Connection Diagram



Top View

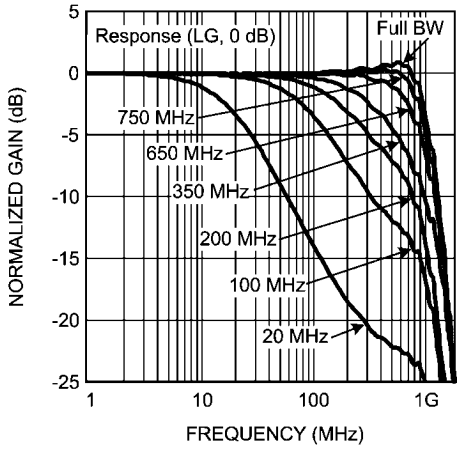
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin LLP	LMH6518SQ	L6518SQ	1k Units Tape and Reel	SQA16A
	LMH6518SQE		250 Units Tape and Reel	
	LMH6518SQX		4.5k Units Tape and Reel	

Typical Performance Characteristics

Unless otherwise specified, Input CM = 2.5V, V_{CM} = 1.2V, $V_{CM\ AUX}$ = 1.2V, Single-ended input drive, V_{CC} = 5V, V_{DD} = 3.3V, R_L = 100Ω differential (both Main & Auxiliary Outputs), V_{OUT} = 0.7 V_{PP} differential (both Main and Auxiliary Outputs), Main output specification (Auxiliary is labeled "Auxiliary"), full bandwidth setting, gain = 18.8 dB (Preamp LG, 0 dB ladder attenuation), Full Power setting (Note 11).

Response (LG, 0 dB)



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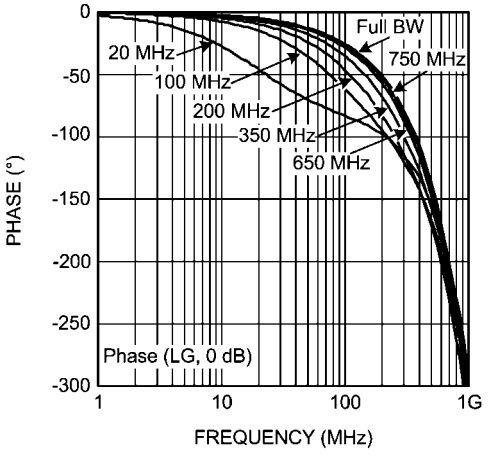
Phase (LG, 0 dB)



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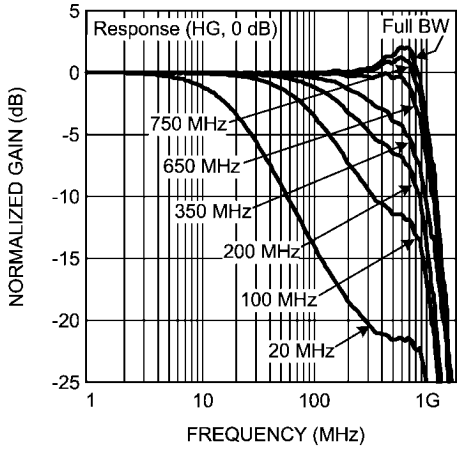
Response (HG, 0 dB)



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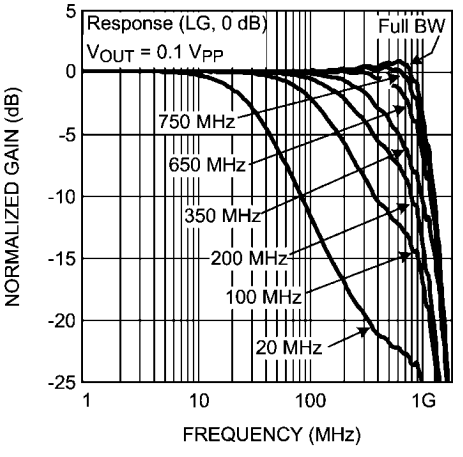
Small Signal Response (LG, 0 dB)



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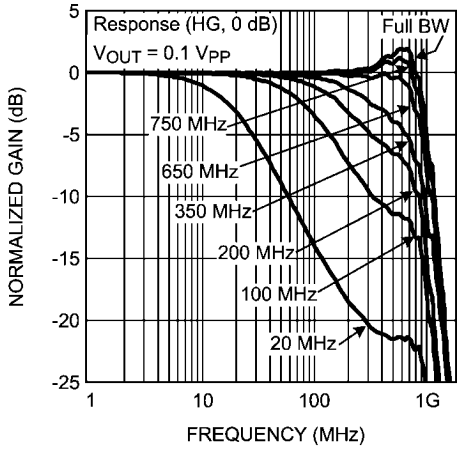
Small Signal Response (HG, 0 dB)



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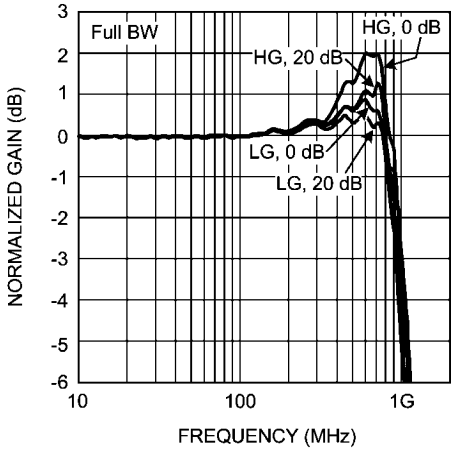
Response vs. Gain



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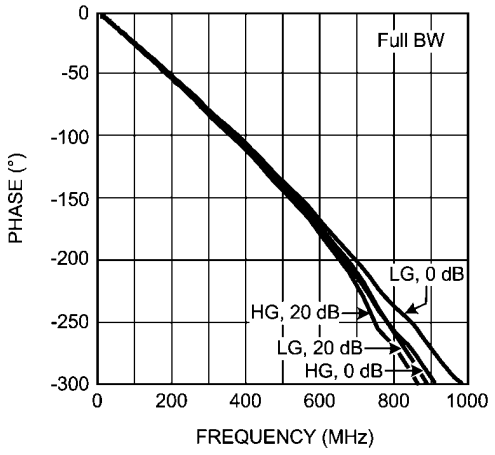
Phase vs. Gain



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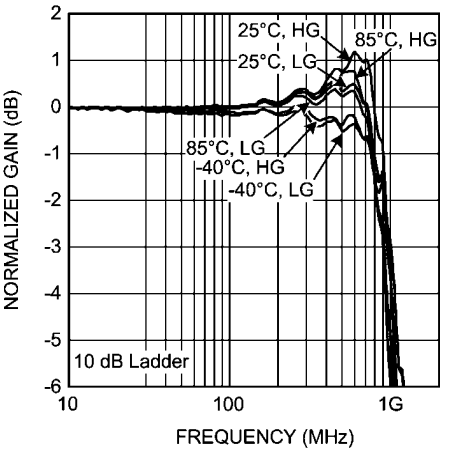
Response Over Temperature



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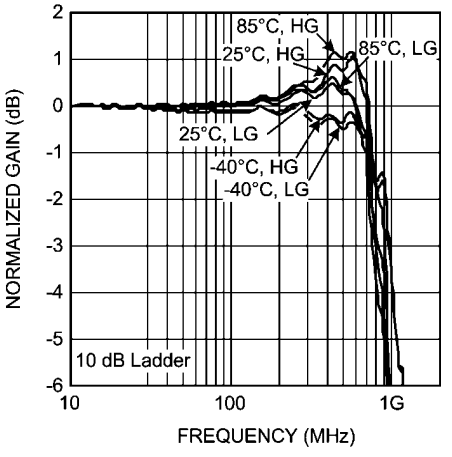
Auxiliary Response Over Temperature



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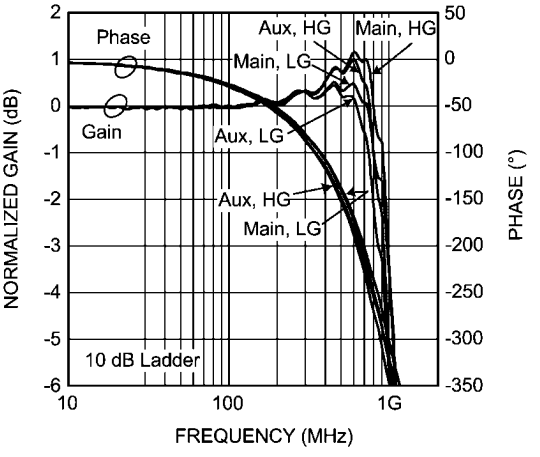
Main vs. Auxiliary Response



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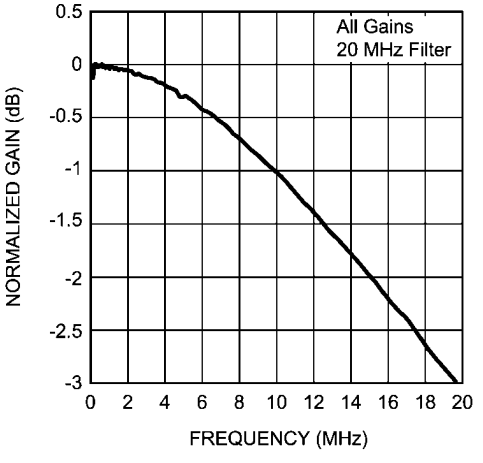
Response vs. Gain



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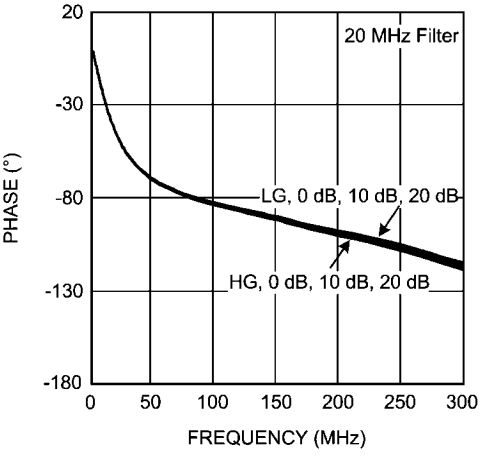
Phase vs. Gain



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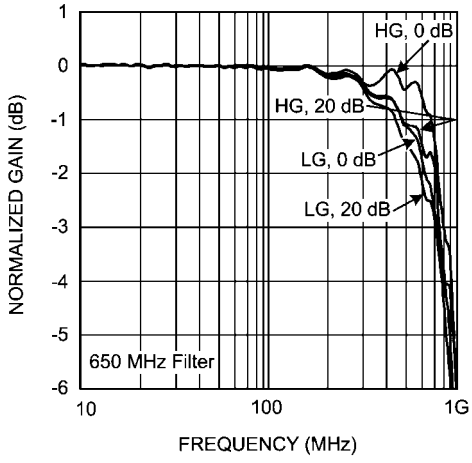
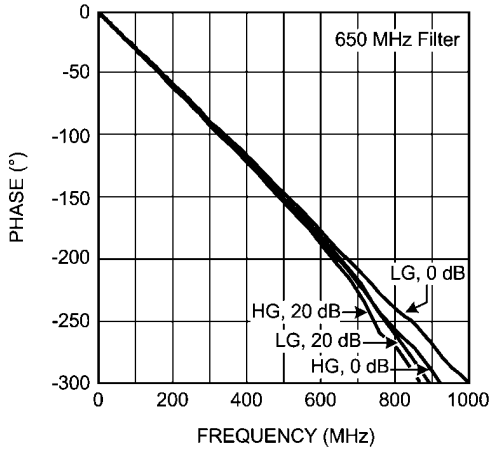
Response vs. Gain



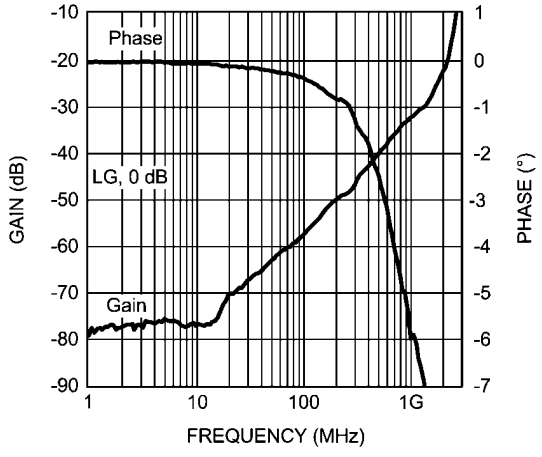
30068849

Phase vs. Gain



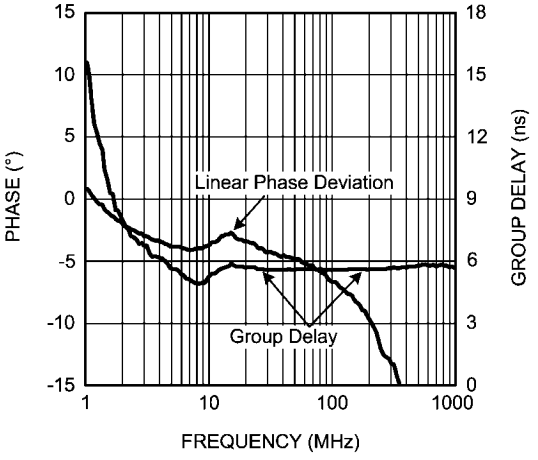
30068850

Balance Error



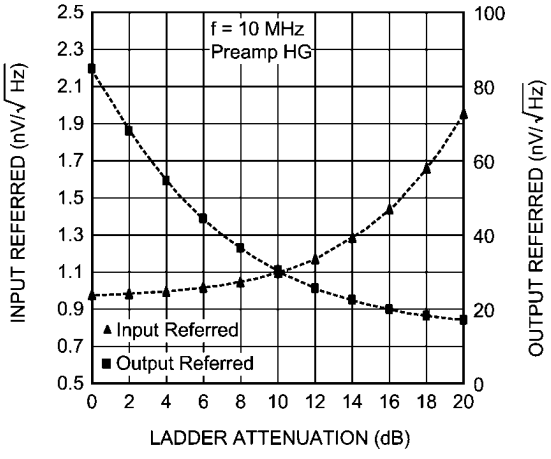
30068853

Linear Phase Deviation and Group Delay



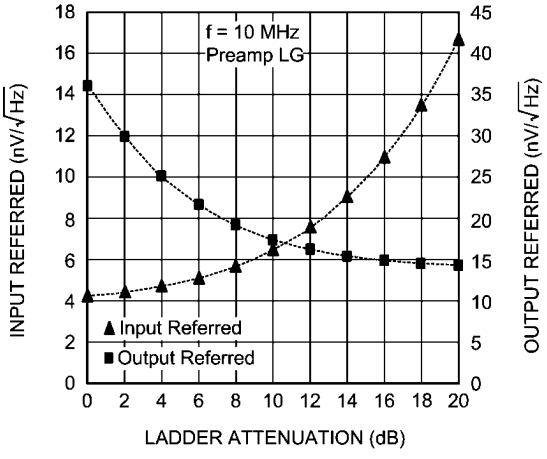
30068840

Noise vs. Ladder Attenuation



30068807

Noise vs. Ladder Attenuation



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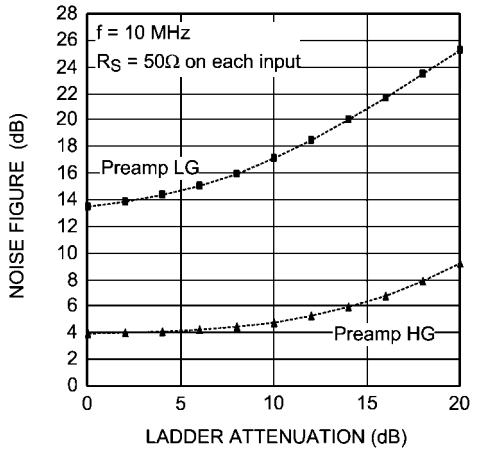
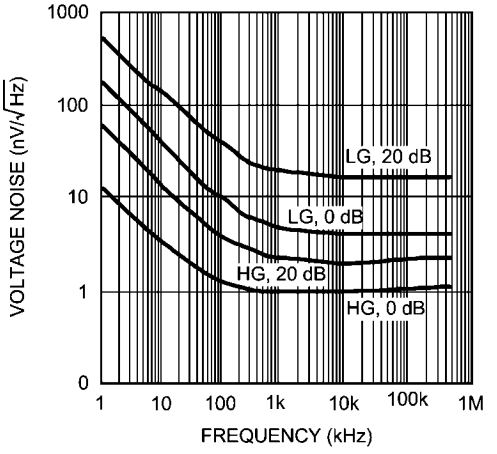
Noise Figure vs. Gain



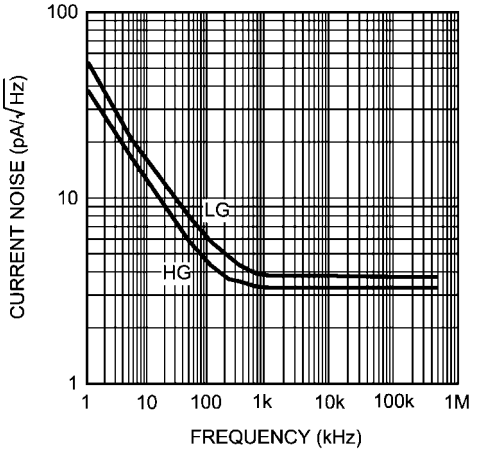
30068838

Input Voltage Noise vs. Frequency



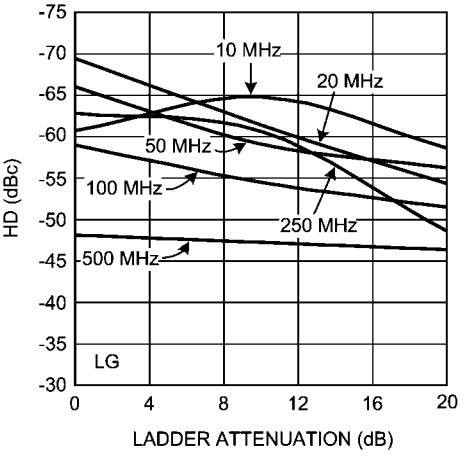
30068878

Input Current Noise vs. Frequency



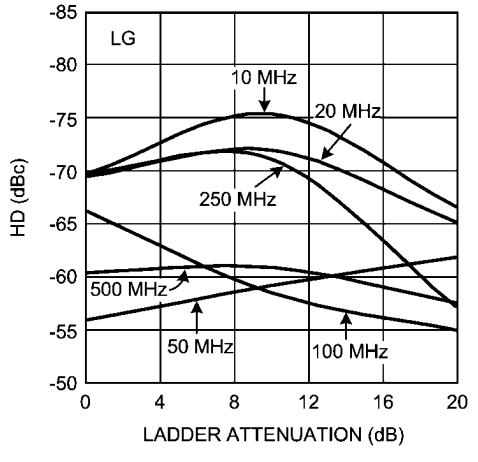
30068879

HD2 vs. Ladder Attenuation



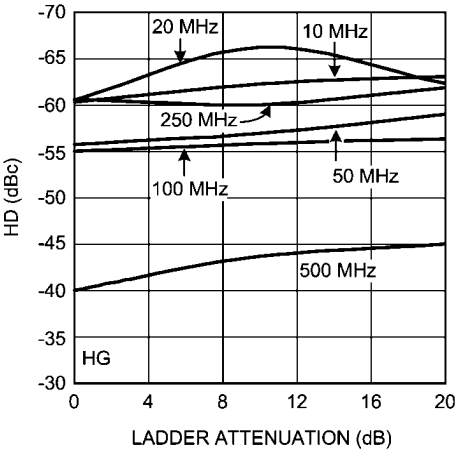
30068874

HD3 vs. Ladder Attenuation



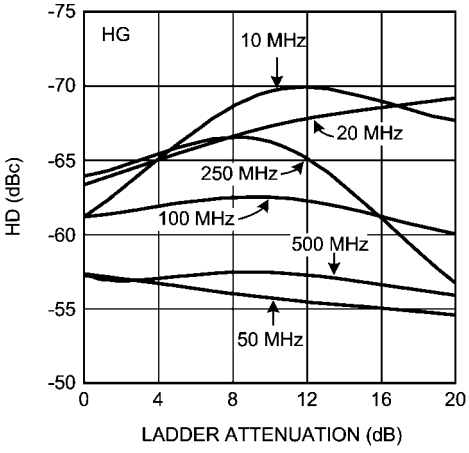
30068875

HD2 vs. Ladder Attenuation



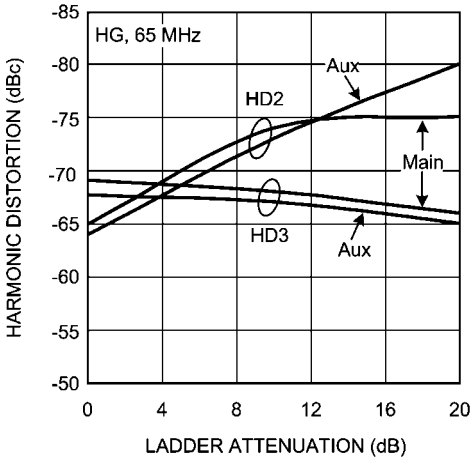
30068872

HD3 vs. Ladder Attenuation



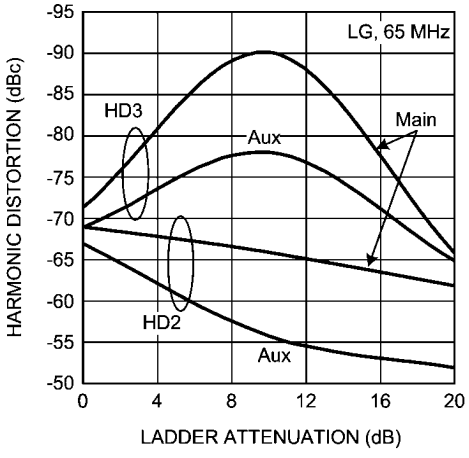
30068873

Main and Auxiliary Distortion Comparison



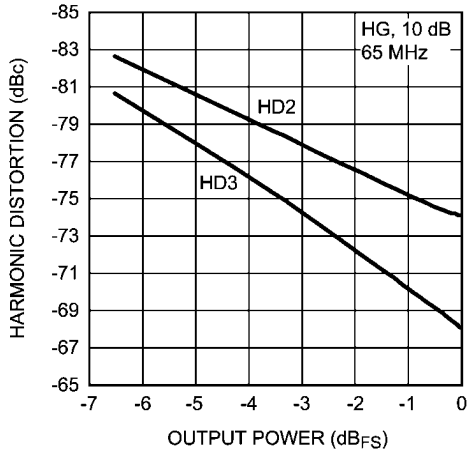
30068896

Main and Auxiliary Distortion Comparison



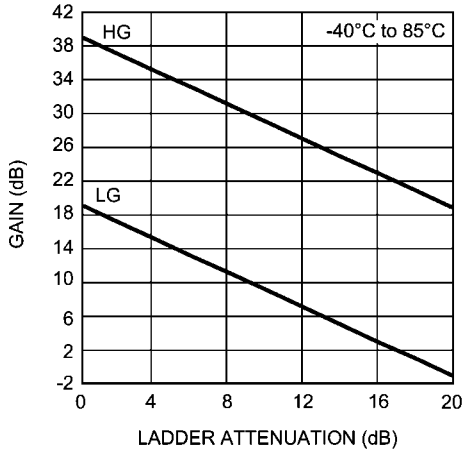
30068897

Distortion vs. Output Power



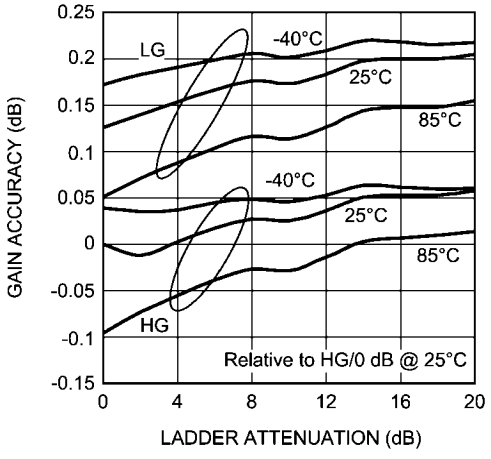
30068898

Gain vs. Ladder Attenuation



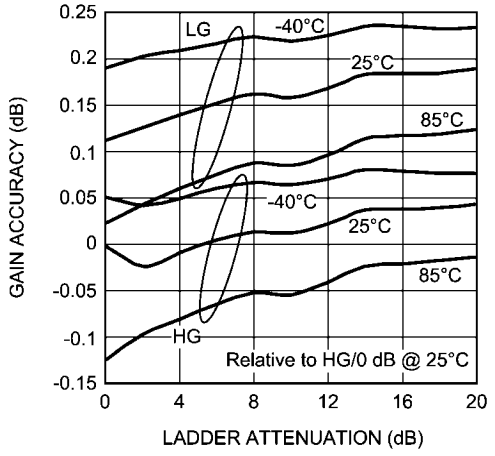
30068871

Gain Accuracy vs. Ladder Attenuation



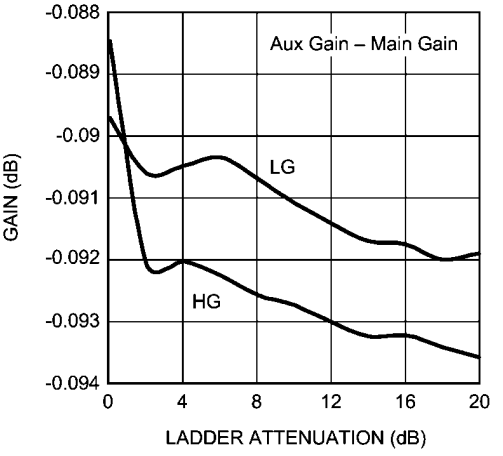
30068869

Auxiliary Gain Accuracy vs. Ladder Attenuation



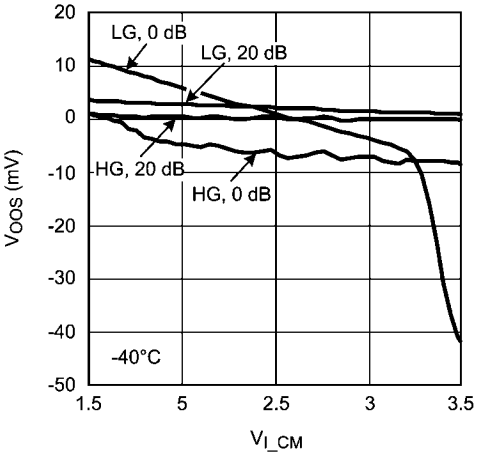
30068870

Gain Matching vs. Ladder Attenuation



30068868

A_{V_CM}



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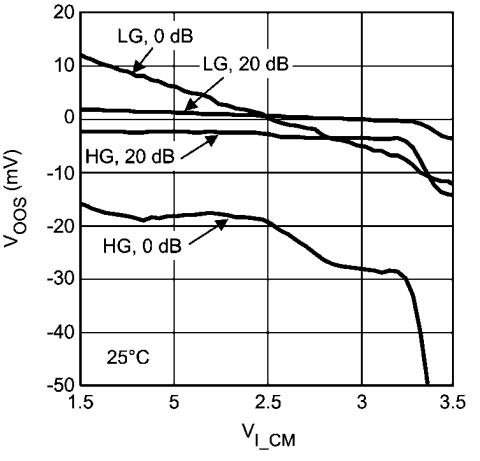
A_{V_CM}



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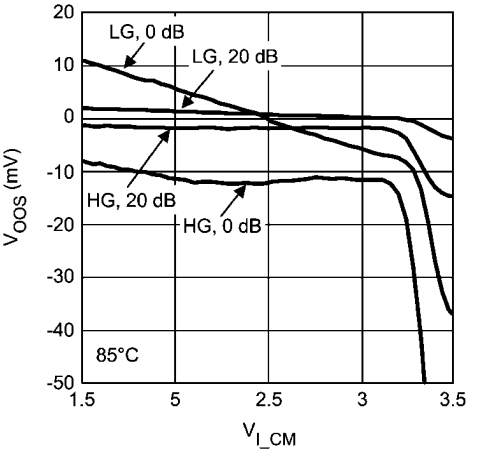
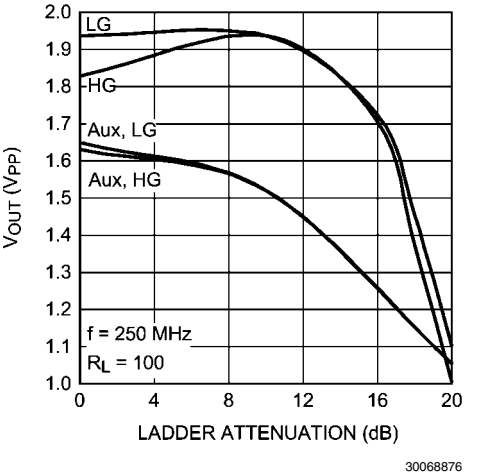
A_{V_CM}



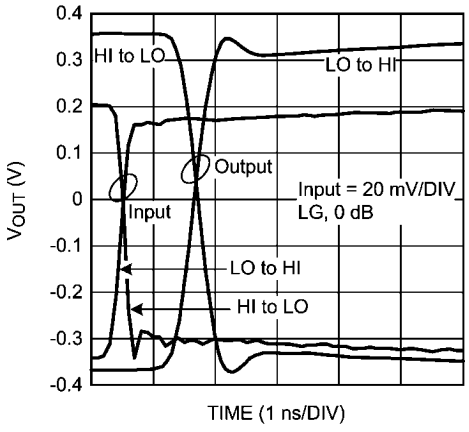
30068859

–1 dB Compression vs. Ladder Attenuation



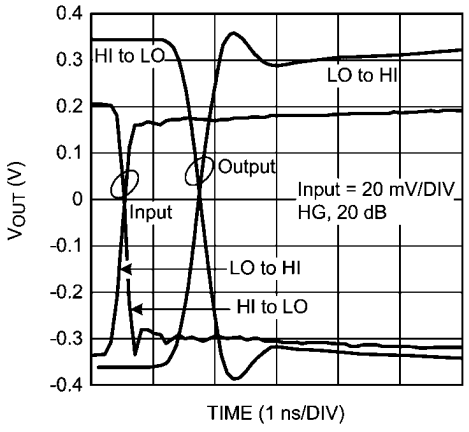
30068876

Step Response



30068889

Step Response



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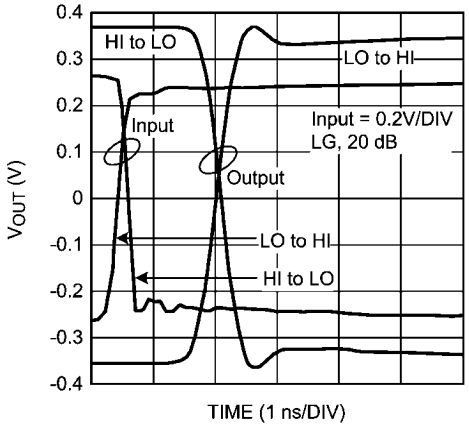
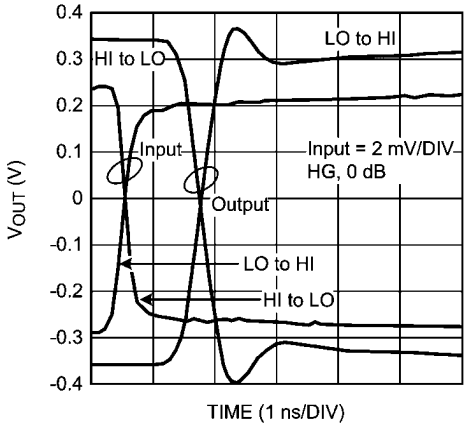
Step Response



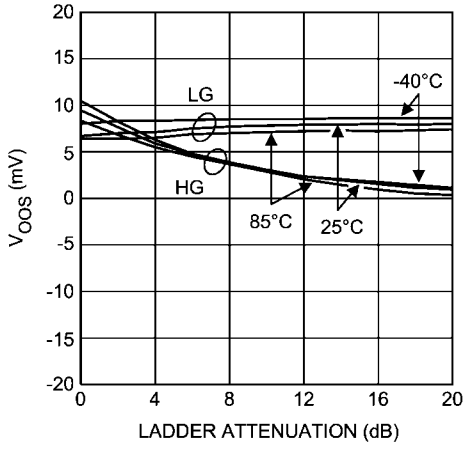
30068891

Step Response



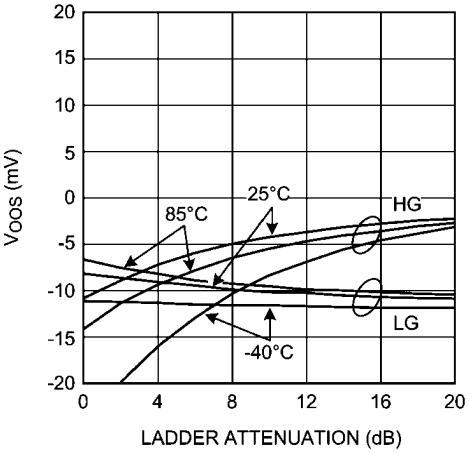
30068892

Output Offset Voltage (Typical Unit 1)



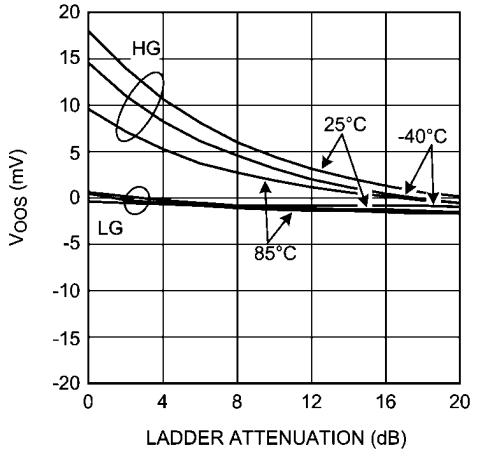
30068865

Output Offset Voltage (Typical Unit 2)



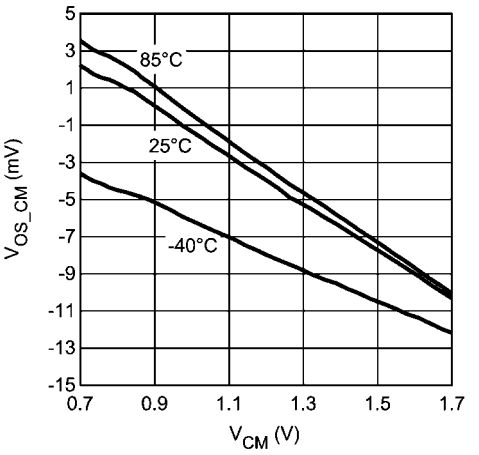
30068866

Output Offset Voltage (Typical Unit 3)



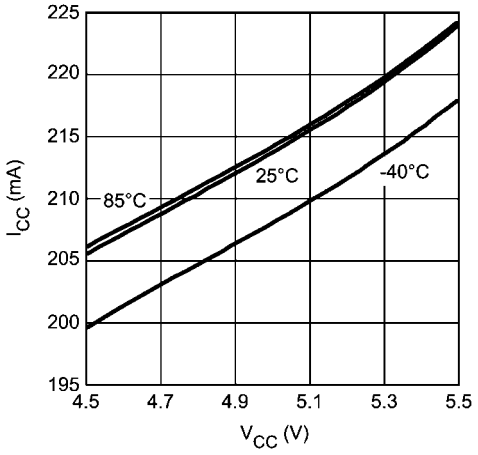
30068867

V_{OS_CM} vs. V_{CM}



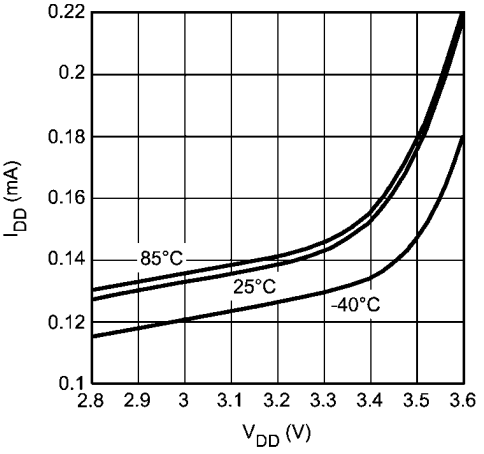
30068860

Supply Current vs. Supply Voltage



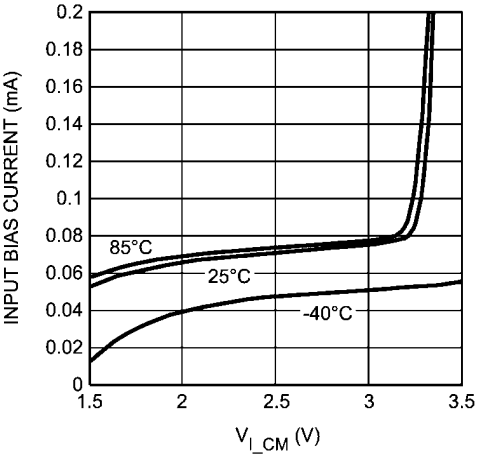
30068863

Supply Current vs. Supply Voltage



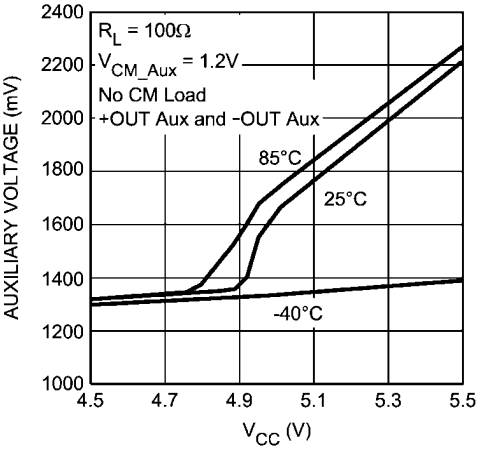
30068864

Input Bias Current vs. Input CM



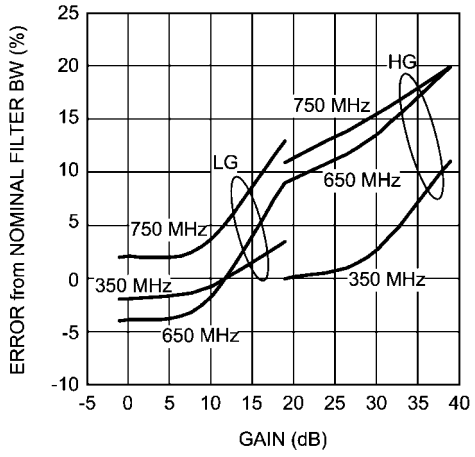
30068861

Auxiliary Output Voltage (Hi-Z Mode)



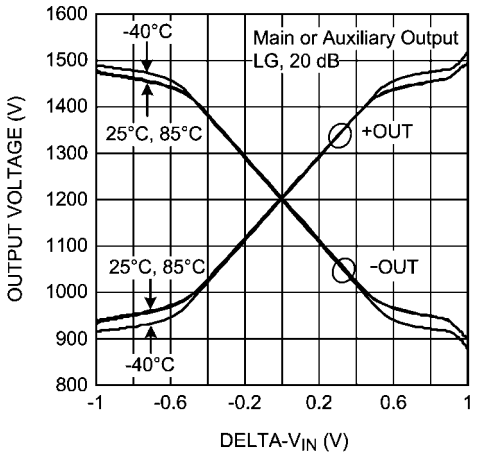
30068862

Filter BW vs. Gain



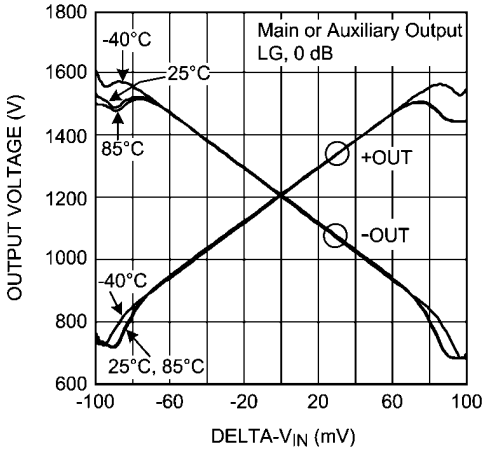
30068895

Output vs. Input



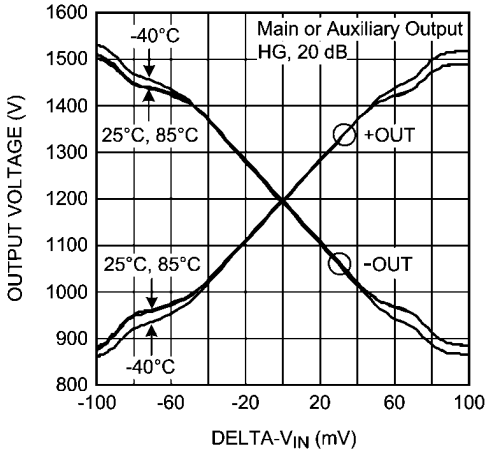
30068880

Output vs. Input



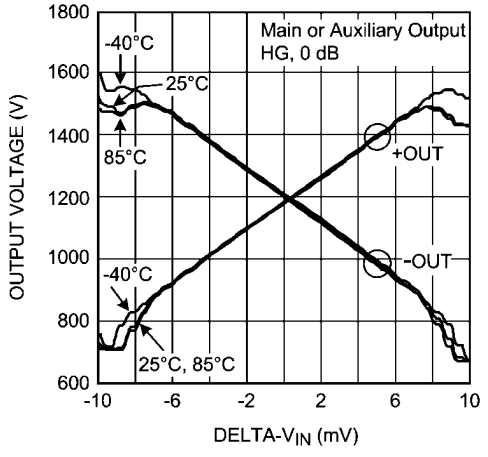
30068881

Output vs. Input



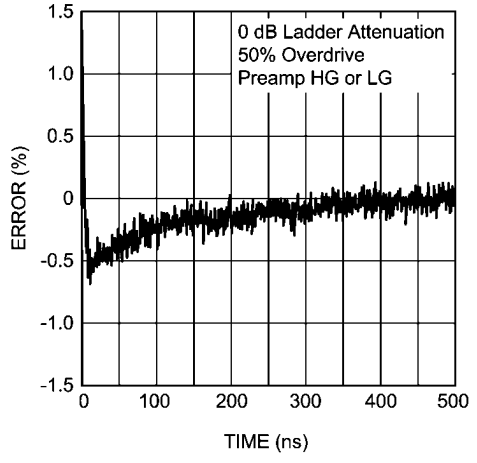
30068882

Output vs. Input



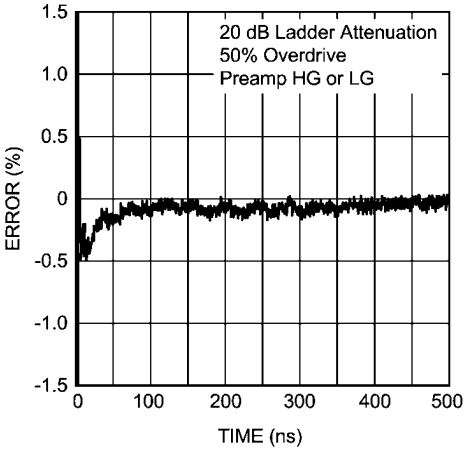
30068883

Overdrive Recovery Time (Return to Zero)



30068893

Overdrive Recovery Time (Return to Zero)



Applications Information

FUNCTIONAL DESCRIPTION AND DYNAMIC RANGE IN OSCILLOSCOPE APPLICATIONS

Here is a block diagram of the LMH6518's Main Output signal path:

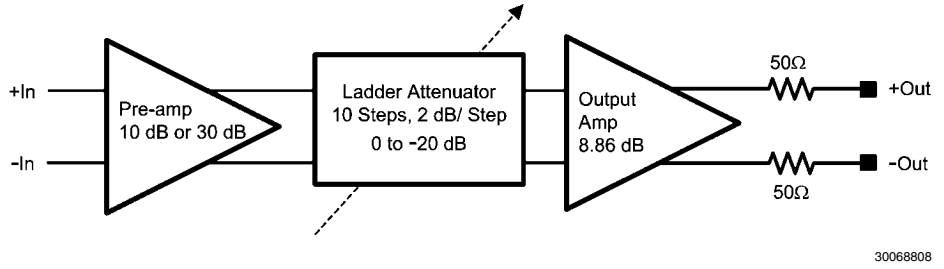


FIGURE 1. LMH6518 Signal Path Block Diagram

The Auxiliary output (not shown) uses another but similar Output Amp that taps into the Ladder Attenuator output. In this document, Preamp gain of 30 dB is referred to as "Preamp HG" (High Gain) and Preamp gain of 10 dB as "Preamp LG" (Low Gain).

The LMH6518's 2 dB/step gain resolution and 40 dB adjustment range (from −1.16 dB to 38.8 dB) allows this device to be used with the National GSample/second ADCs which have Full Scale, FS, adjustment (through their Extended Control Mode or ECM) to provide near-continuous variability (8.5 mdB resolution) to cover a 42.6 dB

$$(20 \times \log \frac{920\ mV_{PP}}{6.8\ mV_{PP}} = 42.6\ dB)$$

FS input range. The National Semiconductor GSample/second ECM control allows the ADC FS to be set using the ADC SPI bus. The ADC FS voltage range is from 560 mV to 840 mV with 9 bits of FS voltage control.

The ADC ECM gain resolution can be calculated as follows:

$$\text{Gain Resolution} = 20 \log \frac{0.56 + \left(\frac{0.84 - 0.56}{2 \times 512}\right)}{0.56 - \left(\frac{0.84 - 0.56}{2 \times 512}\right)} = 8.5\ mdB$$

The *recommended* ADC FS operating range is, however, narrower and it is from 595 mV to 805 mV with 700 mV_{PP} as the mid-point. Raising the value of ADC FS voltage is tantamount to reducing the signal path gain to accommodate a larger input and vice versa, thus providing a method of gain fine-adjust. The ADC ECM gain adjustment is −1.21 dB

$$(= 20 \times \log \frac{700\ mV}{805\ mV}) \text{ to } +1.41\ dB$$

$$(= 20 \times \log \frac{700\ mV}{595\ mV})$$

Because the ADC FS fine-adjust range of 2.62 dB (= 1.41 dB + 1.21 dB) is larger than the LMH6518's 2 dB/step resolution, there is always at least one LMH6518 gain setting to accom-

modate any FS signal from 6.8 mV_{PP} to 920 mV_{PP}, at the LMH6518 input, with 0.62 dB (= 2.62-2) overlap.

Assuming a nominal 0.7V_{PP} output, the LMH6518's minimum FS input swing is limited by the maximum signal path gain possible and vice versa:

$$\text{Minimum LMH6518 FS Input} = \frac{0.7\ V_{PP}}{10^{\frac{(38.8 + 1.41)\ dB}{20}}} = 6.8\ mV_{PP}$$

(or 8 mV_{PP} with no ADC fine adjust)

$$\text{Maximum LMH6518 FS Input} = \frac{0.7\ V_{PP}}{10^{\frac{(-1.16 - 1.21)\ dB}{20}}} = 920\ mV_{PP}$$

(or 800 mV_{PP} with no ADC FS adjust)

To accommodate a higher FS input, an additional attenuator is needed before the LMH6518. This front-end attenuator is shown in the *Figure 6* block diagram with its details shown in *Figure 15*. The highest minimum attenuation level is determined by the largest FS input signal (FS_{max}):

$$\text{Attenuation (dB)} = 20 \times \log \frac{FS_{MAX}\ (V_{PP})}{800\ mV_{PP}}$$

So, to accommodate 80 V_{PP}, 40 dB minimum attenuation is needed before the LMH6518.

In a typical oscilloscope application, the voltage range encountered is from 1 mV/DIV to 10 V/DIV with 8 vertical divisions visible on the screen. One of the primary concerns in a digital oscilloscope is SNR which translates to display trace width/ thickness. Typically, oscilloscope manufacturers need the noise level to be low enough so that the "no-input" visible trace width is less than 1% of FS. Experience has shown that this corresponds to a minimum SNR of 52 dB.

The factors that influence SNR are:

- Scope front end noise (Front-end attenuator + scope probe Hi-Z buffer which is discussed later in this document and shown in *Figure 6*)
- LMH6518
- ADC

LMH6518 related SNR factors are:

- Bandwidth
- Preamp used (Preamp High Gain or Low Gain)
- Ladder Attenuation
- Signal level

SNR increases with the inverse square root of the bandwidth. So, reducing bandwidth from 450 MHz to 200 MHz, for example, improves SNR by 3.5 dB

$$\left(20 \times \log \frac{\sqrt{450\ MHz}}{\sqrt{200\ MHz}} = 3.5\ dB\right)$$

The other factors listed above, preamp and ladder attenuation, depend on the signal level and also impact SNR. The combined effect of these factors is summarized in *Figure 2* where SNR is plotted as a function of the LMH6518 FS input voltage (assuming scope bandwidth of 200 MHz) and not including the ADC and the front end noise:

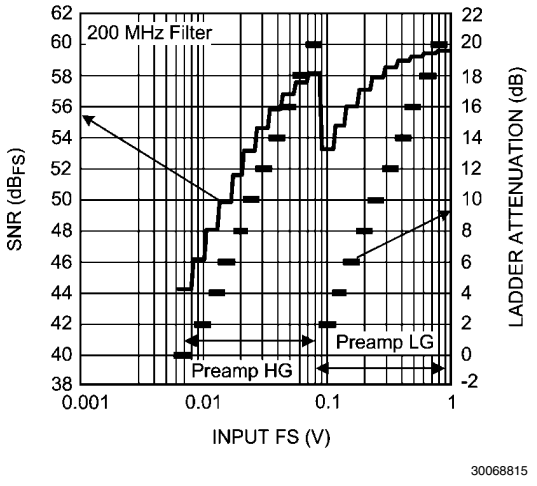


FIGURE 2. LMH6518 SNR & Ladder Attenuation used vs. Input

As can be seen from *Figure 2*, SNR of at least 52 dB is maintained for FS inputs above 24 mV_{PP} (3 mV/DIV on a scope) assuming the LMH6518's internal 200 MHz filter is enabled. Most oscilloscope manufacturers relax the SNR specifications to 40 dB for the highest gain (lowest scope voltage setting) . From *Figure 2*, LMH6518's minimum SNR is 43.5 dB, thereby meeting the relaxed SNR specification for the lower range of scope front panel voltages.

In *Figure 2*, the step-change in SNR near Input FS of 90 mV_{PP} is the transition point from Preamp LG to Preamp HG with a subsequent 3 dB difference due to the Preamp HG/ 20 dB ladder attenuation's lower output noise compared to Preamp LG/ 2 dB ladder attenuation's noise. Judicious choice of front end attenuators can ensure that the 52 dB SNR specification is maintained for scope FS inputs ≥ 24 mV_{PP} by confining the LMH6518 gain range to the lower 30.5 dB

$$\left(= 20 \times \log \frac{0.8\ V_{PP}}{24\ mV_{PP}}\right)$$

from the total range of 40 dB (= 38.8 - (–1.16)) possible.

Here is an example:

To cover the range of 1 mV/DIV to 10 V/DIV (80 dB range), here is a configuration which affords good SNR:

TABLE 1. Oscilloscope Example Including Front-End Attenuators

Row	Scope FS Input (V_{PP})	"S", Scope Vertical Scale (V/DIV)	Preamp	Ladder Attenuation Range (dB)	"A", Front-end attenuation (V/V)	Minimum SNR (dB) with 200 MHz filter
1	8m-24m	1m-3m	HG	0-10	1	44
2	24m-80m	3m-10m	HG	10-20	1	52.0
3	80m-0.8	10m-0.1	LG	0-20	1	53.4
4	0.8-8	0.1-1	LG	0-20	10	53.4
5	8-80	1-10	LG	0-20	100	53.4

In *Table 1*, the highest FS input in Row 5, Column 2 (80 V_{PP}), *and* the LMH6518's highest FS input allowed (0.8 V_{PP}) set the

$$100x \left(= \frac{80\ V_{PP}}{0.8\ V_{PP}}\right)$$

front-end attenuator value. The 100x attenuator will allow high SNR operation to 30.5 dB down, as explained earlier, or 2.4 V_{PP} at scope input. In that same table, Rows 1-3 with no front-end attenuation (1x) cover the scope FS input range from 8 mV_{PP}-800 mV_{PP}. That leaves the scope FS input range of 0.8 V_{PP}-2.4 V_{PP}. If the 100x attenuator were used for the entire scope FS range of 0.8 V_{PP}-80 V_{PP}, SNR would dip below 52 dB for a portion of that range. Another attenuation level is thus required to maintain the SNR specification requirement of 52 dB.

One possible attenuation partitioning is to select the additional attenuator value to cover a 20 dB range above 0.8 V_{PP} FS (to 8 V_{PP}) with the 100x attenuator covering the remaining 20 dB range from 8 V_{PP} to 80 V_{PP}. Mapping 8 V_{PP} FS scope input to 0.8 V_{PP} at LMH6518 input means the additional attenuator is 10x, as shown in *Table 1*, Row 4. The remaining scope input range of 8 V_{PP}-80 V_{PP} would then be covered by the 100x front-end attenuator derived earlier. The entire scope input range is now covered with SNR maintained about 52 dB for scope FS input ≥ 24 mV_{PP}, as shown in *Table 1*.

SETTINGS AND ADC SPI CODE (ECM)

Covering the range from 1 mV/DIV to 10 V/DIV requires the following to be adjusted within the digital oscilloscope:

- Front-end attenuator
- LMH6518 Preamp
- LMH6518 Ladder Attenuation
- ADC FS value (ECM)

The LMH6518 Product Folder contains a spreadsheet which allows one to calculate the front-end attenuator, LMH6518 Preamp gain (HG or LG) and ladder attenuation, and ADC FS setting based on the scope vertical scale (S in V/DIV). This spreadsheet can be found at:

http://www.national.com/appinfo/amps/LMH6518_Cal.xls

Here is the step by step procedure that explains the operations performed by the said spreadsheet based on the scope vertical scale setting (S in V/div) and front-end attenuation "A" (from *Table 1*). A numerical example is also worked out for more clarification:

1. Determine the required signal path gain, K:

$$K = 20 \times \log \frac{0.95 \times 700\ mV_{PP}}{\frac{8 \times S(V/div)}{A}} = -21.6 + 20 \times \log \frac{A}{S(V/div)}$$

(assuming the full scale signal occupies 95% of the 0.7 V_{PP} FS (for 5% overhead) which occupies 8 vertical scope divisions).
Required condition: –2.37 dB ≤ K ≤ 40.3 dB
Example: With S = 110 mV/DIV, *Table 1* shows that *A = 10 V/V:*

$$\rightarrow K = -21.6 + 20 \times \log \frac{10}{110\ mV} = 17.57\ dB$$

2. Determine the LMH6518 gain, G:
G is the closest LMH6518 gain, to the value of K where:
G = (38.8 – 2n)dB; n = 0, 1, 2, …, 20
For this example, the closest G to K = 17.57 dB is 16.8 dB (with n = 11). The next LMH6518 gain, 18.8 dB (with n = 10) would be incorrect as 16.8 is closer. If 18.8 dB were mistakenly chosen, the ADC FS setting would be out of range.
Therefore: *G = 16.8 dB*
3. Determine Preamp (HG or LG) & Ladder Attenuation:
If G ≥ 18.8 dB → Preamp is HG and Ladder Attenuation = 38.8 - G
If G < 18.8 dB → Preamp is LG and Ladder Attenuation = 18.8 - G
For this example, with G = 16.8 → *Preamp LG* and *Ladder Attenuation = 2 dB* (= 18.8-16.8).
4. Determine the required ADC FS voltage, FS_E:

$$FS_E = \frac{S \times 8}{A} \times 1.05 \times 10^{\frac{G}{20}}$$

The "1.05" factor is to add 5% FS overhead margin to avoid ADC overdrive.

$$FS_E = \frac{S \times 8}{10} \times 1.05 \times 10^{\frac{16.8}{20}} = 639.3\ mV$$

Required condition: 0.56V ≤ FS_E ≤ 0.84V
Recommend condition: 0.595V ≤ FS_E ≤ 0.805V for optimum ADC FS
5. Determine the ADC ECM code ratio:

$$ECM\ (ratio) = \frac{FS_E - 0.56}{0.28}$$

where:
a) 0.28V= (0.84-0.56)V
b) 0.56V is the lower end of the ADC FS adjustability
For this example:

$$\text{ECM (ratio)} = \frac{0.6393 - 0.56}{0.28} = 0.283$$

Required condition: 0 ≤ ECM (ratio) ≤ 1

6. Determine the ECM binary code to be sent on ADC SPI bus:
   Convert the ECM value represented by the ratio calculated above, to binary:
   ECM (binary) = DEC2BIN{ECM(ratio)* 511, 9}

where "DEC2BIN" is a spreadsheet function which converts the decimal ECM ratio, from step 5 above, multiplied by 511 distinct levels, into binary 9 bits.

Note: The Web based spreadsheet computes ECM without the use of "DEC2BIN" function to ease usage by all spreadsheet users who may not have this function installed.

For this example: ECM (binary) = DEC2BIN(0.283*511, 9) = 010010000. This would be the number to be sent to the ADC on the SPI bus to program the ADC to the proper FS voltage.

INPUT/OUTPUT CONSIDERATIONS

The LMH6518's ideal Input/Output Conditions, considered individually, are listed below:

TABLE 2. LMH6518's Ideal Input/Output Conditions

Impedance from each input to ground (Ω)	Common Mode Input (V)	Differential Input (V_{PP})	Load Impedance (Ω)	Differential Output (V)	Common Mode Output (V)
≤50	1.5 to 3.1	<0.8	100 (differential)/ 50 (single ended)	<0.77	0.95-1.45

In addition to the individual conditions listed in *Table 2*, the Input/Output terminal conditions should match differentially (i.e. +IN to −IN and +OUT to −OUT), as well, for best performance.

The input is differential but can be driven single-ended as long as the conditions of *Table 2* are met and there is good matching between the driven and the undriven inputs from DC to the highest frequency of interest. If not, there could be a settling time impact among other possible performance degradations. The datasheet specifications are with single-ended input, unless specified. Here is the recommended bench-test schematic to drive one input and to bias the other input with good matching in mind:

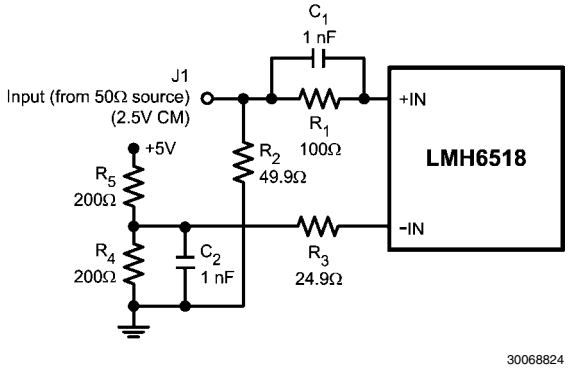


FIGURE 3. Recommended Single-Ended Bench-Test Input Drive from 50Ω Source

With the schematic of *Figure 3*, each LMH6518 input sees 25Ω to ground at the higher frequencies when the capacitors look like shorts. This impedance increases to 125Ω at DC for both inputs, thereby preserving the required matching at any frequency. This configuration, using properly selected R's and C's, allows four times less biasing power dissipation than when the undriven input is biased with an effective 25Ω from the LMH6518 input to ground.

It is possible to drive the LMH6518 input from a ground referenced 50Ω source by providing level shift circuitry on the driven input. *Figure 4* shows a circuit where ½ the input signal reaches the LMH6518 input while the negative supply voltage (V_{EE}) ensures that the 50Ω source at J1 does not experience any biasing current while providing 50Ω termination to the source. The driven input (+IN) is biased to 2.5V (V_{CC}/2):

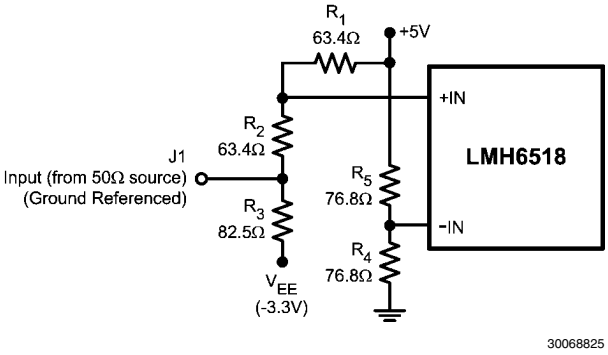


FIGURE 4. LMH6518 Driven by a Ground Referenced Source

In the schematic of *Figure 4*, the equivalent impedance from each LMH6518 input to ground is around 38Ω. This configuration's power consumption of ~0.5W (in R_1 - R_5) is higher than that of *Figure 3* because of additional power dissipated to perform the level shifting. Additional 50Ω attenuators can be placed between J1 and R_2/R_3 junction in *Figure 4* in order to accommodate higher input voltages.

It is also possible to shift the LMH6518 *output* common mode level using a level shift approach similar to that of *Figure 4*. The circuit in *Figure 5* shows an implementation where the LMH6518's nominal 1.2V CM output, set by a 1.2V on V_{CM} input from the Gsample/s ADC, is shifted lower for proper interface to different ADC's which require V_{CM} = 0V and have high input impedance:

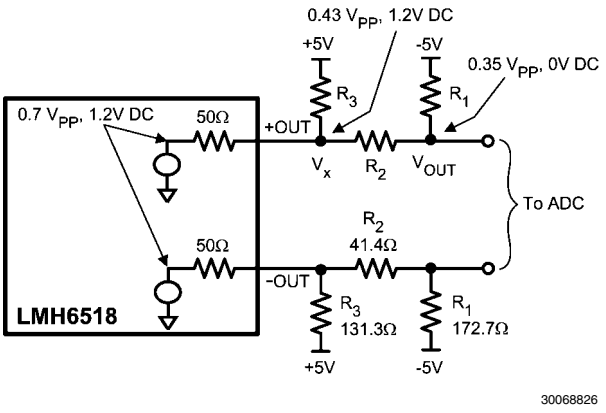


FIGURE 5. Output CM Shift Scheme

With the scheme of *Figure 5*, Vx is kept at 1.2V, by proper selection of external resistor values, so that the LMH6518 outputs are not CM-loaded. As was the case with input level shifting, this output level shifting also consumes additional power (0.58W).

Output Swing, Clamping, and Operation Beyond Full Scale

One of the major concerns in interfacing to low voltage ADC's (such as the Gsample/s ADC's that the LMH6518 is intended to drive) is ensuring that the ADC input is not violated with excessive drive. For this reason, plus the very important requirement of an oscilloscope to recover quickly and gracefully from an overdrive condition, the LMH6518 is fitted with three overvoltage clamps; one at the Preamp output and one at Main and Auxiliary outputs each. The Preamp clamp is responsible for preventing the Preamp from saturation (to minimize recovery time) with large ladder attenuation when Preamp output swing is at its highest. On the other hand, the output clamps, perform this function when the Ladder attenuation is lower and hence the output amplifier is closer to saturation, and prolonged recovery, if not properly clamped. The combination of these clamps results in the Typical Performance Characteristic plots of "Output vs. Input" where it is possible to observe where output limiting starts due to the clamp action. LMH6518 owes its fast recovery time (< 5 ns) from 50% overdrive to the said clamps.

"Output vs. Input" plots, in the Typical Performance Characteristics section, can be used to determine the LMH6518 linear swing beyond full scale. This information sets the overdrive limit for both oscilloscope waveform capture and for signal triggering. The Preamp clamp is set tighter than the output clamp, evidenced by lower output swing with 20 dB Ladder attenuation than with 0 dB. With high ladder attenuation (20 dB) defining the limit, the graphs show that the "+Out" and "–Out" difference of 0.4V is well inside the clamp range, thereby ensuring 0.8 V_{PP} of unhindered output swing. This corresponds to an overdrive capability of approximately ±7% beyond full scale.

Here is a block diagram for how the LMH6518 is used in an oscilloscope:

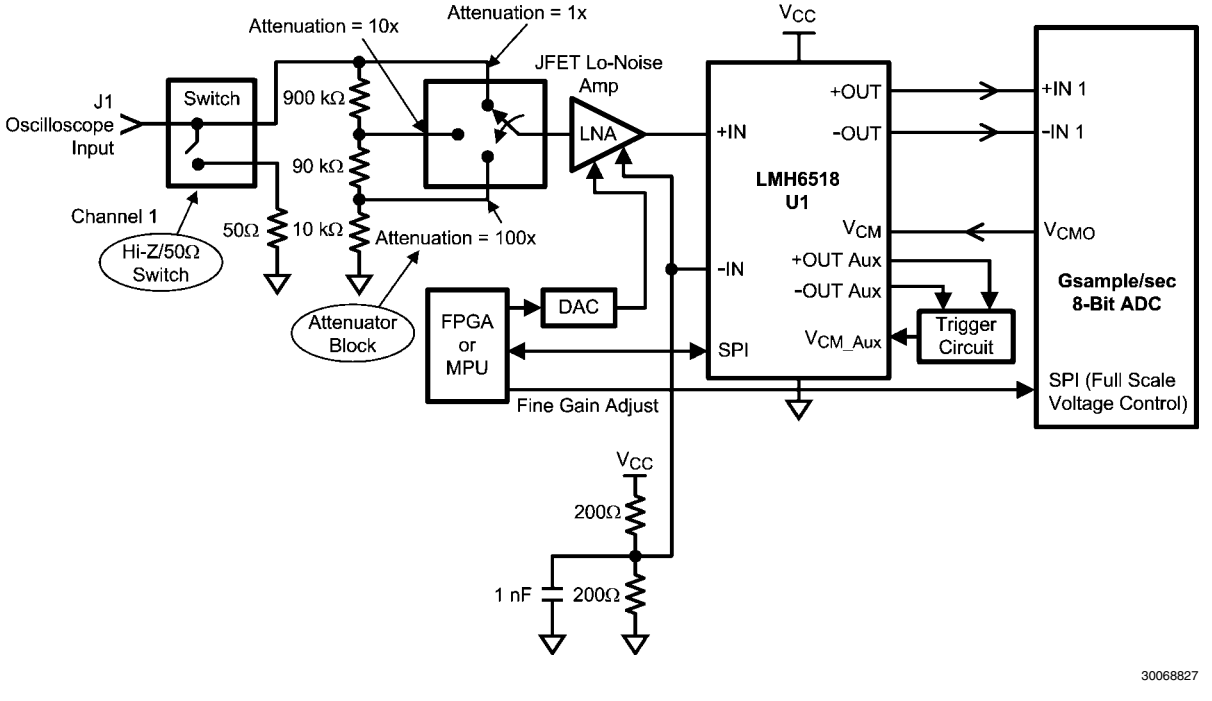


FIGURE 6. Digital Oscilloscope Front-End

From *Figure 6*, the signal path consists of the input impedance switch, the attenuator switch, Low Noise Amplifier (LNA, JFET amplifier) to drive the LMH6518 input (+IN), and the DAC to provide offset adjust. The LNA must have the following characteristics:

- Set U1's common mode level to $V_{CC}/2$ (~2.5V)
- Very low drift (1 mV shift at LNA output could translate into 88 mV shift at LMH6518 output at max gain, or ~13% of FS).
- Low output impedance (≤ 50Ω) to drive U1, for good settling behavior
- Low Noise (<0.98 nV/$\sqrt{Hz}$) to reduce the impact on the LMH6518 Noise Figure. Note that *Figure 6* does not show the necessary capacitors across the resistors in the front-end attenuators (see *Figure 15*). These capacitors provide frequency response compensation and limit the noise contribution from the resistors so that they do not impact the signal path noise. For more information about front-end attenuator design, including frequency compensation, see the Reference section for additional resources.
- Gain of 1 V/V (or very close to 1 V/V)
- Excellent frequency response flatness from DC to > 500-800 MHz to not impact the time domain performance

The undriven input (–IN) is biased to $V_{CC}/2$ using a voltage driver. The impedance driving the LMH6518's –IN should be closely matched to the LNA's output impedance for good settling time performance.

Appendix A shows one possible implementation of the LNA buffer along with performance data.

When the LMH6518's Auxiliary output is not used, it is possible to disable this output using SPI-1 (see "Logic Functions" section for SPI register map). The Electrical Characteristic Table shows that by doing so, device power dissipation decreases by the reduction in supply current of about 60 mA. As can be seen in *Figure 7*, in the absence of heavy common loading, the Auxiliary output will be at a voltage close to 1.7V (V_{CC} = 5V). With higher supply voltages, the Auxiliary voltage will also increase and it is important to make sure any circuitry tied to this output is capable of handling the 2.3V possible under V_{CC} worst case condition of 5.5V.

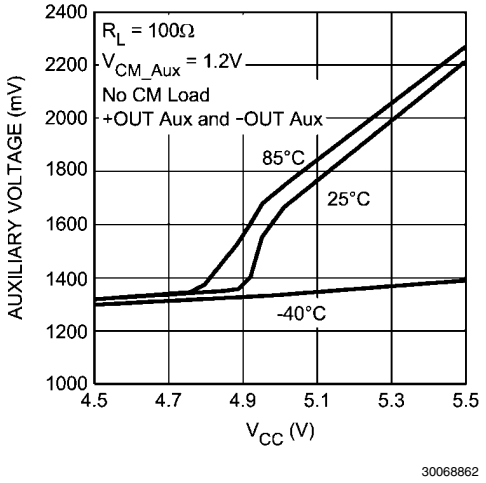


FIGURE 7. Auxiliary Output Voltage as a Function of V_{CC}

LOGIC FUNCTIONS

The following LMH6518 functions are controlled using the SPI-1 compatible bus:

- Filters (20, 100, 200, 350, 650, 750 MHz or full bandwidth)
- Power Mode (Full Power or Auxiliary Hi-Z (high impedance)
- Preamp (HG or LG)
- Attenuation Ladder (0-20 dB, 10 states)
- LMH6518 state "Write" or "Read" back

The SPI-1 bus uses 3.3V logic. "SDIO" is the serial digital input-output which can write to the LMH6518 or read back from it. "SCLK" is the bus clock with chip select function controlled by "$\overline{CS}$"

TABLE 3. SPI-1 Pin Descriptions

Pin Name	Type	Function and Connection
$\overline{CS}$	Input	Serial Chip Select: While this signal is asserted SCLK is used to accept serial data present on SDIO and to source serial data on SDIO. When this signal is de-asserted, SDIO is ignored and SDIO is in TRI-STATE® mode.
SCLK	Input	Serial Clock: Serial data are shifted into and out of the device synchronous with this clock signal. SCLK transitions with $\overline{CS}$ de-asserted are ignored. SCLK to be stopped when not needed to minimize digital crosstalk.
SDIO	Input-Output	Serial Data-In or Data-out: Serial data are shifted into the device (8 bit Command and 16 bit Data) on this pin while $\overline{CS}$ signal is asserted during Write operation. Serial data are shifted out of the device on this pin during a read operation while $\overline{CS}$ signal is asserted. At other times, and after one complete Access Cycle (24 bits, see *Figure 8* and *Figure 9*), this input is ignored. This output is in TRI-STATE mode when $\overline{CS}$ is de-asserted. This pin is bi-directional.

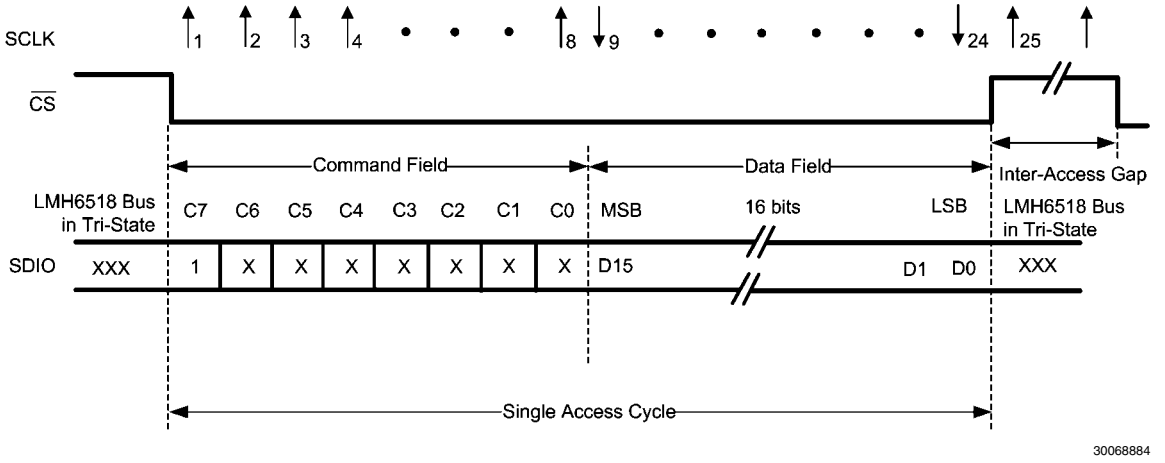


FIGURE 8. Serial Interface Protocol- Read Operation

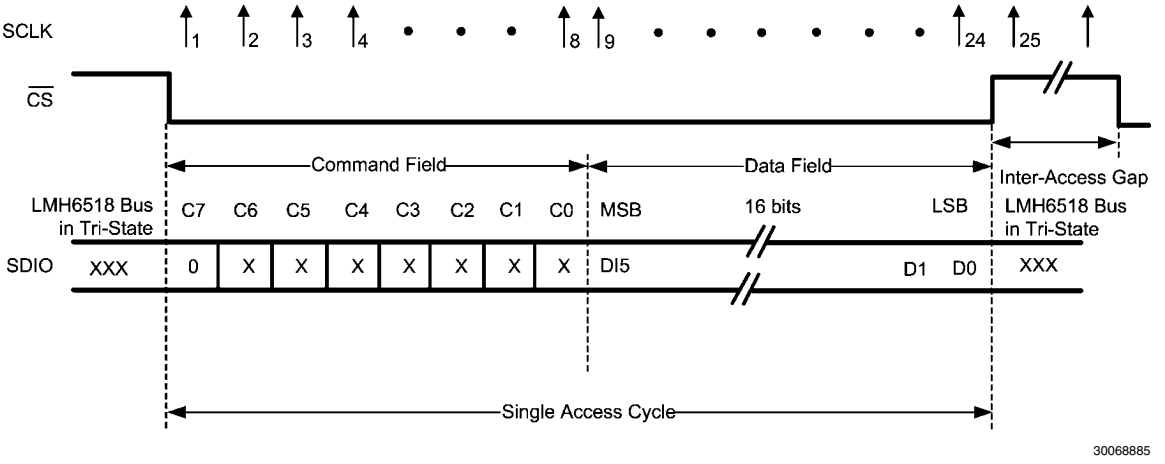


FIGURE 9. Serial Interface Protocol- Write Operation

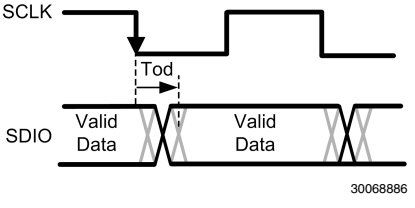


FIGURE 10. Read Timing

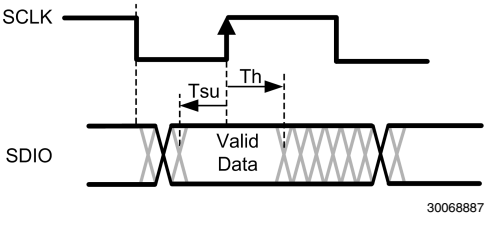


FIGURE 11. Write Timing

TABLE 4. Data Field

							Filter				Pre-amp	Ladder Attenuation			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
X	0	0	0	0	0=Full Power 1=Aux Hi-Z	0	See Table 6			0	0=LG 1=HG	See Table 7			

Note: Bits D5, D9, D11-D14 must be "0". Otherwise, device operation is undefined and specifications are not guaranteed.

TABLE 5. Default Power-On Reset Condition

							Filter				Pre-amp	Ladder Attenuation			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

TABLE 6. Filer Selection Data Field

Filter			Filter BW
D8	**D7**	**D6**	**(MHz)**
0	0	0	Full
0	0	1	20
0	1	0	100
0	1	1	200
1	0	0	350
1	0	1	650
1	1	0	750
1	1	1	Unallowed

Note: All filters are low pass single pole roll-off and operate on both Main and Auxiliary outputs. These filters are intended as signal path bandwidth and/ or noise limiting.

TABLE 7. Ladder Attenuation Data Field

Ladder Attenuation				Ladder Attenuation (dB)
D3	**D2**	**D1**	**D0**	
0	0	0	0	0
0	0	0	1	–2
0	0	1	0	–4
0	0	1	1	–6
0	1	0	0	–8
0	1	0	1	–10
0	1	1	0	–12
0	1	1	1	–14
1	0	0	0	–16
1	0	0	1	–18
1	0	1	0	–20
1	0	1	1	Unallowed
1	1	0	0	Unallowed
1	1	0	1	Unallowed
1	1	1	0	Unallowed
1	1	1	1	Unallowed

Note: An "Unallowed" SPI-1 state may result in undefined operation where device behavior is not guaranteed.

OSCILLOSCOPE TRIGGER APPLICATIONS

With the Auxiliary output of the LMH6518 offering a second output that follows the Main one (except for a slightly reduced distortion performance), the oscilloscope trigger function can be implemented by tapping this output. The "V_{CM_Aux}" input of the LMH6518 allows the Auxiliary common mode to be set. The trigger function can be physically located at a distance from the main signal path, if need be, by taking advantage of the differential Auxiliary output and rejecting any board related common mode interference pick-up at the receive end.

If Trigger circuitry is physically close to the LMH6518, the circuit diagram shown in *Figure 12* allows operation using only one of two Auxiliary outputs. The unused output does need to be terminated properly using R_1, R_{11} combination. U3 (DAC101C085) generates a 0- 2.5V trigger level, with 2.4 mV resolution

$$(= \frac{2.5V}{2^{10}})$$

or 0.7% (= 2.4 mV x 100/0.35 V_{PP}) of FS, which is compared to the LMH6518 "+Out Aux" by using an ultra-fast comparator, U2 (LMH7220). U2's complimentary LVDS output is terminated in the required 100Ω load (R_{10}), for best performance, where the LVDS Trigger output is available. The LMH7220's offset voltage (±9.5 mV) and offset voltage drift (±50 µV/°C) error will be 5.9 LSB

$$(9.5\ mV + 50\ \frac{\mu V}{°C} \times 100°C = 1.45\ mV \equiv 5.9\ LSB)$$

of the Trigger DAC (U3). The offset voltage related portion of this error can be nulled-out, if necessary, during the oscilloscope initial calibration. To do so, the LMH6518 input is terminated properly with no input applied and U3 output is adjusted around V_{CM_Aux} voltage (1.2V ±10 mV) while looking for U2's output transition. U3's output, relative to V_{CM_Aux} at transition corresponds to U2's offset error which can be factored into the Trigger readings and thus eliminated, leaving only the Offset voltage temperature drift component (= 2 LSB).

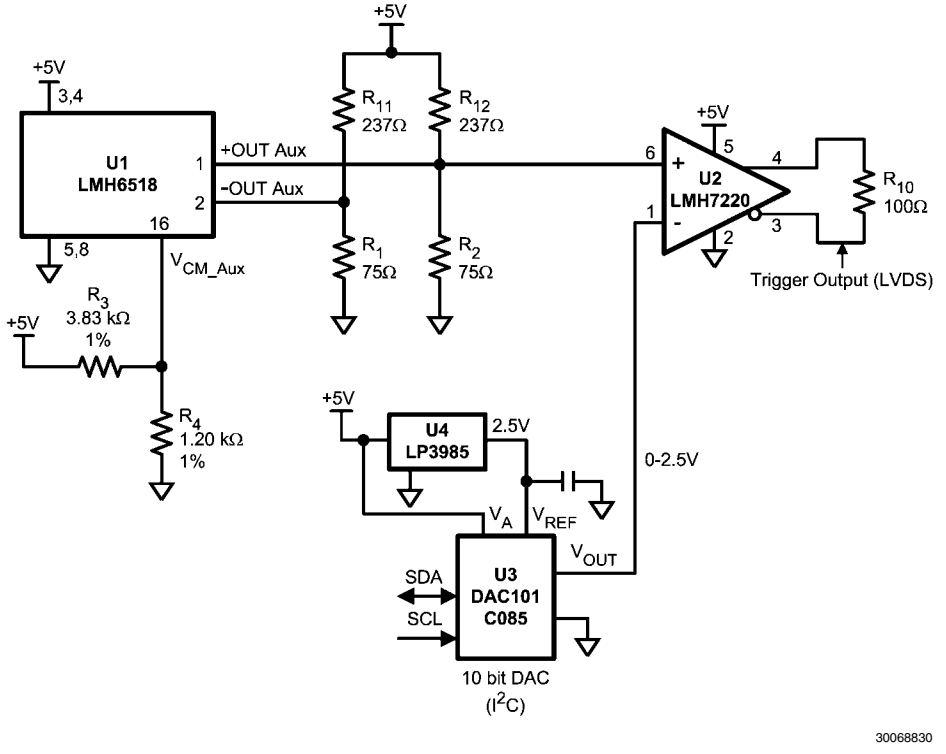


FIGURE 12. Single-Ended Trigger from LMH6518 Auxiliary Output

U2's minimum Toggle Rate specification of 750 Mb/s with ±50 mV overdrive allow the oscilloscope to trigger on repetitive waveforms well above the 500 MHz oscilloscope bandwidth applications, when the input signal is at least 14.3% of FS swing

$$(= \frac{50\ mV}{\frac{0.7V}{2}} \times 100)$$

The worst case single event minimum discernable pulse width is set by the LMH7220's propagation delay specification of 3.63 ns (20 mV overdrive).

Both the Main and the Auxiliary outputs can recover gracefully and quickly from a 50% overdrive condition as tabulated in the Electrical Characteristics table under overdrive Recovery Time. Overdrive conditions beyond 50%, however, could result in longer recovery times due to the interaction between an internal clamp and the common mode feedback loop that sets the output common mode voltage. This may have an impact on both the displayed waveform and the oscilloscope

Trigger. The result could be a loss of Trigger pulse and/or visual distortion of the displayed waveform. To avoid this scenario, the oscilloscope should detect an excessive overdrive and go into trigger-loss mode. Done this way, the oscilloscope display would show the last waveform that did not violate the overdrive condition. Preferably there would be a visual indicator on the screen that alerts the user of the situation so that he can correct the excessive condition to return to normal display.

APPENDIX A

Here is the schematic drawing for a possible implementation of the LNA buffer shown in *Figure 6*:

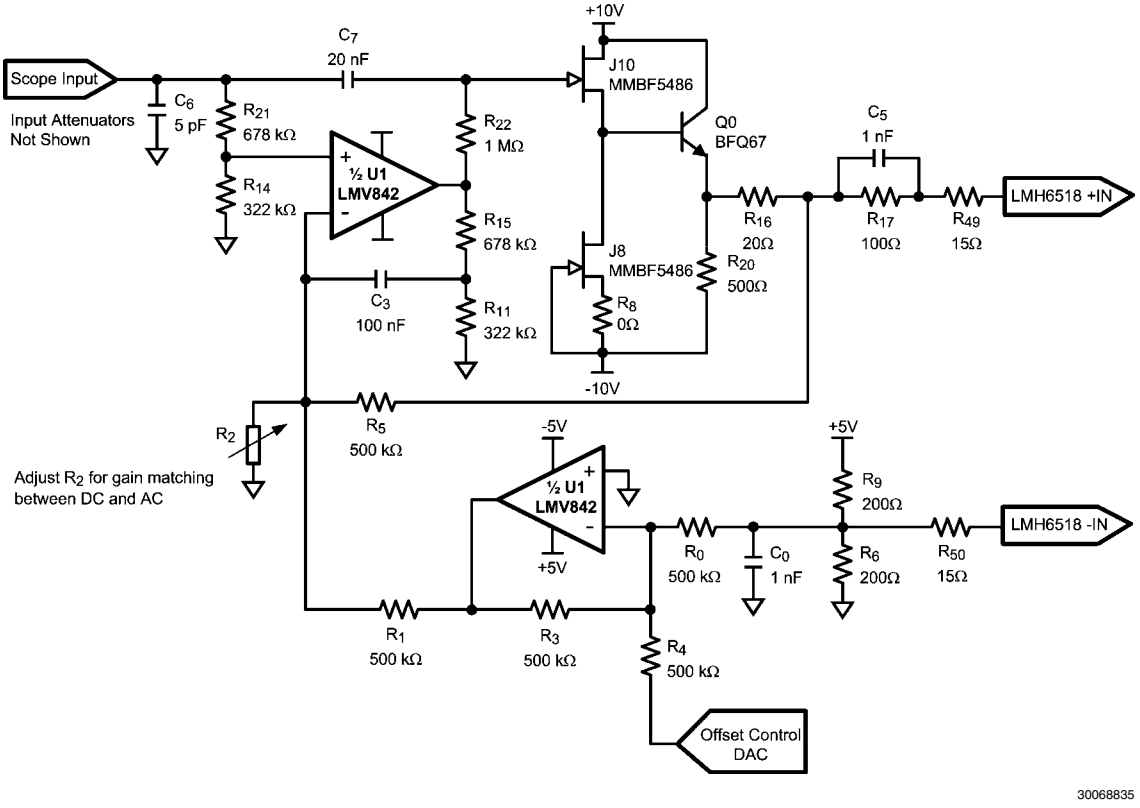


FIGURE 13. JFET LNA Implementation

CIRCUIT OPERATION

This circuit uses an N-Channel JFET (J10) in Source-Follower configuration, to buffer the input signal, with J8 acting as a constant current source. This buffer presents a fixed input impedance (1 MΩ||10 pF) with a gain close to 1 V/V.

The signal path is AC coupled through C_7 with DC (and low frequency) at LMH6518 +IN maintained through the action of U1. NPN transistor Q0 is an emitter follower which isolates the buffer from the load (LMH6518 input and board traces).

The undriven input of the LMH6518, –IN, is biased to 2.5V by R_6, R_9 voltage divider. The Lower ½ of U1 inverts this voltage and the upper ½ of U1 compares it to the combination of the driven output level at LMH6518 +IN and the scaled version of scope input at R_{14}, R_{21} junction, and adjusts J10 Gate accordingly to set the LMH6518 +IN. This control loop has a frequency response that covers DC to a few Hz, limited by the roll-off capacitor C_3 and R_{15} combination (1st order approximation). DC and low frequency gain is given by:

$$\text{Gain (DC)} = \frac{R_{14}}{R_{14} + R_{21}} \left(1 + \frac{R_5}{R_1 \,||\, R_2}\right) \cong 1 \text{ V/V}$$

With the values in *Figure 13* → $R_2 \approx 452$ kΩ: .

For a flat frequency response, the DC (low frequency) gain needs to be lowered to match the less-than-1 V/V AC (high frequency) path gain through the JFETs. This can be done by increasing the value of R_2.

By choosing the values of R_{15} and R_{11} so that

$$\frac{R_{21}}{R_{14}} = \frac{R_{15}}{R_{11}}$$

the frequency response at J10 Gate (and consequently the output) will remain flat when C_7 starts to conduct. Offset correction is done by varying the voltage at R_4, using a DAC or equivalent as shown, in order to shift the LMH6518 +IN voltage relative to –IN. The result is a circuit which shifts the ground referenced scope input to 2.5V (V_{CC}/2) CM with adjustable offset and without any JFET or BJT related offsets.

Note that the front-end attenuator (not shown) lower leg resistance should be increased for proper divider-ratio to account for the 1 MΩ shunt due to the series combination of R_{21} and R_{14}. For example, a 10:1 front-end attenuator could be formed by a series 900 kΩ and a shunt 111 kΩ for a scope BNC input impedance of 1 MΩ (= 900K + (111K || 1M)).

Table 8 lists other possible JFET candidates that fall in the range of speed (f_t) and low noise needed:

TABLE 8. Suitable JFET Candidates Specifications

Company	Part Number	V_P (V)	I_{dss} (mA)	gm (mS)	Input C (pF)	noise * (nV/RtHz)	Break down (V)	Calculated f_t (MHz)
Interfet	IF140	–2.2	10	5.5	2.3	4	–20	380
Interfet	IF142	–2.2	10	5.5	2.3	4	–25	380
Interfet	2N5397/8	–2.5	13	8	5	2.5	–25	254
Interfet	2N5911/2	–2.5	13	8	5	2.5		254
Interfet	J308/9/10	–2.3	21	17	5.8		–25	466
Philips	BF513	-3	15	10	5			318
Fairchild	MMBF5486	–4	14	7	4	2.5	–25	278
Vishay Siliconix	SST441	–3.5	13	6	3.5	4	–35	272

*Noise data at ~ $I_{dss}/2$

The LNA noise could degrade the scope's SNR if it is comparable to the input referred noise of the LMH6518. LNA noise is influenced by the following operating conditions:

a) JFET equivalent input noise

b) BJT Base current

Reducing either "a" or "b" above, or both, reduces noise. One way to reduce "a" is to increase R_8 (currently set to 0Ω). This will reduce the noise impact of J8 but requires a JFET which has a higher I_{dss} rating in order to maintain the operating current of J10 so that J10's noise contribution is minimized. Reducing the BJT Base current can be accomplished with increasing R_{20} at the expenses of higher rise/fall times. A higher β will also reduce the Base current (keep in mind that β and f_t at the operating Collector current is what matters).

Figure 14 shows the impact of the JFET buffer noise on SNR, compared to SNR in *Figure 2*, assuming either 3 nV/$\sqrt{\text{Hz}}$ or 1.5 nV/$\sqrt{\text{Hz}}$ buffer noise for comparison:

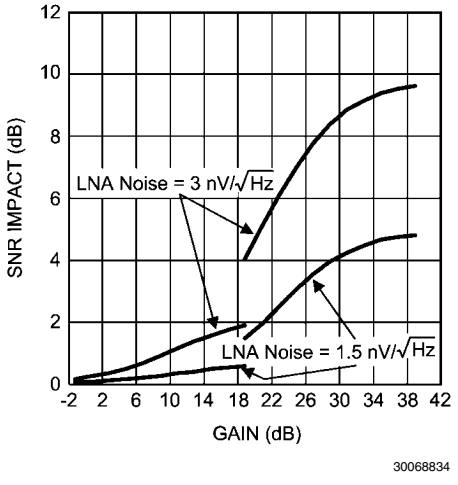


FIGURE 14. LNA Buffer SNR Impact

ATTENUATOR DESIGN

Figure 15 shows a front-end attenuator designed to work with the JFET LNA of *Figure 13*.

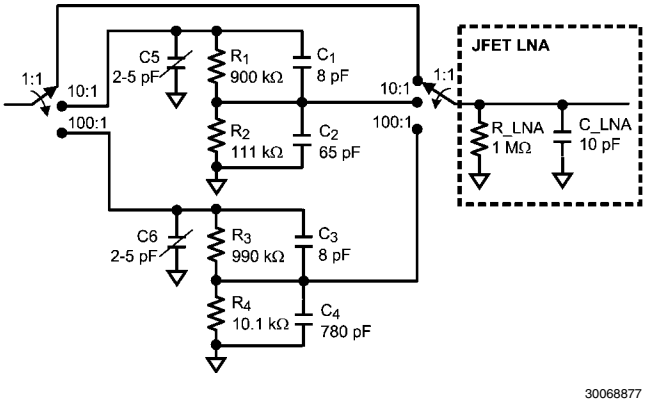


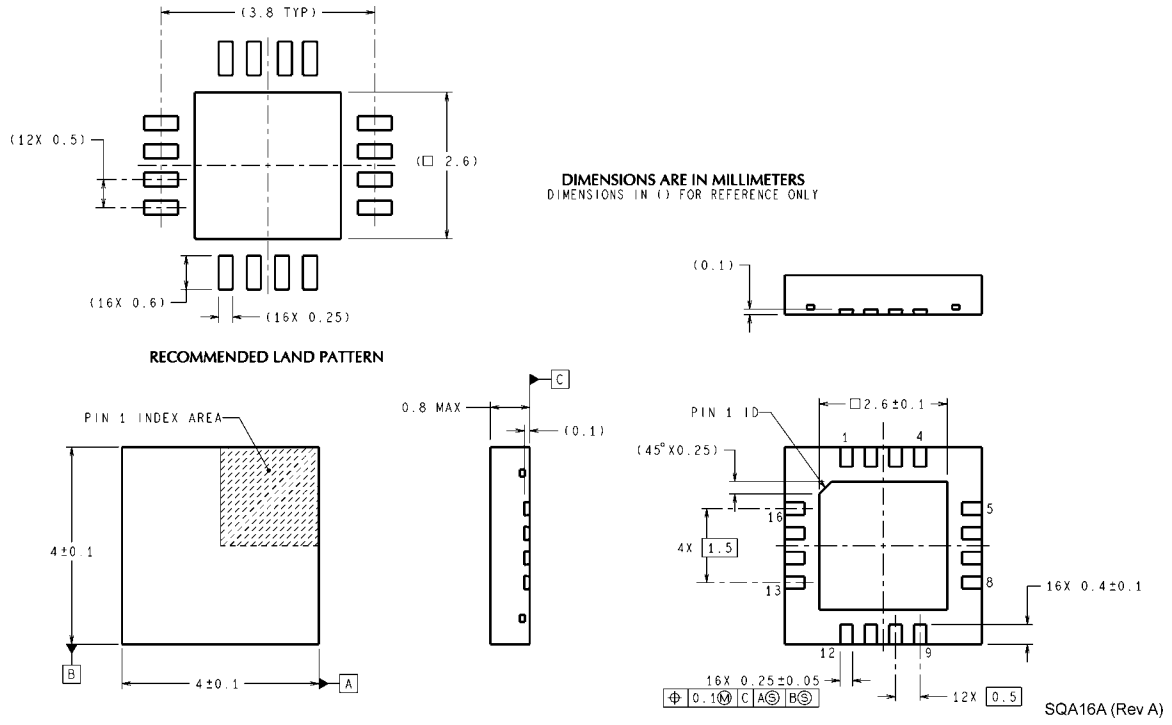
FIGURE 15. Front End Attenuator for *Figure 13* JFET LNA

R_LNA" and "C_LNA" are the input impedance components of the JFET LNA. The 10:1 and 100:1 attenuators bottom resistors (R_2 and R_4) are adjusted higher to compensate for the LNA's 1 MΩ input impedance, compared to the case where a high-input-impedance LNA is used. The two switches used on the input and output of the attenuator block must be low capacitance, high isolation switches in order to reduce any speed or crosstalk impact. C_1-C_4 provide the proper frequency response (and step response) by creating "zeros" that flatten the response for wide-band operation. For the 10:1 attenuator, $R_1C_1 = R_2C_2$. The same applies to the 100:1 attenuator. The shunt capacitors C_1-C_4 have a very important other benefit in that they roll-off the resistor thermal noise at a low frequency (low pass response, –3 dB down at ~20 kHz) thereby eliminating any significant noise contribution from the attenuation resistors. Otherwise, the channel noise would be dominated by the attenuator resistor thermal noise. C_2 and C_6 trimmer capacitors can be adjusted to match the input capacitance regardless of attenuator used.

REFERENCE

1. Wideband amplifiers by Peter Staric and Erik Margan, published by Springer in 2006. (Section 5.2).

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

Notes

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