AN-2045 LMH6521EVAL Evaluation Board
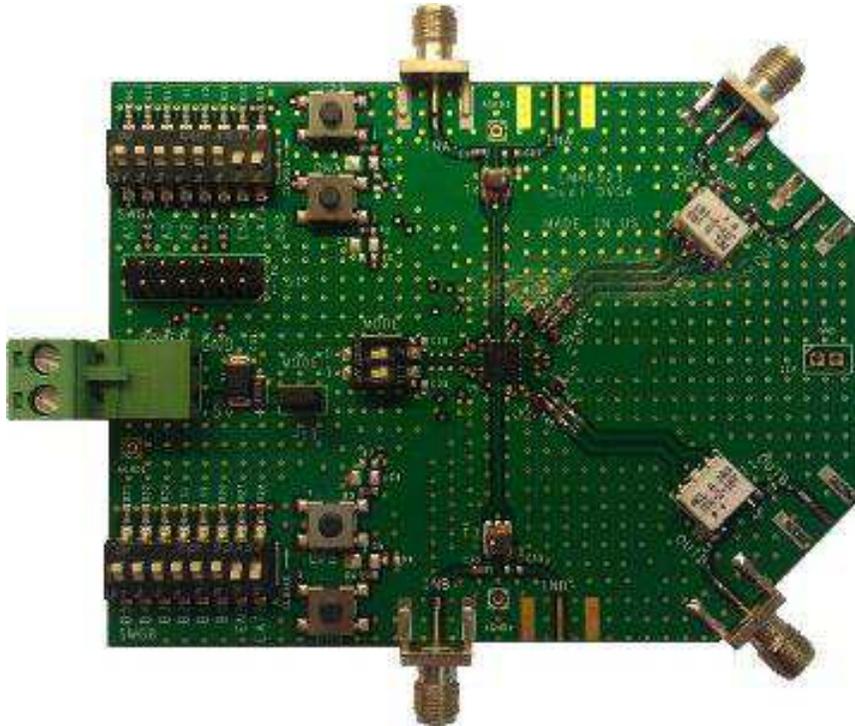

Figure 1. LMH6521EVAL Evaluation Board

1   General Description

The LMH6521EVAL evaluation board, Figure 1, is designed to aid in the characterization of Texas Instruments' High Speed LMH6521 High Performance Dual DVGA. The evaluation board is used as a guide for high frequency layout and as a tool to aid in device testing and characterization.

2   Basic Operation

The LMH6521 DVGA has differential inputs and differential outputs for both channels A and B. To aid in evaluation with 50Ω single ended test equipment, the LMH6521EVAL evaluation board provides for input and output transformers and is shipped with both input and output transformers loaded. The signal path uses the IN+ and OUT− marked connectors. The IN− and OUT+ signal paths are grounded and the SMA connectors are not installed.

The input and output pins of the LMH6521 will self bias to approximately mid supply (2.5V). The LMH6521EVAL board has been designed with AC coupling on both input and output signal paths to protect test equipment and to ensure proper operation of the LMH6521 DVGA. Any modifications to the board should preserve the operating points of the DVGA and protect sensitive test equipment.

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The LMH6521 is a dual DVGA with channels A and B that have independent enable for power down. The LMH6521EVAL board operates with a single 5V supply with typical supply current of 225mA when both channels are enabled.

Transformers T1– T4 can provide both impedance matching as well as single ended to differential conversion. The 4:1 turns ratio input transformers match 50Ω equipment with the 200Ω input impedance of the LMH6521 DVGA . Do not connect the transformer secondary winding directly to ground.

Capacitors C34–C37 isolate the output transformer from the output of the amplifier. The spaces marked C14 and C15 are left empty by the factory and capacitors can be added to create a low pass filter. Resistors could be placed in these locations to create different load conditions for the amplifier. The spaces marked C7 & C8 are populated with a 0Ω resistor to connect the primary side of the transformers to outputs OUTA- and OUTB-.
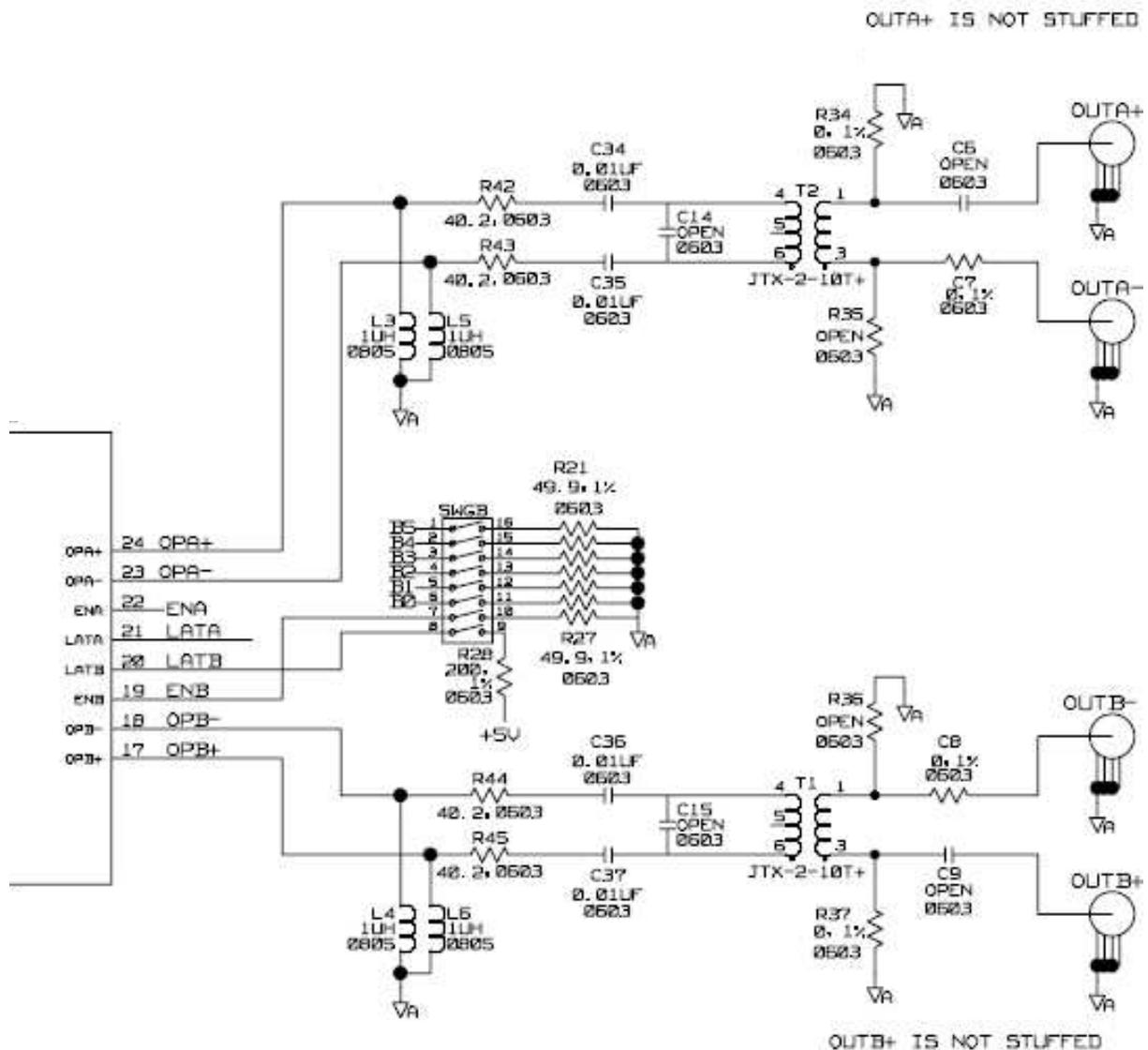

Figure 2. Output Schematic

Figure 3. Input Schematic

The board was designed to be very flexible for many different configurations. Zoomed in portions of the input and output schematics are shown above in Figure 2 and Figure 3. The evaluation board, as shipped, has been optimized for ease of use with single ended 50 Ohm test equipment. This configuration may not emulate the most common application circuits. The full schematic is shown in Figure 10 and the board or Gerber files are available in the LMH6521 product folder on www.ti.com.

3   Standard EVK Board Configurations

The LMH6521EVAL evaluation board is shipped for a single-ended input, single-ended output configuration. The input transformers (T3 & T4) have a 4:1 turns ratio to match the 200Ω input impedance of the amplifier. The LMH6521 amplifier has low output impedance of around 8Ω. With the low output impedance and output resistors R42–R45 of 40.2Ω, the output transformers (T1 & T2) 2:1 turns ratio gives a 200Ω load at the amplifier output. Other load conditions can be achieved by changing out the components on the evaluation board.

Near the power connector is a 0.1" pitch double-row headers (J1) that provides off board access to the LMH6521 digital control pins. The J1 pins and functions are described in the J1 Header Jack Pin Assignment table below. The jack labeled J11 is a shorting block and it provides the 5V power to the LMH6521. By removing the short on this jack and replacing it with an ammeter the current drawn by the DVGA can be measured. The jack labeled J12 is a ground connector and is normally left empty.

4   Using with Different Sources or Loads

The LMH6521EVAL board supports differential operation on both inputs and outputs. However, they will require additional components and some board rework. For driving the evaluation board from a differential source, symmetrical signal paths are provided. Both input and output paths support fully differential test equipment.

To drive the LMH6521 evaluation board from a differential source, the transformers T3 & T4 and zero ohm resistors R47 & R49 must be removed and the addition of 0.01uF capacitors are needed for C21 and C23. Add a short wire jumper between the primary and secondary transformer pads to complete the differential signal path along with a 200Ω termination resistor across the inputs to match the impedance of the source and amplifier as shown in Figure 4. DC coupled operation is possible using differential signals. For DC coupled operation, make sure that the test equipment can provide the 2.5±1V offset voltage on the input and output.

For differential output signals remove transformers T1 & T2 and zero ohm resistors R34 & R37. Add short wire jumpers or zero ohm resistors for place holders labeled C6 & C9 to complete the signal path across the transformer pads similar to the changes required for differential inputs as shown in Figure 5. Additional SMA connectors will be needed for signals INA-, INB-, OUTA+, and OUTB+.

The LMH6521EVAL evaluation board is 0.63" thick and uses edge mounted Emerson part # 142–0701–806 end launch, nickel plated SMA connectors.
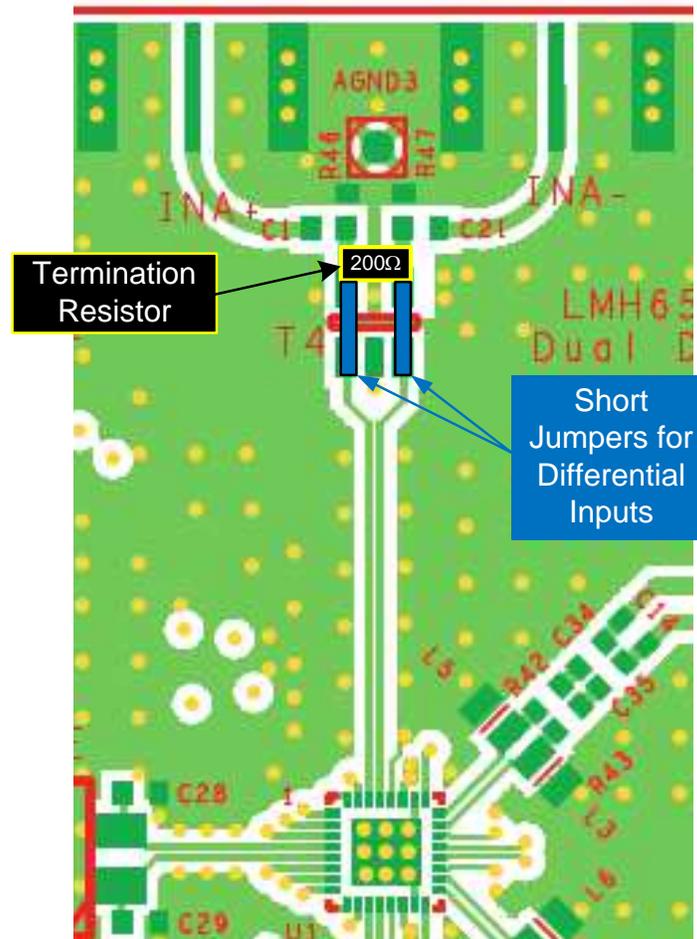
Figure 4. Connections for Differential Input
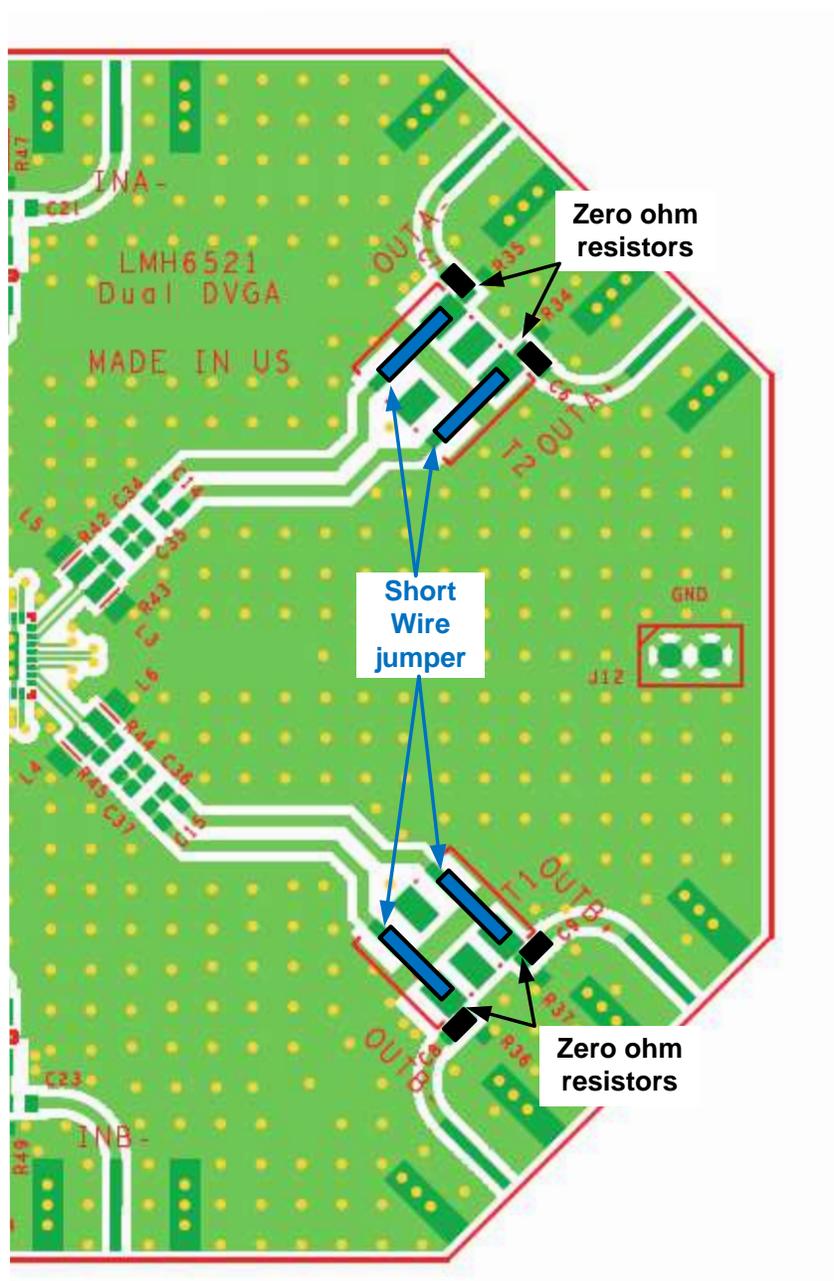
Figure 5. Connections for Differential Output

5   Gain Control

The LMH6521 DVGA has three control modes including parallel mode, serial (SPI compatible) mode, and pulse mode. Parallel and pulse modes are fully supported on the board. Serial mode control requires the use of a PC and the SPUSI2 USB to SPI interface board (available separately) or an external signal source like a logic analyzer or a microcontroller. Each of the control modes is detailed fully below.

6   Parallel Mode

For ease of use, dip switches SWGA & SWGB are provided to set the LMH6521 gain in parallel mode. This mode is the easiest to use for basic measurements. To set the board in parallel mode, the dip-switch labeled MODE must be set such that the top switch labeled MODE0 is in the OFF position and the bottom switch labeled MODE1 is also in the OFF position. To move the MODE switches to the OFF position, slide them towards the LMH6521 device.

When using the dip switches SWGA & SWGB to change gain in parallel mode ensure that the switch labeled LATA or LATB is in the OFF position. With the latch switch in the OFF state the device is in transparent mode and any change in the dip switches is immediately reflected in the device gain. Moving the latch pin switch to the ON position holds the last gain setting and ignores changes in the gain control switches. When the latch switch is in the ON position the dip switches that control the gain can be configured as desired and then implemented by momentarily switching the LATA or LATB switch. For detailed instructions on the pin functions see the LMH6521 product datasheet. The gain bits are binary weighted with the LSB representing a 0.5dB gain step and the MSB representing a 16dB step. The steps increase the gain when the switch is in the ON position. For example, switching A5 or B5 from OFF to ON will increase the gain by 16dB. For example, maximum gain of channel A is when SWGA dip switch positions A5 to A0 are all in the ON position while minimum gain is when they are all in the OFF position. The LMH6521 has a maximum voltage gain of 26dB and minimum gain of —5.5dB with a total of 31.5dB of gain range. Between the Gain control bits [A5–A0 and B5–B0] and the latch switch is the enable (ENA or ENB) switch. Setting this switch to the OFF position Enables the respective DVGA channel.

7   Pulse Mode

The DVGA is also very easy to control in Pulse mode. For system implementations Pulse mode requires fewer digital control lines than parallel mode at the expense of gain control speed. To use Pulse Mode the Mode switches should be set such that MODE0 is in the OFF position and MODE1 is in the ON position. Gain changes are accomplished by using the UP and DN buttons. There are separate buttons for the A channel and the B channel.

The dip switches that are used to control gain in parallel mode have different functions in Pulse mode. SWGA, which controls the A channel should be set with the A4, A3, ENA, and LATA positions in the OFF settings. The positions marked A5 and A0 need to be in the ON position. The positions marked A2(S1) and A1(S0) are used to set the DVGA gain step size as shown below in the Pulse Mode Gain Step Sizes S1 and S0 table.

Table 1. SWG Switch Settings for Pulse Mode

SWGA	A5	A4	A3	A2	A1	A0	ENBA	LATA
SWGB	B5	B4	B3	B2	B1	B0	ENBB	LATB
Position	ON	OFF	OFF	A/R	A/R	ON	OFF	OFF

The switch marked SWGB controls the B channel and should be configured as follows: positions marked B4, B3, ENBB and LATB set to OFF, the positions marked B5 and B0 need to be in the ON position. The positions marked B2(S1) and B1(S0) set the channel B gain step size. Refer to the Pulse Mode Gain Step Sizes S1 and S0 table below. Note that if the switch marked B5 on SWGB is in the OFF position the entire amplifier will be in an undefined state and will not operate correctly.

The push button switches located just to the right of dip switches SWGA & SWGB, are for use in pulse mode. The UPA and UPB buttons increment the gain up one step while the DNA and DNB buttons decrement the gain by one step. The gain step sizes are set by the DIP switches labeled S1 and S0 on the parallel control DIP switches. Each channel can have a different gain step size.

Table 2. Pulse Mode Gain Step Sizes S1 and S0 are located in SWGA and SWGB

S1	S0	Gain Step Size
On	On	0.5dB
On	Off	1dB
Off	On	2dB
Off	Off	6dB

8 Serial Mode

Serial mode is the most complex control mode and is considerably slower than parallel mode, but it is very flexible and requires fewer digital control lines. Serial mode requires external logic, either from a microcontroller or logic analyzer. A 0.1" double-row header strip (J1) is located between dip switch SWGA and green power connector. This strip can be used to connect a micro-controller or logic analyzer to the serial control pins. The header pin functions are shown in the table below. Please refer to the product datasheet for the full description of these pin functions. Please note that the SWGA dip switches will impact the on-board impdeance for the J1 header pins. If the SWGA dip switches are set to the OFF postion, there is no on-board termination for the J1 header pins and they will appear as high impedance to the logic analyzer. Make sure that this does not result in logic signals that are beyond the absolute maximum rating for the LMH6521. When the SWGA dip switches are in the ON position there are 50Ω resistors to ground connected the header pins in parallel with the LMH6521 logic pins. Some digital sources are unable to drive this load condition. If it seems that the LMH6521 is not responding to digital control signals this could be one cause. The default operation is to set all the dip switch positions for SWGA to all OFF.

To aid in the evaluation of SPI controlled devices, TI™ manufactures the SPUSI2 board and provides the TinyI2CSPI software to control it. The software and the SPUSI2 evaluation board kit, shown in , can be ordered from the TI website. The software is Windows compatible. The first step in using the board in serial mode is to place the MODE switches in the proper configuration. The MODE0 switch will be in the ON position and the MODE1 switch will be in the OFF position. For proper SPI operation, the SWGA dip switches need to be set to the OFF positions while SWGB switch positions B5 and B0 need to be in the ON positions with B1–B4 set to OFF. Directions for installing the USB control software and evaluation board drivers are in the user's guide available on the TI website.

Once the SPUSI2 board drivers and TinyI2CSPI software are installed, connect the SPUSI2 board directly onto the LMH6521 EVK double-row header (J1) by aligning pin 1 as shown in the Figure 8. The TinyI2CSPI software should be set to SPI mode and the CS and CKPOL columns should be set to 1. The CKPHA column needs to be set to 1 and the number of bits should be set to 16. Check the LMH6521 datasheet for details on the data to be sent to the DVGA registers. Some simple SPI commands, as well as the proper software settings are shown below in Figure 7.

Table 3. Header Jack Pin Assignment (J1)

Header Pin	LMH6521 Pin #	Parallel Function	Serial Function	Pulse Function
J1–1	32	Address bit 2	Chip Select	Step Size MSB
J1–2	N/A	Ground	Ground	N/A
J1–3	2	Address bit 4	CLK	Up A
J1–4	N/A	N/A	N/A	N/A
J1–5	31	Address bit 1	Serial Data Out	Step Size LSB
J1–6	21	Latch A	N/A	N/A
J1–7	1	Address bit 3	Serial Data In	Down A
J1–8	22	Enable A	Enable A	Enable A
J1–9	3	Address bit 5	N/A	N/A
J1–10	25	Address bit 0	N/A	N/A
J1–11	N/A	N/A	N/A	N/A
J1–12	N/A	N/A	N/A	N/A
J1–13	N/A	N/A	N/A	N/A
J1–14	N/A	N/A	N/A	N/A
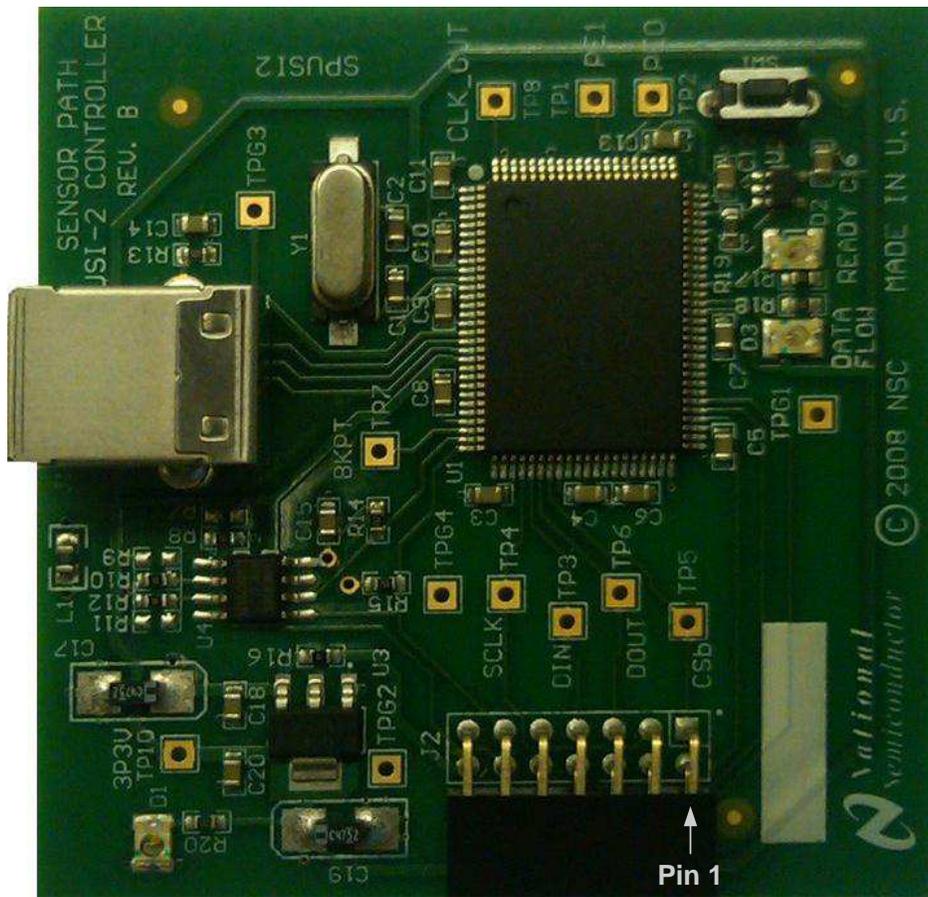
Figure 6. SPUSI2 Serial Protocal Interface Board
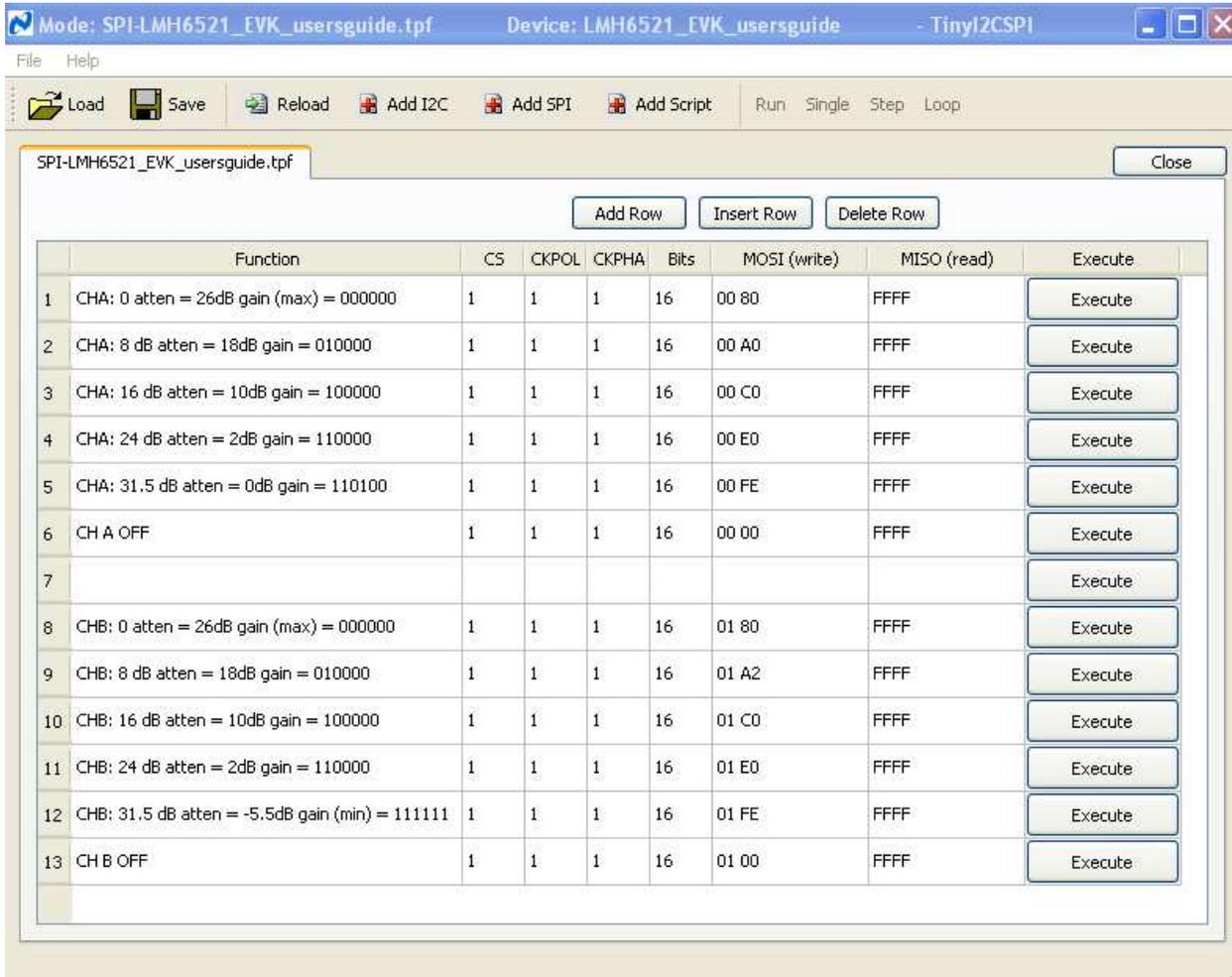
Figure 7. Software Setting for SPI control
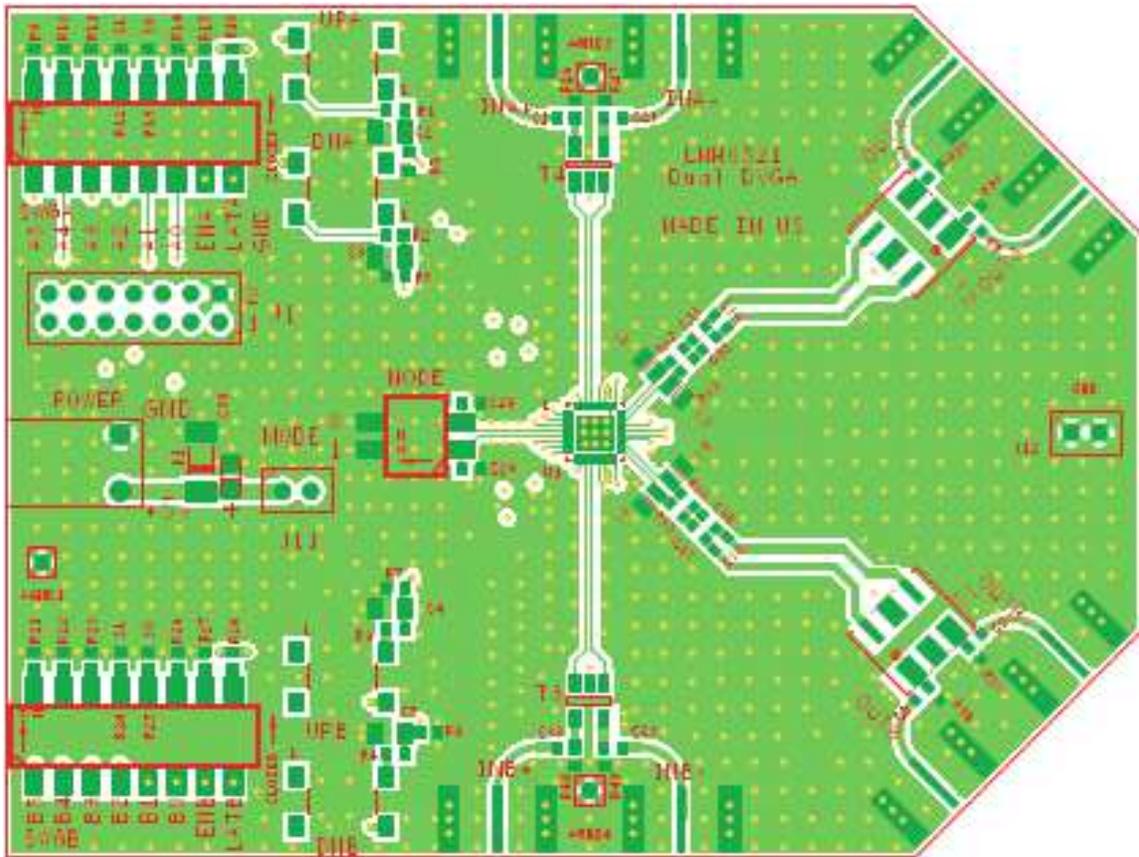
Figure 8. Evaluation Board Top Layer
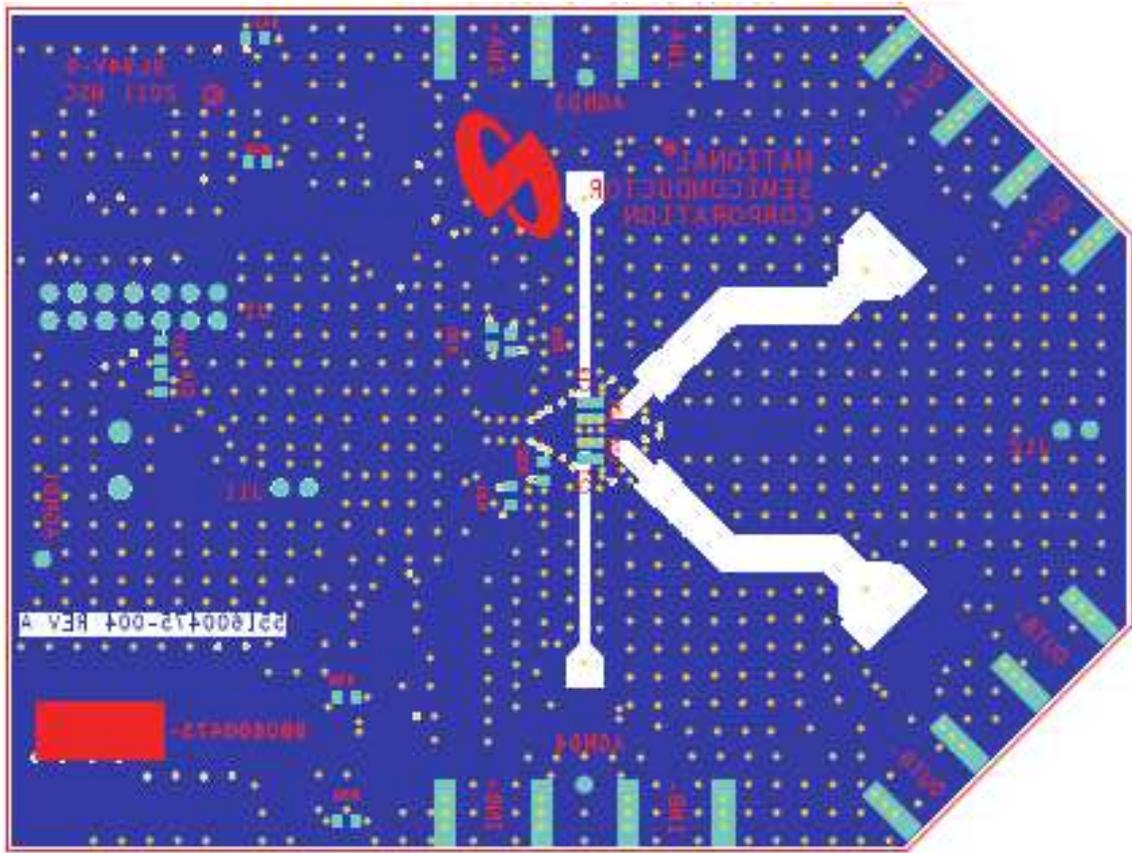
Figure 9. Evaluation Board Bottom Layer
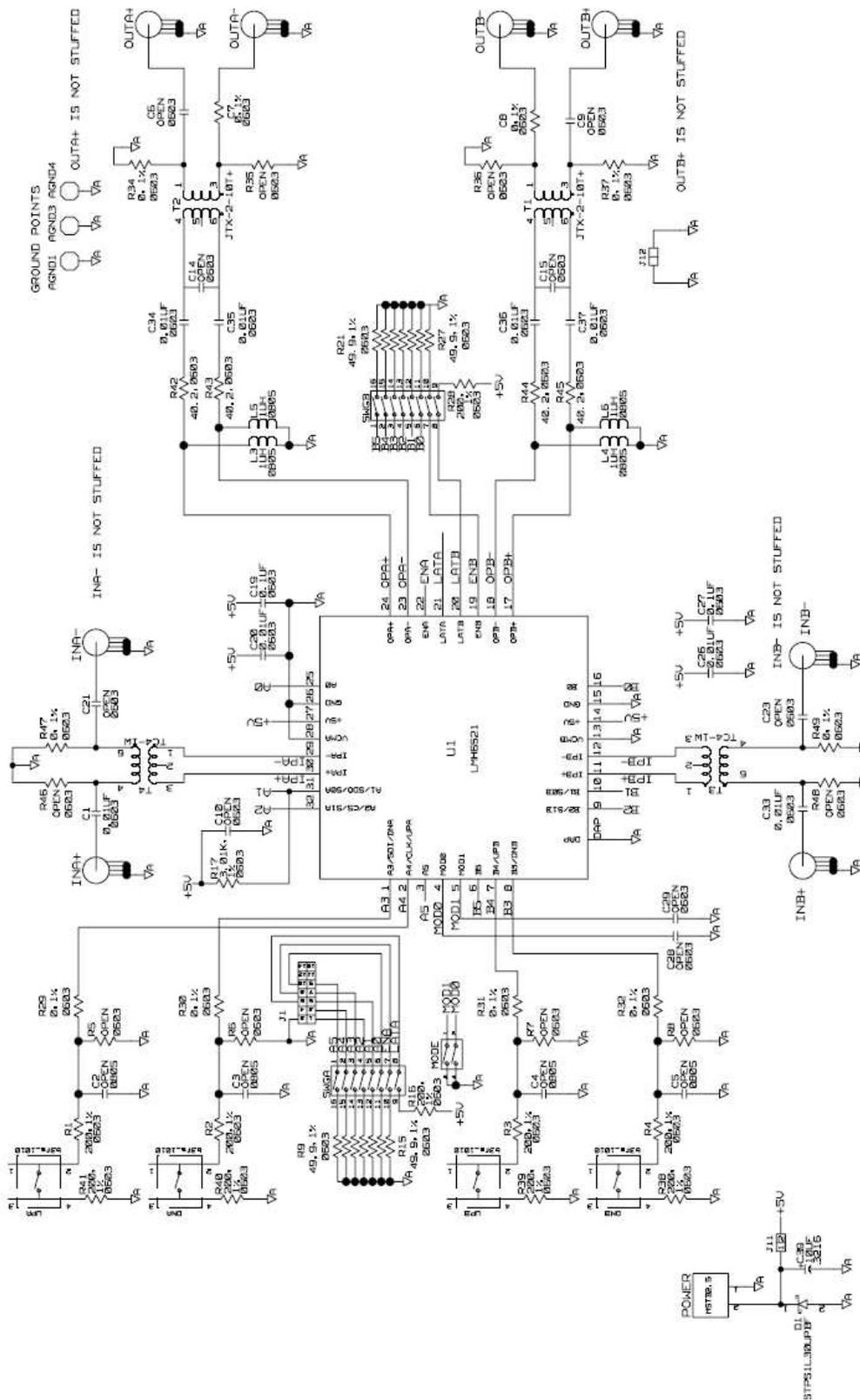
Figure 10. Signal Path Schematic

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