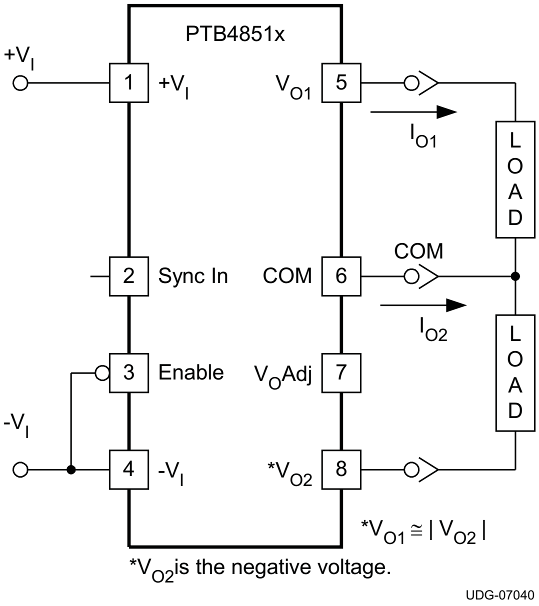
DUAL COMPLEMENTARY-OUTPUT DC/DC CONVERTER FOR DSL

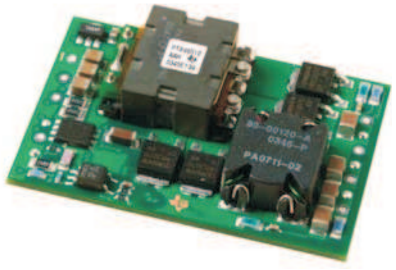
Check for Samples: PTB48510, PTB48511

FEATURES

- **Dual Complementary Outputs (±5 V, ±12 V, or ±15 V)**
- **Input Voltage Range: 36 V to 75 V**
- **On/Off Enable for Sequencing**
- **1500 V_{DC} Isolation**
- **Overcurrent Protection**
- **Overvoltage Protection (PTB48511 only)**
- **Over Temperature Shutdown**
- **Undervoltage Lockout**
- **Temperature Range: –40°C to 85°C**
- **Industry Standard Outline**
- **Fixed Frequency Operation**
- **Synchronizes with PTB48500**
- **Powers Line Drivers for AC-7 and Other xDSL Chipsets**
- **Safety Approvals:**
  - **EN 60950**
  - **UL/cUL 60950**

STAND-ALONE APPLICATION





DESCRIPTION

The PTB4851x series of isolated DC/DC converter modules produce a complementary pair of regulated supply voltages for powering line-driver devices in xDSL telecom applications. The modules operate from a standard telecom (–48 V) central office (CO) supply and can provide up to a 72 W of power in a balanced load configuration.

The A-suffix module (±5 V) is designed to power the line driver devices for the AC-7 ADSL chipset. Other voltage options powers other analog applications requiring a complementary supply with relatively balanced loads.o

Both the PTB48510 and PTB48511 include an “on/off” enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO). The PTB48511 adds output overvoltage protection (OVP).

The control inputs, *Enable* and *Sync In*, are compatible with the *EN Out* and *Sync Out* signals of the PTB48500 DC/DC converter. This allows the power-up and switching frequency of the PTB4851x modules to be directly controlled from a PTB48500. Together the PTB48500 and PTB4851xA converters meet all the system power and sequencing requirements of the AC- ADSL chipset.

The PTB4851x uses double-sided surface mount technology contruction. The package size is based on the industry standard outline and does not require a heatsink. Both through-hole and surface mount pin configurations are available.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

BASE DEVICE NUMBER. (PTB4851xxx)		OUTPUT VOLTAGE (PTB4851xx)		PACKAGE OPTIONS (PT4851xx)		
ORDER PREFIX	**DESCRIPTION**	**CODE**	**VOLTAGE (V)**	**CODE**	**DESCRIPTION**	**PACKAGE REFERENCE (1)**
PTB48510xxx	Basic model	A	±5	AH	Horizontal T/H	ERK
PTB48511xxx	Adds output overvoltage protection (2)	B	±12	AS	SMD, Standard (3)	ERL
		C	±15 (4)			

(1) Reference the applicable package reference drawing for the dimensions and PC board layout
(2) Output overvoltage protection
(3) *Standard* option specifies 63/37, Sn/Pb pin solder material
(4) ±15-V output is not available with the PTB48511

Environmental and General Specifications

(Unless otherwise stated, all voltages are with respect to V_{I2})

				VALUE	UNIT
V_I	Input Voltage Range	Over output load range		36 to 75	V_{DC}
	Isolation Voltage	Input-output/input/case		1500	V
	Capacitance	Input to output		1500	pF
	Resistance	Input to output		10	mΩ
T_A	Operating Temperature Range	Over V_I Range		–40 to 85	°C
OTP	Over-Temperature Protection	Shutdown threshold		115 (1)	
		Hysterisis		10	
T_{reflow}	Solder Reflow Temperature	Surface temperature of module body or pins		235 (2)	
T_s	Storage Temperature			–55 to 125	
	Mechanical Shock	Per Mil-STD-883D, Method 2002.3 1 ms, 1/2 Sine, mounted	T/H	500	G
			SMD	250	
	Mechanical Vibration Mil-STD-883D	Mil-STD-883D, Method 2007.2 20-2000 Hz	T/H	10	G
			SMD	5	
	Weight			28	grams
	Flammability	Meets UL 94V-O			

(1) This parameter is assured by design.
(2) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

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ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, C_I = 0 μF, C_O = 0 μF, I_{O1} = I_{O2} = 3.25 A maximum)

PARAMETER		TEST CONDITIONS		PTB4851xA			UNIT
				MIN	TYP	MAX	
P_O	Output Power	Total output power from V_{O1} or V_{O2}		0		65 (1)	W
I_{O1}, I_{O2}	Output Current	Over V_I range, $I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A		0		6.5(2)	A
I_{O1} - I_{O2}	Output Load Imbalance	$I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A		0		1 (3)	A
V_{O1}, V_{O2}	Output Voltage	Includes set point, line, load, $I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A $-40°C \leq T_A \leq 85°C$		4.75(2)	5	5.25(2)	V
ΔReg_{temp}	Temperature Variation	$-40°C \leq T_A \leq 85°C$, $I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A	V_{O1}		±1		$\%V_O$
			V_{O2}		±1		
ΔReg_{line}	Line Regulation	Over V_I range, balanced load	V_{O1} or V_{O2}		±0.1	±0.4	$\%V_O$
ΔReg_{load}	Load Regulation	Over I_{O1}, I_{O2}range, balanced load	V_{O1} or V_{O2}		±0.2	±0.4	$\%V_O$
η	Efficiency				86%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, C_O = 10-μF tantalum capacitor			20	30 (4)	mV_{pp}
t_{tr}	Transient Response	0.11 A/μs load step, 50% to 75% I_{O1} or I_{O2} maximum			30		μs
ΔV_{tr}		V_{O1} or V_{O2} overshoot/undershoot			±1.0		$\%V_O$
$I_O$trip	Overcurrent Threshold	V_I = 36 V, reset followed by auto-recovery		6.8	7.5	10	A
$V_{O1(trip)}$, $V_{O2(trip)}$	Overvoltage Threshold	Outputs latched off (5)	PTB48510	NA		NA	V
			PTB48511	5.9		7	
	Short Circuit Current	Continuous overcurrent trip, I_{O1} = I_{O2}	$I_{O1(pk)}$ $I_{O2(pk)}$		12.5		A
			Duty		10%		
$V_{O1(adj)}$, $V_{O2(adj)}$	Output Voltage Adjust Range	V_{O1} or V_{O2} adjust simultaneously		3.5		5.5	V
f_S	Switching Frequency	Over V_I and I_O ranges		440	470 (6)	500	kHz
V_I on	Undervoltage lockout	V_I increasing			33		V
V_I off		V_I decreasing			32		
V_{IH}	On/Off Enable (pin 3) High-level input voltage	Referenced to V_I (pin 4)		3.6		75 (7)	V
V_{IL}	Low-level input voltage			–0.2		0.8	
I_{IL}	Low-level input current					–1	mA
I_I standby	Standby Input Current	Pin 3 connected			2		mA
t_{ON}	Start-up Time	$I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A, V_{O1} or V_{O2} rising 0 to 0.95 (typ)		6	10	22	ms
C_I	Internal Input Capacitance				3		μF
C_O	External Output Capacitance	Capacitance from either output to COM (pin 6)		0		5000 (8)	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, T_A = 40°C, ground benign	PTB48510A	2.7			10^6 hrs
			PTB48511A	2.5			

(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) Under balanced load conditions, load current flowing out of V_{O1} is balanced to within ±0.1 A of that flowing into V_{O2}.
(3) A load imbalance is the difference in current flowing from V_{O1} to V_{O2}. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10-μF tantalum capacitor connected from V_{O1} (pin 5) or V_{O2} (pin 8), to COM (pin 6).
(5) If the overvoltage threshold is exceeded by either regulated output the module will shut down, turning both outputs off. This is a latched condition, which can only by reset by removing and then re-applying the module's input power.
(6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to V_I. The open-circuit voltage is 5 V maximum. If it is left open circuit the converter operates when input power is applied.
(8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

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ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, C_I = 0 μF, C_O = 0 μF, I_{O1} = I_{O2} = 3.25 A maximum)

PARAMETER		TEST CONDITIONS		PTB4851xB			
				MIN	TYP	MAX	UNIT
P_O	Output Power	Total output power from V_{O1}or V_{O1}		0		72(1)	W
I_{O1} or I_{O2}	Output Current	Over V_I range, I_{O1} ≤ 0.1 A or I_{O2} ≤ 0.1 A ≤ 0.1 A		0		3(2)	A
I_{O1} - I_{O2}	Output Load Imbalance	I_{O1} ≥ 0.1 A, I_{O2} ≥ 0.1 A		0		1(3)	A
V_{O1} or V_{O2}	Output Voltage	Includes set point, line, load, I_{O1} ≤ 0.1 A or I_{O2} ≤ 0.1 A ≤ 0.1 A –40°C ≤ T_A ≤ 85°C		11.6(2)	12	12.4(2)	V
ΔReg_{temp}	Temperature Variation	–40°C ≤ T_A ≤ 85°C, I_{O1} ≤ 0.1 A or I_{O2} ≤ 0.1 A	V_{O1} or V_{O2}		±1		%V_O
ΔReg_{line}	Line Regulation	Over V_I range, balanced load	V_{O1} or V_{O2}		±0.05	±0.5	%V_O
ΔReg_{load}	Load Regulation	Over I_{O1} or I_{O2} range, balanced load	V_{O1} or V_{O2}		±0.1	±1	%V_O
η	Efficiency				89%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, C_O = 10 μF tantalum capacitor			20	80(4)	mV_{pp}
t_{tr}	Transient Response	0.1 A/μs load step, 50% to 75% I_{O1} or I_{O2} maximum			30		μs
ΔV_{tr}		V_{O1} or V_{O2} overshoot/undershoot			±1		%V_O
$I_O$trip	Overcurrent Threshold	V_I = 36 V, reset followed by auto-recovery		3.3	3.8	5	A
$V_{O1(trip)}$, $V_{O2(trip)}$	Overvoltage Threshold	Outputs latched off (5)	PTB48510A	NA		NA	V
			PTB48511A	14	15.8	17	
	Short Circuit Current	Continuous overcurrent trip, I_{O1} = I_{O2}	$I_{O1(pk)}$ $I_{O2(pk)}$		6		A
			Duty		10%		
$V_{O1(adj)}$, $V_{O2(adj)}$	Output Voltage Adjust Range	V_{O1} and V_{O2} adjust simultaneously		6.5		13.4	V
f_S	Switching Frequency	Over V_I and I_O ranges		440	480(6)	500	kHz
V_I on	Under-Voltage Lockout	V_I increasing			33		V
V_I off		V_I decreasing			32		
	On/Off Enable (pin 3)	Referenced to V_I (pin 4)					
V_{IH}	High-level input voltage			3.6		75(7)	V
V_{IL}	Low-level input voltage			–0.2		0.8	
I_{IL}	Low-level input current					–1	mA
I_I standby	Standby Input Current	Pin 3 open circuit			2		mA
t_{ON}	Start-up Time	I_{O1} ≤ 1 A or I_{O2} ≤ 1 A, V_{O1} or V_{O2} rising 0 to 0.95 (typ)		6	12	18	ms
C_I	Internal Input Capacitance				3		μF
C_O	External Output Capacitance	Capacitance from either output to COM (pin 6)		0		3000(8)	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, T_A = 40°C, ground benign	PTB48510B	2.8			10^6 Hrs
			PTB48511B	2.5			

(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) Under balanced load conditions, load current flowing out of V_{O1} is balanced to within ±0.1 A of that flowing into V_{O2}.
(3) A load imbalance is the difference in current flowing from V_{O1} to V_{O2}. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10 μF tantalum capacitor connected from V_{O1} (pin 5) or V_{O2} (pin 8), to COM (pin 6).
(5) If the overvoltage threshold is exceeded by either regulated output the module will shut down, turning both outputs off. This is a latched condition, which can only by reset by removing and then re-applying the module's input power.
(6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to V_I. The open-circuit voltage is 5 V maximum. If it is left open circuit the converter operates when input power is applied.
(8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

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ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, C_I = 0 μF, C_O = 0 μF, $I_{O1} = I_{O2}$ = 3.25 A maximum)

PARAMETER		TEST CONDITIONS		PTB4851xC			
				MIN	TYP	MAX	UNIT
P_O	Output Power	Total output power from V_{O1} or V_{O2}		0		66[1]	W
I_{O1} or I_{O2}	Output Current	Over V_I range, $I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A		0		2.2[2]	A
I_{O1} - I_{O2}	Output Load Imbalance	$I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A		0		1[3]	A
V_{O1} or V_{O2}	Output Voltage	Includes set point, line, load, $I_{O1} - I_{O2} \leq 0.1$ A, $-40°C \leq T_A \leq 85°C$		14.5[2]	15	15.5[2]	V
ΔReg_{temp}	Temperature Variation	$-40°C \leq T_A \leq 85°C$, $I_{O1} \leq 0.1$ A or $I_{O2} \leq 0.1$ A	V_{O1} or V_{O2}		±1		$\%V_O$
ΔReg_{line}	Line Regulation	Over V_I range, balanced load	V_{O1} or V_{O2}		±0.05	±0.5	$\%V_O$
ΔReg_{load}	Load Regulation	Over I_{O1} or I_{O2} range, balanced load	V_{O1} or V_{O2}		±0.1	±1	$\%V_O$
η	Efficiency	$I_{O1} = I_{O2}$			90%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, C_O = 10 μF tantalum capacitor			50	100[4]	mV_{pp}
t_{tr}	Transient Response	0.1 A/μs load step, 50% to 75% I_{O1} or I_{O2} maximum			30		μs
ΔV_{tr}		V_{O1} or V_{O2} overshoot/undershoot			±1		$\%V_O$
$I_O$trip	Over Current Threshold	V_I = 36 V, reset followed by auto-recovery		2.45	3	3.85	A
	Short Circuit Current	Continuous overcurrent trip, $I_{O1} = I_{O2}$	$I_{O1(pk)}$ $I_{O2(pk)}$		4.5		A
			Duty		10%		
$V_{O1(adj)}$, $V_{O2(adj)}$	Output Voltage Adjust Range	V_{O1} and V_{O2} adjust simultaneously		7.2		16.7	V
f_S	Switching Frequency	Over V_I and I_O ranges		440	480[5]	520	kHz
V_I on	Under-Voltage Lockout	V_I increasing			33		V
V_I off		V_I decreasing			32		
	On/Off Enable (pin 3)	Referenced to $-V_I$ (pin 4)					
V_{IH}	High-level input voltage			3.6		75[6]	V
V_{IL}	Low-level input voltage			–0.2		0.8	
I_{IL}	Low-level input current					–1	mA
I_I standby	Standby Input Current	Pin 3 open circuit			2		mA
t_{ON}	Start-up Time	$I_{O1} \leq 1$ A or $I_{O2} \leq 1$ A, V_{O1} or V_{O2} or rising 0 to 0.95 (typ)		6	12	18	ms
C_I	Internal Input Capacitance				3		μF
C_O	External Output Capacitance	Capacitance from either output to COM (pin 6)		0		3000[7]	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, T_A = 40°C, ground benign		2.8			10^6 hrs

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(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) Under balanced load conditions, load current flowing out of V_{O1} is balanced to within ±0.1 A of that flowing into V_{O2}.
(3) A load imbalance is the difference in current flowing from V_{O1} to V_{O2}. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10-μF tantalum capacitor connected from V_{O1} (pin 5) or V_{O2} (pin 8), to COM (pin 6).
(5) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(6) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to V_I. The open-circuit voltage is 5 V maximum. If it is left open circuit the converter operates when input power is applied.
(7) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

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DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	**NO.**	
$+V_I$ (1)	1	The positive input supply for the module with respect to V_I (or ground return). When powering the module from a –48 V telecom central office supply, this input is connected to the primary system ground.
Sync In	2	This pin is used when the PTB4851x and PTB4850x DC/DC converter modules are used together. Connecting this pin to the *Sync Out* of the PTB4850x module allows the PTB4851x to be synchronized to the same switch conversion frequency as the PTB4850x.
Enable (2)	3	This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to $–V_I$. A logic 0 at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to $–V_I$. **Note:** Connecting this input directly to the *EN Out* pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB4851x) to power up in sequence.
$-V_I$	4	The negative input supply for the module, and the 0 VDC reference for the *Enable*, and *Sync In* signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.
V_{O1}	5	The positive output supply voltage, which is referenced to the *COM* node. The voltage at V_{O1} has the same magnitude, but is the complement to that at V_{O2} .
V_{O2}	8	The negative output supply voltage, which is referenced to the *COM* node. The voltage at V_{O2} has the same magnitude, but is the complement to that at V_{O1} .
COM	6	The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.
V_OAdj	7	Using a single resistor, this pin allows the magnitude of both V_{O1} and V_{O2} to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

(1) Shaded functions indicate signals that are referenced to $-V_I$
(2) Denotes negative logic: Open = Output Off, $–V_I$ = Normal operation.

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TYPICAL CHARACTERISTICS

PTB4851xA CHARACTERISTIC DATA at V_I = 48 V (1) (2)

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

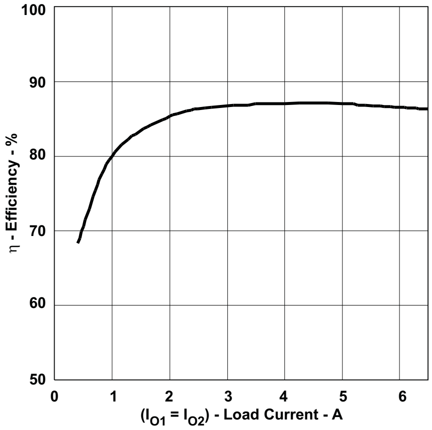
EFFICIENCY
vs
LOAD CURRENT

Figure 1. (1)

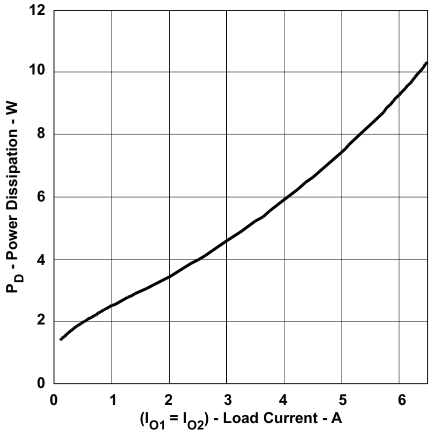
POWER DISSIPATION
vs
LOAD CURRENT

Figure 2. (1)

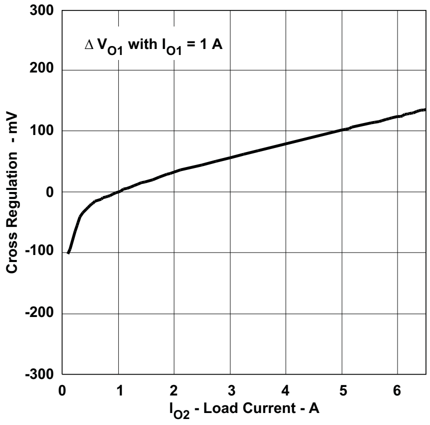
CROSS REGULATION

Figure 3.

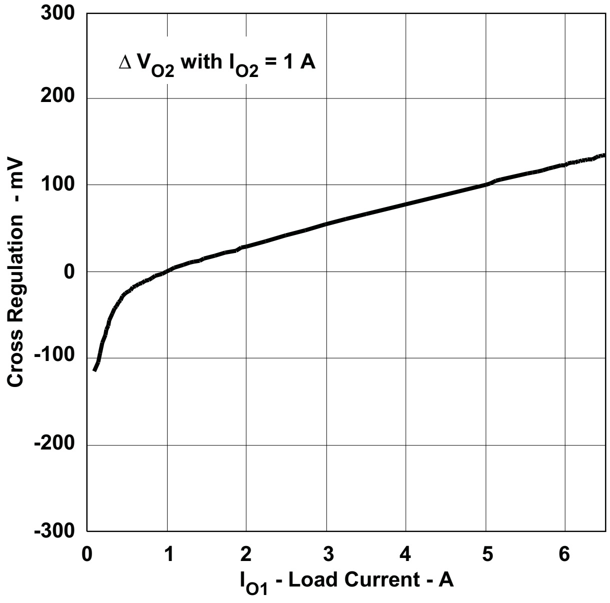
CROSS REGULATION

Figure 4.

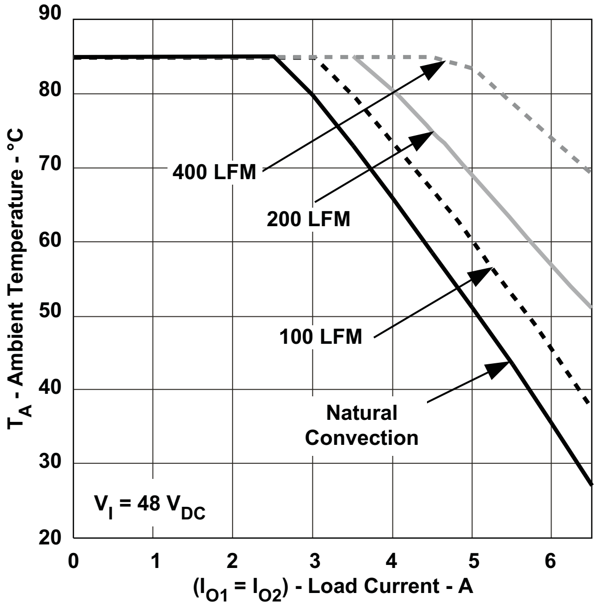
SAFE OPERATING AREA

Figure 5. (1) (2)

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(1) Under a balanced load, current flowing out of V_{O1} is equal to that flowing into V_{O2}.
(2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

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TYPICAL CHARACTERISTICS (Continued)

PTB4851xB CHARACTERISTIC DATA at V_I = 48 V (1) (2)

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

EFFICIENCY
vs
LOAD CURRENT

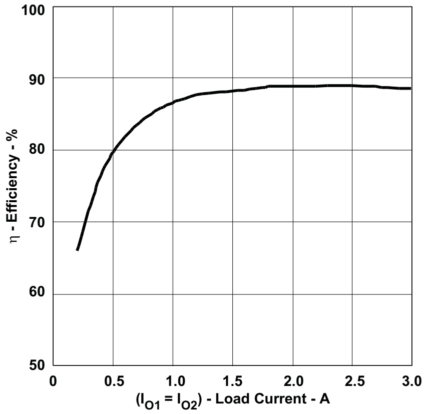

Figure 6. (1)

POWER DISSIPATION
vs
LOAD CURRENT

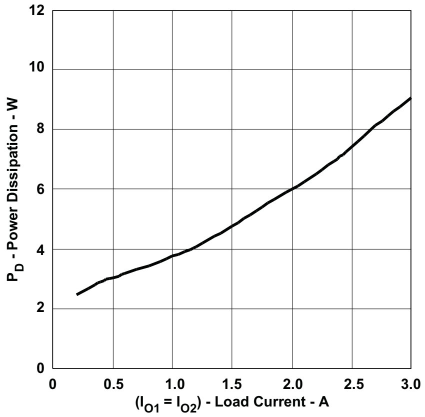

Figure 7. (1)

CROSS REGULATION

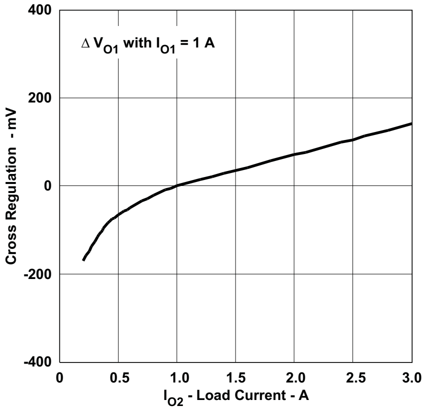

Figure 8.

CROSS REGULATION

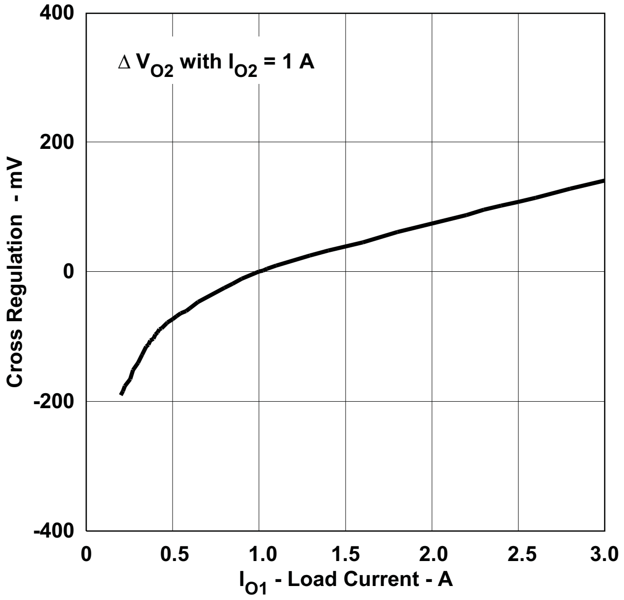

Figure 9.

SAFE OPERATING AREA

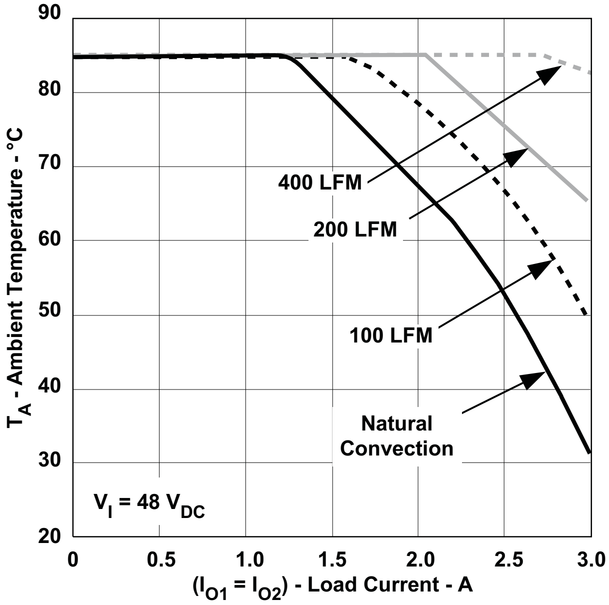

Figure 10. (1) (2)

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(1) Under a balanced load, current flowing out of V_{O1} is equal to that flowing into V_{O2}.
(2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

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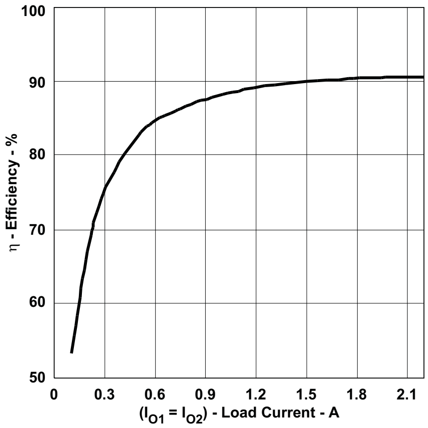
TYPICAL CHARACTERISTICS (Continued)

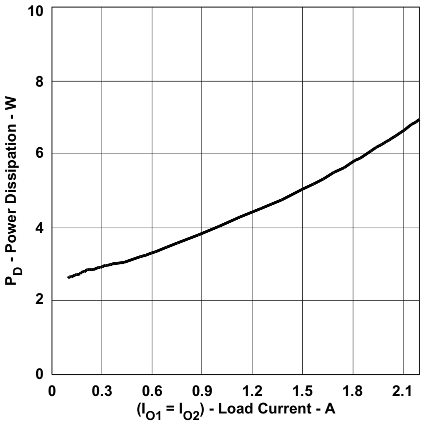
PTB4851xC CHARACTERISTIC DATA at V_I = 48 V (1) (2)

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.



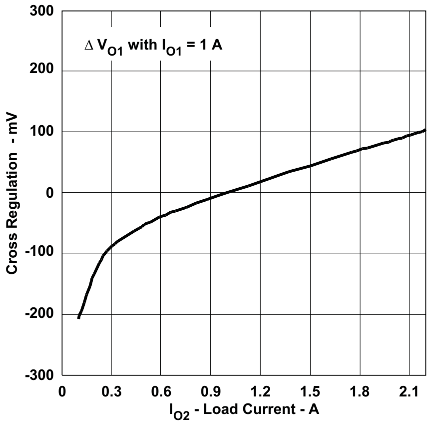
EFFICIENCY vs LOAD CURRENT

Figure 11. (1)



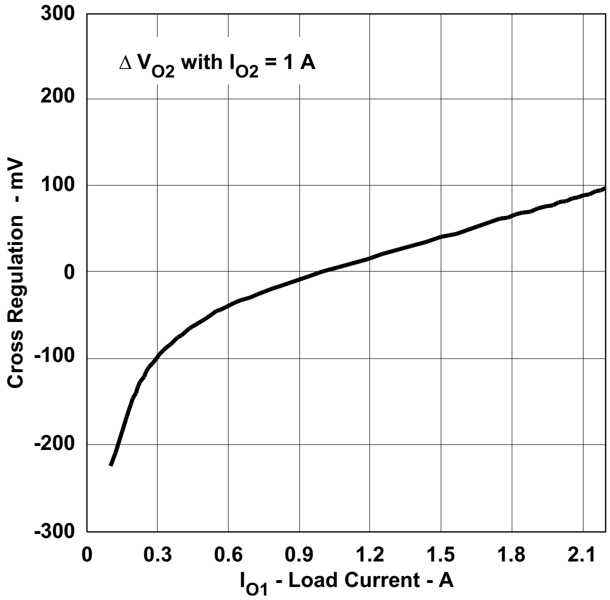
POWER DISSIPATION vs LOAD CURRENT

Figure 12. (1)



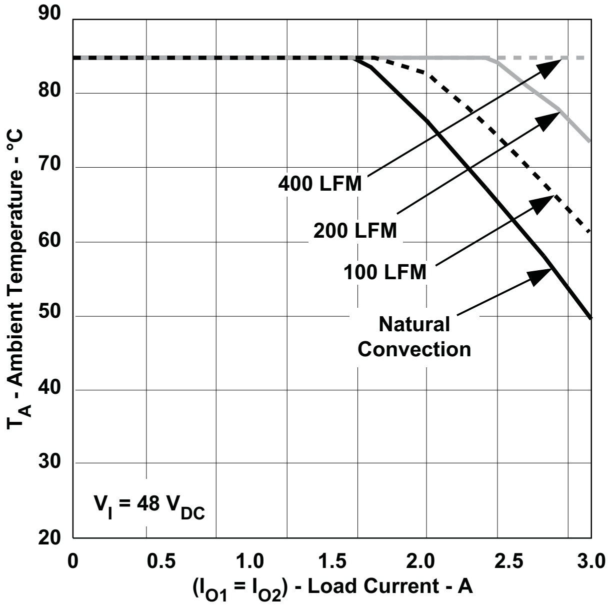
CROSS REGULATION

Figure 13.



CROSS REGULATION

Figure 14.



SAFE OPERATING AREA

Figure 15. (1) (2)

(1) Under a balanced load, current flowing out of V_{O1} is equal to that flowing into V_{O2}.
(2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

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APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE OF THE PTB4851x SERIES OF DC/DC CONVERTERS

The PTB48510 and PTB48511 DC/DC converters produce a balanced pair of complimentary output voltages. They are identified V_{O1} and V_{O2}, respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower, by up to ±10% of their nominal. The adjustment method uses a single external resistor.[1] The value of the resistor determines the adjustment magnitude, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in Table 1. The placement of each resistor is as follows.

Adjust Up: To increase the magnitude of both output voltages, place a resistor R_1 between $V_{O\ 1}Adj$ (pin 7) and the V_{O2} (pin 8) voltage rail; see Figure 16.

Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R_2), between V_OAdj (pin 7) and the V_{O1} (pin 5) voltage rail; see Figure 17.

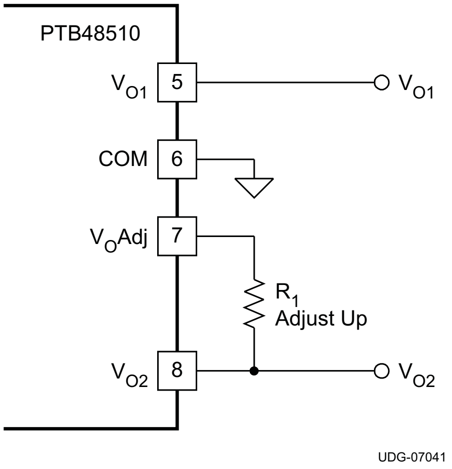

Figure 16. Adjust Up Resistor Placement

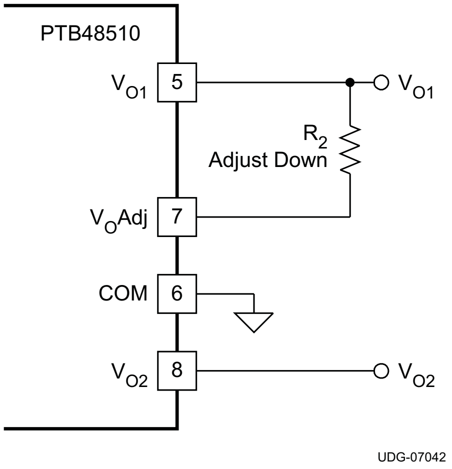

Figure 17. Adjust Down Resistor Placement

ADJUST RESISTOR CALCULATION

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R_1 to adjust up, or (R_2) to adjust down.

$$R_1\ [\text{Adjust Up}] = \frac{V_r\,R_o}{2\left(V_a - V_o\right)} - R_s\ \text{k}\Omega \tag{1}$$

$$\left(R_2\right)\ [\text{Adjust Down}] = \frac{R_o\left(2\,V_a - V_r\right)}{2\,\left(V_o - V_a\right)} - R_s\ \text{k}\Omega \tag{2}$$

Where:

V_O = Magitude of the original V_{O1} or V_{O2}
V_a = Magnitude of the adjusted voltage
V_r = The reference voltage from Table 1
R_O = The resistance value in Table 1
R_S = The series resistance from Table 1

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Table 1. Adjustment Range and Formula Parameters

PARAMETERS	PTB4851xA	PTB4851xB	PTB48510C
V_O(nom) (V)	5	12	15
V_a(min) (V)	3.5	6.5	7.2
V_a(max) (V)	5.5	13.4	16.7
$V_{r\ (V)}$	2.495	2.495	2.495
R_n (kΩ)	7.5	18.2	22.1
R_s (kΩ)	9.09	16.9	16.9

NOTES:

1. A 0.05 W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the R_1 or (R_2) location, as close to the converter as possible.
2. Never connect capacitors to the *Vo Adj* pin. Capacitance added to this pin can affect the stability of the regulated output.
3. **The overvoltage protection (PTB48511x)** is nominally set to 25% above the original output voltage set-point. Increasing the magnitude of the output voltages reduces the margin between the output voltage and the overvoltage (OV) protection threshold. This could make the module more sensitive to OV faults, as a result of random noise and load transients.

   Note: An OV fault is a latched condition that shuts down the converter's outputs. The fault can be cleared by cycling the Enable pin, or by momentarily removing input power to the module.

CONFIGURING THE PTB4850x and PTB4851x DC/DC CONVERTERS FOR DSL APPLICATIONS

When operated as a pair, the PTB4850x and PTB4851x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB4851x produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB4851x may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 19 shows the required cross-connects between the two converters to enable these two features.

SWITCHING FREQUENCY SYNCHRONIZATION

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter’s switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

POWER-UP SEQUENCING

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be assured if the PTB4850x and PTB4851x are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the *EN Out* pin of the PTB4850x is directly connected to the activelow *Enable* input of the PTB4851x (see Figure 19). This allows the PTB4850x to momentarily hold off the outputs from the PTB4851x until the logic-level voltages have risen first. Figure 19 shows the power-up waveforms of all four supply voltages from the schematic of Figure 19.

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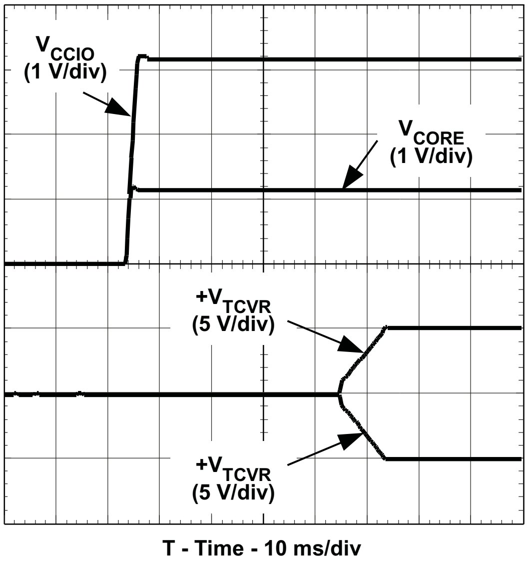

Figure 18. Power-Up Sequencing Waveforms

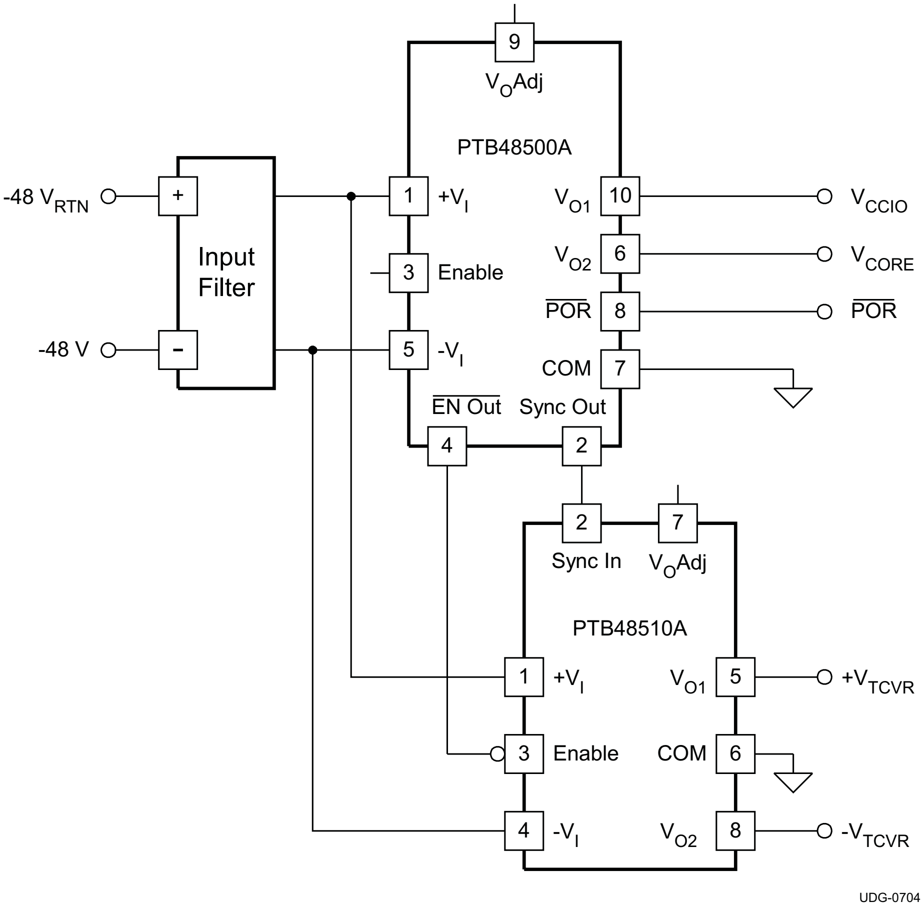

Figure 19. Example of PTB4850x and PTB4851x Modules Configured for DSL Applications

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTB48510AAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48510BAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48510BAS	NRND	Surface Mount Module	ERL	8	9	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		
PTB48510BAZ	NRND	Surface Mount Module	ERL	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTB48510CAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48510CAZ	NRND	Surface Mount Module	ERL	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTB48511AAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48511AAS	OBSOLETE	Surface Mount Module	ERL	8		TBD	Call TI	Call TI	-40 to 85		
PTB48511BAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48511BAZ	NRND	Surface Mount Module	ERL	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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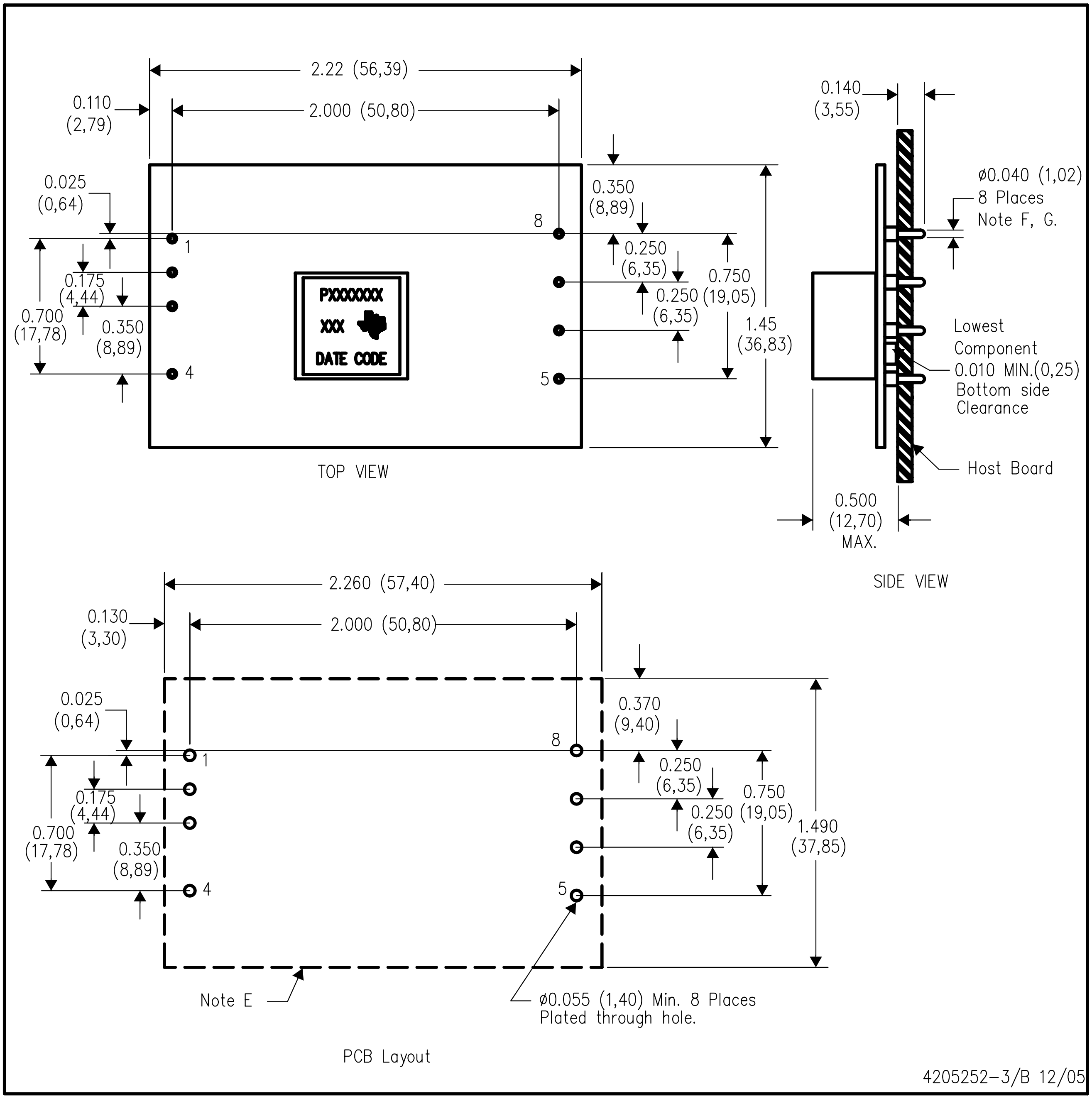
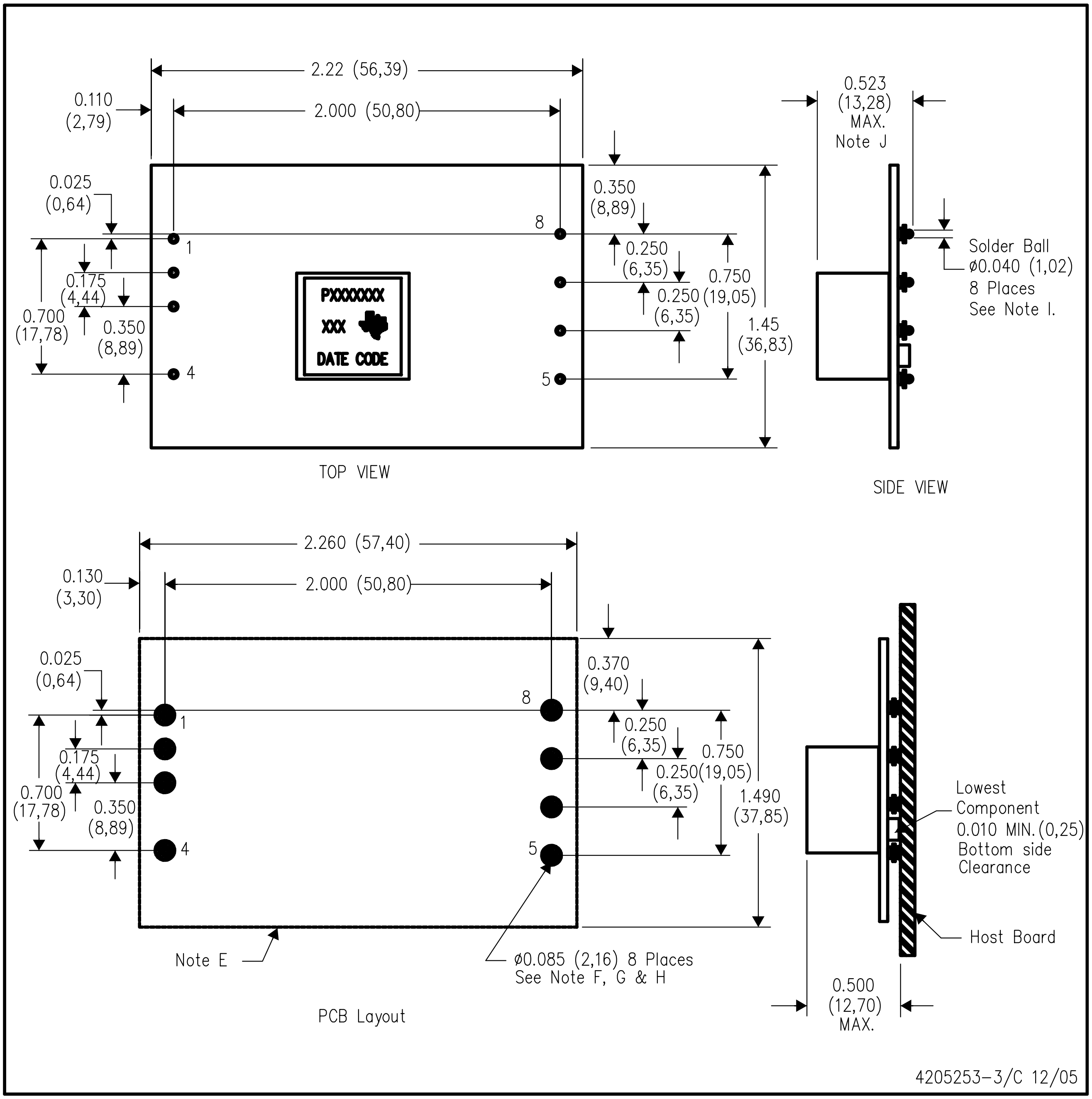
ERK (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.020 (±0,51mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended keep out area for user components.
- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material – Copper Alloy
  Finish – Tin (100%) over Nickel plate

ERL (R–PDSS–B8) DOUBLE SIDED MODULE



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.020 (±0,51mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended keep out area for user components.
- F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material – Copper Alloy
  Finish – Tin (100%) over Nickel plate
  Solder Ball – See product data sheet.
- J. Dimension prior to reflow solder.

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