## Dual Complementary-Output DC/DC Converter for DSL



#### **Features**

- Dual Complementary Outputs (±5 V, ±12 V)
- Input Voltage Range: 36 V to 75 V
- On/Off Enable for Sequencing
- 1500 VDC Isolation
- Over-Current Protection
- Over-Temperature Shutdown
- Under-Voltage Lockout

- Temp Range: -40 to +85 °C
- Industry Standard Outline
- Fixed Frequency Operation
- Synchronizes with PTB48500
- Powers line driver ICs for AC-7 and other xDSL chipsets
- Safety Approvals: (Pending): EN60950 UL/cUL60950

## **Description**

The PTB48580 series of isolated DC/DC converter modules produce a complementary pair of regulated supply voltages for powering line-driver ICs in xDSL telecom applications. The modules operate from a standard telecom (-48 V) central office (CO) supply and can provide up to a 30 W of power in a balanced load configuration.

The A-suffix module (±5 V) is designed to power the line driver ICs for the AC-7 ADSL chipset. Other voltage options will power other analog applications requiring a complementary supply with relatively balanced loads. The outputs can also be easily configured for single-ended use.

The modules incorporate an On/Off enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO) as standard features.

The control inputs, "Enable" and "Sync In," are compatible with the "EN Out" and "Sync Out" signals of the PTB48500 DC/DC converter. This allows the power-up and switching frequency of the PTB48580 series to be directly controlled from a PTB48500. Together a PTB48500 and a PTB48580A converter meet all the system power and sequencing requirements of an AC-7 ADSL chipset.

The PTB48580 series uses doublesided surface mount contruction. The package size is based on an industry standard outline and does not require a heatsink. Both through-hole and surface mount pin configurations are available.

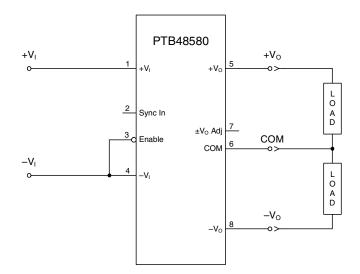
### **Pin Configuration**

Pin	Function
1	$+V_{I}$
2	Sync In
3	Enable *
4	$-V_{I}$
5	$+V_{O}$
6	COM
7	V <sub>O</sub> Adjust
0	<b>T</b> 7

Shaded functions indicate signals that are referenced to  $-V_I$ .

\* Denotes negative logic: Open = Outputs Off  $-V_I$  = Normal operation

## **Stand-Alone Application**





#### **Ordering Information**

Base Pt. No.	(PTB48580xxx)	Output Vo	oltage (PTB48580□xx)	Package Options (PT48580x□□)		
Order Prefix	Description	Code	Voltage	Code	Description	Pkg Ref. (1)
PTB48580xxx	Basic Model	A	±5 V	AH	Horiz. T/H	(ERV)
		В	±12 V	AS	SMD, Standard (2)	(ERS)

Notes: (1) Reference the applicable package reference drawing for the dimensions and PC board layout

(2) "Standard" option specifies 63/37, Sn/Pb pin solder material.

### **Pin Descriptions**

**+V<sub>I</sub>:** The positive input supply for the module with respect to  $-V_I$ . When powering the module from a -48 V telecom central office supply, this input is connected to the primary system ground.

**-V<sub>i</sub>:** The negative input supply for the module, and the 0 VDC reference for the 'Enable\*', and 'Sync In' signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.

**+V<sub>0</sub>:** The positive output supply voltage, which is referenced to the 'COM' node. The voltage at '+ $V_O$ ' has the same magnitude, but is the complement to that at '- $V_O$ '.

**-V<sub>0</sub>:** The negative output supply voltage, which is referenced to the 'COM' node. The voltage at '- $V_0$ ' has the same magnitude, but is the complement to that at '+ $V_0$ '.

**COM:** The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.

 $\pm V_0$  **Adjust:** Using a single resistor, this pin allows the magnitude of both ' $\pm V_0$ ' and ' $\pm V_0$ ' to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

**Enable\*:** This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to  $-V_I$ . A logic '0' at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to  $-V_I$ . Note: Connecting this input directly to the "EN Out" pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB48580) to power up in sequence.

**Sync In:** This pin is used when the PTB48580 and PTB4850x DC/DC converter modules are used together. Connecting this pin to the 'Sync Out' of the PTB4850x module allows the PTB48580 to be synchronized to the same switch conversion frequency as the PTB4850x.

## Environmental and General Specifications (Unless otherwise stated, all voltages are with respect to -V<sub>I</sub>)

Characteristics	Symbols	Conditions	Min	Тур	Max	Units
Input Voltage Range	$V_{\rm I}$	Over output load range	36	48	75	VDC
Isolation Voltage Capacitance Resistance		Input-output/input-case Input to output Input to output	$\frac{1500}{10}$	1500 —	=	V pF MΩ
Operating Temperature Range	$T_A$	Over V <sub>I</sub> Range	-40	_	+85	°C
Over-Temperature Protection	OTP	Shutdown threshold Hysterisis	_	115 <sup>(i)</sup> 10	=	°C
Solder Reflow Temperature	$T_{REFLOW}$	Surface temperature of module body or pins			235 (ii)	°C
Storage Temperature	$T_S$	_	-40	_	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	_	500	_	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 T/H 20-2000 Hz SMD	_	20 5	_	G's
Weight	_		_	13.5	_	grams
Flammability	_	Meets UL 94V-O				

lotes: (i) This parameter is guaranteed be design

(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.



**Specifications** (Unless otherwise stated,  $T_A = 25^{\circ}\text{C}$ ,  $V_I = 48 \text{ V}$ ,  $C_I = 0 \text{ } \mu\text{F}$ ,  $\pm C_O = 0 \text{ } \mu\text{F}$ ,  $|\pm I_O| = |-I_O|$ , and  $|\pm I_O| = 0.5 \text{ } |\pm I_O| \text{max}$ )

			PTB48580A				
Characteristic	Symbol	Conditions	Min	Тур	Max	Units	
Output Power	Po	Total output power from ±V <sub>O</sub>	0	_	30 (1)	W	
Output Current	±I <sub>O</sub>	Over $V_I$ range, $ +I_O  -  -I_O  \le 0.1 \text{ A}$	0	_	3 (2)	A	
Output Load Imbalance	+I <sub>O</sub>   -  -I <sub>O</sub>	+I <sub>O</sub>   ≥0.1 A,  -I <sub>O</sub>   ≥ 0.1 A	0	_	1 (3)	A	
Output Voltage	$ \pm V_{\rm O} $	Inleudes set-point, line, $ +I_{\rm O}  -  -I_{\rm O}  \le 0.1$ A $-40 \le \Gamma_{\rm A} \le +85^{\circ}{\rm C}$	4.75 (2)	5	5.25 (2)	V	
Temperature Variation	$\Delta \mathrm{Reg}_{\mathrm{temp}}$	$-40 \le \Gamma_A \le +85^{\circ}\text{C},  \pm I_O  = 0.1 \text{ A}$ $\pm V_O$	_	±1	_	$%V_{O}$	
Line Regulation	$\Delta \mathrm{Reg}_{\mathrm{line}}$	Over V <sub>I</sub> range, balanced load ±V <sub>O</sub>	_	±0.1	±0.4	$%V_{O}$	
Load Regulation	$\Delta \text{Reg}_{\text{load}}$	Over ±I <sub>O</sub> range, balanced load ±V <sub>O</sub>	_	±0.2	±0.4	$%V_{O}$	
Efficiency	η	$P_O = P_O \max$	_	86	_	%	
$V_{o}$ Ripple (pk-pk)	±Vr	20 MHz bandwidth, C <sub>O</sub> =10 µF tantalum capacitor	_	25	50 (4)	$\mathrm{mV}_\mathrm{pp}$	
Transient Response	$t_S$	$0.1$ A/µs load step, 50% to 75% $\pm I_O$ max	_	30	_	μs	
	$\Delta { m V_O}{ m pk}$	±V <sub>O</sub>   over/undershoot	_	±1	_	$%V_{O}$	
Over Current Threshold	$I_{O}$ trip	$ m V_I$ =36 V reset followed by auto-recovery	3.3	4.3	5.3	A	
Short Circuit Current		Continuous over-current trip, $\pm I_O _{PK}$	_	6.5	_	A	
		+I <sub>O</sub>   =  -I <sub>O</sub>   Duty	_	10	_	%	
Output Voltage Adjust Range	±V <sub>O</sub>   adj	$ +V_{\rm O} $ and $ -V_{\rm O} $ adjust simulataneously	3.5	_	6 (5)	V	
Switching Frequency	$f_{S}$	Over $V_I$ and $I_O$ ranges	440	470 (6)	500	kHz	
Under-Voltage Lockout	$egin{array}{c} V_I on \ V_I off \end{array}$	$egin{array}{l} V_I \ \text{increasing} \ V_I \ \text{decreasing} \end{array}$	_	33 32	_	V	
On/Off Enable (pin 3) Input High Voltage Input Low Voltage	$egin{array}{c} V_{IH} \ V_{IL} \end{array}$	Referenced to $-V_I(pin 4)$	+3.6 -0.2	_	+75 <sup>(7)</sup> +0.8	V	
Input Low Current	${ m I}_{ m IL}$		_	_	-1	mA	
Standby Input Current	I <sub>I</sub> standby	pin 3 open circuit	_	2	_	mA	
Start-up Time	t <sub>ON</sub>	$ \pm I_{\rm O} $ =1 A, $ \pm V_{\rm O} $ rising 0 to 0.95 $ \pm V_{\rm O} $ TYP	_	10	_	ms	
Internal Input Capacitance	$C_{I}$		_	2	_	μF	
External Output Capacitance	C <sub>O</sub>	Capacitance from either output to COM (pin 6)	0	_	2,000 (8)	μF	
Reliability	MTBF	Per Telcordia SR-332 50% stress, T <sub>A</sub> =40°C, ground benign	2.8	_	_	106 Hrs	

- Notes: (1) See Safe Operating Area curves or contact the factory for the appropriate derating.

  (2) Under balanced load conditions, load current flowing out of +V<sub>O</sub> is balanced to within ±0.1 A of that flowing into -V<sub>O</sub>.

  (3) A load imbalance is the difference in current flowing from +V<sub>O</sub> to -V<sub>O</sub>. The module can operate with a higher imbalance but with reduced specifications.

  (4) Output voltage ripple is measured with a 10 µF tantalum capacitor connected from +V<sub>O</sub> (pin 5) or -V<sub>O</sub> (pin 8), to COM (pin 6).

  (5) When the output voltage is adjusted higher than the nominal output voltage the load current must not exceed the module's maximum power rating.

  (6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.

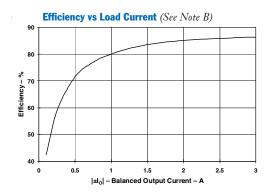
  (7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to +V<sub>I</sub>. The open-circuit voltage is TV max. If it is left open circuit the converter will operate when input power is applied.

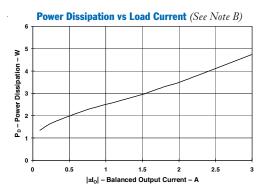
  (8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.
  - capacitors with organic, or polymer-aluminum type electrolytes.

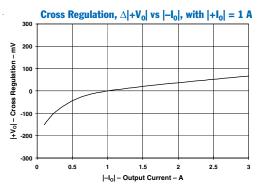
Dual Complementary-Output DC/DC Converter for DSL

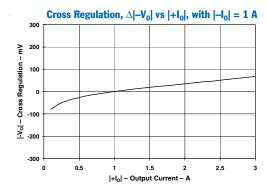
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## PTB48580A Characteristic Data @V<sub>I</sub> =48 V (See Notes A)

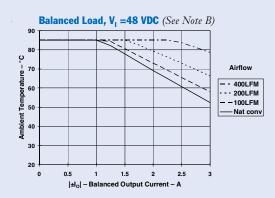








## **Safe Operating Area PTB48580A** (See Note C)



Note A: Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

Note B: Under a balanced load, current flowing out of  $+V_O$  is equal to that flowing into  $-V_O$ .

Note C: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in.  $\times$  4 in. double-sided PCB with 2 oz. copper.



## **Dual Complementary-Output DC/DC Converter for DSL**

**Specifications** (Unless otherwise stated,  $T_A = 25^{\circ}\text{C}$ ,  $V_I = 48 \text{ V}$ ,  $C_I = 0 \text{ }\mu\text{F}$ ,  $\pm C_O = 0 \text{ }\mu\text{F}$ ,  $|\pm I_O| = |-I_O|$ , and  $|\pm I_O| = 0.5 \text{ }|\pm I_O| \text{max}$ )

				PTB48580B				
Characteristic	Symbol	Conditions	Min	Тур	Max	Units		
Output Power	Po	Total output power from ±V <sub>O</sub>	0	_	30 (1)	W		
Output Current	±I <sub>O</sub>	Over $V_I$ range, $ +I_O - -I_O  \le 0.1$ A	0	_	1.25 (2)	A		
Output Load Imbalance	+I <sub>O</sub>   -  -I <sub>O</sub>	+I <sub>O</sub>   ≥0.1 A,  -I <sub>O</sub>   ≥ 0.1 A	0	_	0.5 (3)	A		
Output Voltage	$ \pm V_{\rm O} $	Inlcudes set-point, line, $ +I_{\rm O}  -  -I_{\rm O}  \le 0.1$ A $-40 \le \Gamma_{\rm A} \le +85^{\circ}{\rm C}$	11.6 (2)	12	12.4 (2)	V		
Temperature Variation	$\Delta \mathrm{Reg}_{\mathrm{temp}}$	$-40 \le \Gamma_A \le +85^{\circ}\text{C},  \pm I_O  = 0.1 \text{ A}$ $\pm V_O$	_	±1	_	$%V_{O}$		
Line Regulation	$\Delta \text{Reg}_{\text{line}}$	Over V <sub>I</sub> range, balanced load ±V <sub>O</sub>	_	±0.1	±0.5	$%V_{O}$		
Load Regulation	$\Delta \text{Reg}_{\text{load}}$	Over ±I <sub>O</sub> range, balanced load ±V <sub>O</sub>	_	±0.1	±1	$%V_{O}$		
Efficiency	η	$P_O = P_O \max$	_	88	_	%		
$V_{o}$ Ripple (pk-pk)	±Vr	20 MHz bandwidth, C <sub>O</sub> =10 µF tantalum capacitor	_	50	100 (4)	$\mathrm{mV}_\mathrm{pp}$		
Transient Response	$t_S$	$0.1$ A/µs load step, 50% to 75% $\pm I_{O}$ max	_	30	_	μs		
	$\Delta { m V_O}{ m pk}$	±V <sub>O</sub>   over/undershoot	_	±1	_	$%V_{O}$		
Over Current Threshold	$I_{O}$ trip	$V_{\rm I}$ =36 V reset followed by auto-recovery	1.4	1.9	2.4	A		
Short Circuit Current		Continuous over-current trip, $ \pm I_O _{PK}$	_	3	_	A		
		+I <sub>O</sub>   =  -I <sub>O</sub>   Duty	_	10	_	%		
Output Voltage Adjust Range	±V <sub>O</sub>   adj	$ +V_{\rm O} $ and $ -V_{\rm O} $ adjust simulataneously	6.5	_	13.4 (5)	V		
Switching Frequency	$f_{\mathrm{S}}$	Over $V_I$ and $I_O$ ranges	440	480 (6)	520	kHz		
Under-Voltage Lockout	$egin{array}{c} V_{I}on \ V_{I}off \end{array}$	$V_{ m I}$ increasing $V_{ m I}$ decreasing	_	33 32	_	V		
On/Off Enable (pin 3) Input High Voltage Input Low Voltage	$egin{array}{c} V_{ m IH} \ V_{ m IL} \end{array}$	Referenced to $-V_I(pin 4)$	+3.6 -0.2	_	+75 <sup>(7)</sup> +0.8	V		
Input Low Current	${ m I}_{ m IL}$		_	_	-1	mA		
Standby Input Current	${ m I_I}$ standby	pin 3 open circuit	_	2	_	mA		
Start-up Time	t <sub>ON</sub>	$ \pm I_{\rm O} $ =1 A, $ \pm V_{\rm O} $ rising 0 to 0.95 $ \pm V_{\rm O} $ TYP	_	10	_	ms		
Internal Input Capacitance	$C_{\mathrm{I}}$		_	2	_	μF		
External Output Capacitance	Co	Capacitance from either output to COM (pin 6)	0	_	1,500 (8)	μF		
Reliability	MTBF	Per Telcordia SR-332 50% stress, T <sub>A</sub> =40°C, ground benign	2.8		_	106 Hrs		

- Notes: (1) See Safe Operating Area curves or contact the factory for the appropriate derating.

  (2) Under balanced load conditions, load current flowing out of +V<sub>O</sub> is balanced to within ±0.1 A of that flowing into -V<sub>O</sub>.

  (3) A load imbalance is the difference in current flowing from +V<sub>O</sub> to -V<sub>O</sub>. The module can operate with a higher imbalance but with reduced specifications.

  (4) Output voltage ripple is measured with a 10-µF tantalum capacitor connected from +V<sub>O</sub> (pin 5) or -V<sub>O</sub> (pin 8), to COM (pin 6).

  (5) When the output voltage is adjusted higher than the nominal output voltage the load current must not exceed the module's maximum power rating.

  (6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.

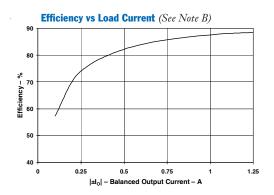
  (7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to +V<sub>I</sub>. The open-circuit voltage is 7 V max. If it is left open circuit the converter will operate when input power is applied.

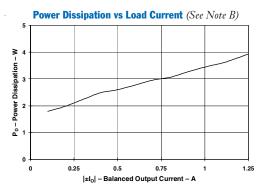
  (8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

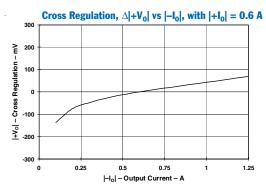
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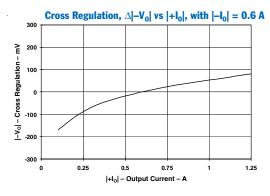
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## PTB48580B Characteristic Data @V<sub>IN</sub> =48 V (See Notes A)

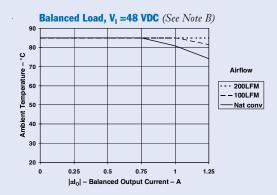








## **Safe Operating Area PTB48580B** (See Note C)



Note A: Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

Note B: Under a balanced load, current flowing out of  $+V_0$  is equal to that flowing into  $-V_0$ .

Note C: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in.  $\times$  4 in. double-sided PCB with 2 oz. copper.



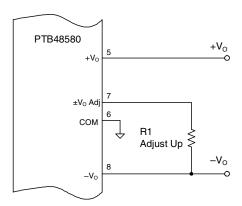
#### PTB48580 Series

## Adjusting the Output Voltages of the PTB48580 Series of DC/DC Converters

The PTB48580 series of DC/DC converters produce a balanced pair of complementary output voltages. They are identified  $+V_O$  and  $-V_O$ , respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower, by up to  $\pm 10\%$  of their nominal. The adjustment method uses a single external resistor. <sup>1</sup> The value of the resistor determines the magnitude of the adjustment, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in Table 1-1. The placement of each resistor is as follows.

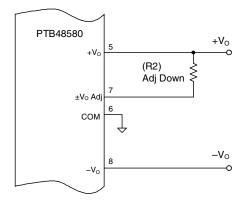
**Adjust Up:** To increase the magnitude  $^{(3)}$  of both output voltages, place a resistor R1 between  $\pm V_O Adj$  (pin 7) and the  $-V_O$  (pin 8) voltage rail; see Figure 1-1(a).

Figure 1-1a



**Adjust Down:** To decrease the magnitude of both output voltages, add a resistor (R2), between  $V_O$  Adj (pin 7) and the  $+V_O$  (pin 5) voltage rail; see Figure 1-1(b).

Figure 1-1b



#### **Calculation of Resistor Adjust Values**

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R1 to adjust up, or (R2) to adjust down.

$$R_{1} \text{ [Adjust Up]} \qquad = \quad \frac{V_{R} R_{O}}{2 (V_{A} - V_{O})} \quad -R_{S} \quad k\Omega$$

$$\begin{array}{ll} (R_2) \; [Adjust \; Down] & = & \underline{R_O \left(2 \; V_A - V_R\right)} \; - R_S \quad k\Omega \\ \hline 2 \left(V_O - V_A\right) \end{array}$$

Where:  $V_O$  = Magitude of the original  $\pm V_O$ 

 $V_{\rm A}$  = Magnitude of the adjusted voltage  $V_{\rm R}$  = The reference voltage from Table 1-1  $R_{\rm O}$  = The resistance value in Table 1-1

 $R_s$  = The series resistance from Table 1-1

Table 1-1

ADJUSTMENT RANGE AND FORMULA PARAMETERS								
Series Pt. No.	PTB48580A	PTB48580B						
V <sub>o</sub> (nom)	5 V	12 V						
V <sub>A</sub> (min)	3.5 V	6.5 V						
V <sub>A</sub> (max) (3)	6 V	13.4 V						
V <sub>R</sub>	2.495 V	2.495 V						
$R_0$ (k $\Omega$ )	7.5	18.2						
R <sub>s</sub> (kΩ)	9.09	16.9						

## **Notes:**

- 1. A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the R1 or (R2) location, as close to the converter as possible.
- 2. Never connect capacitors to the  $\pm V_O Adj$  pin. Capacitance added to this pin can affect the stability of the regulated output.
- 3. When the output voltage is adjusted higher than the nominal output voltage the load current must not exceed the module's maximum power rating of 30 W. For example, when the PTB48580A is adjusted to  $\pm 6$  V (12 V in the single output configuration), the load current is limited to 2.5 A.



PTB48580 Series

# Configuring the PTB48580 Series of DC/DC Converters for DSL Applications

When operated as a pair, the PTB4850x and PTB48580 converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB48580 produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB48580 may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 2-1 shows the required cross-connects between the two converters to enable these two features.

#### **Switching Frequency Synchronization**

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

#### **Power-Up Sequencing**

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be guaranteed if the PTB4850x and PTB48580 are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the "EN Out" pin of the PTB4850x is directly connected to the active-low "Enable" input of the PTB48580 (see Figure 2-1). This allows the PTB4850x to momentarily hold off the outputs from the PTB48580 until the logic-level voltages have risen first. Figure 2-2 shows the power-up waveforms of all four supply voltages from the schematic of Figure 2-1.

Figure 2-2; Power-Up Sequencing Waveforms

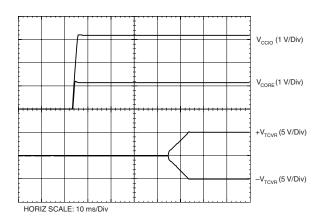
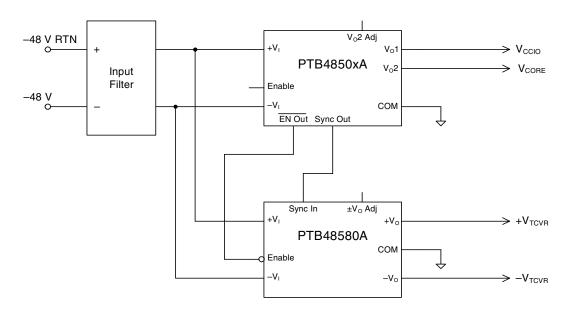


Figure 2-1; Example of PTB4850x & PTB48580A Modules Configured for DSL Applications







30-Jul-2011

### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
PTB48580AAH	ACTIVE	Through- Hole Module	ERV	8	15	Pb-Free (RoHS)	SN	N / A for Pkg Type	
PTB48580AAS	ACTIVE	Surface Mount Module	ERS	8	15	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	
PTB48580AAZ	ACTIVE	Surface Mount Module	ERS	8	15	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	
PTB48580BAH	ACTIVE	Through- Hole Module	ERV	8	15	Pb-Free (RoHS)	SN	N / A for Pkg Type	
PTB48580BAZ	ACTIVE	Surface Mount Module	ERS	8	15	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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30-Jul-2011

#### DOUBLE SIDED MODULE ERS (R-PDSS-T8) - 2.22 (56,39) 0.436 0.110(2,79) 2.000 (50,80) (11,07)MAX. 0.025 - 0.075 (1,90) Note J (0,64)Solder Ball 0.250 (6,35) ↓ Ø0.040 (1,02) 0.750 0.250 (19,05) 8 Places PXXXXXX See Note I. 0.700 (17,78) (6,35)0.90 0.350 XXX (22,86)(8,89)DATE CODE 5 💁 TOP VIEW SIDE VIEW 2.260 (57,40) 0.130(3,30)2.000 (50,80) 0.095 (2,41) 0.025 (0,64)0.250 (6,35) ↓ 0.750 ↑ 0.250(19,05) | 0.940 0.700 10.350 Lowest (6,35)(23,88)Component (8,89)0.010 MIN. (0,25) Bottom side Clearance - Host Board Note E Ø0.085 (2,16) 8 Places See Note F, G & H 0.413 (10,50)PCB Layout MAX. 4206558/A 12/04

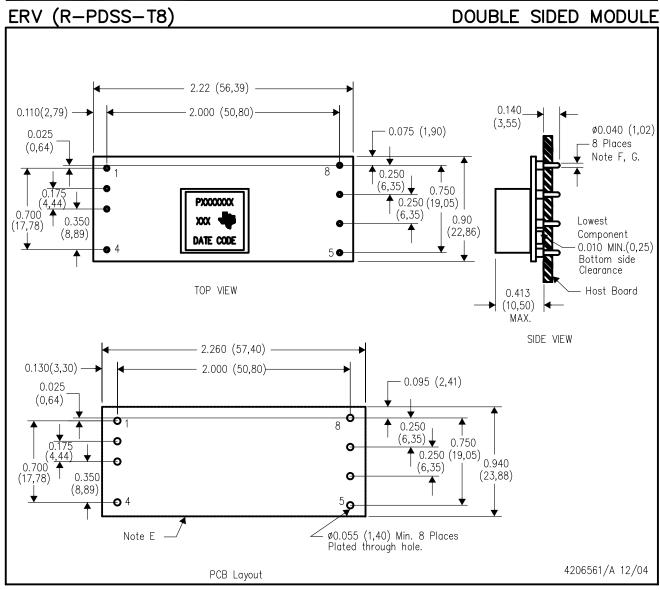
- NOTES: All linear dimensions are in inches (mm).
  - This drawing is subject to change without notice.
  - 2 place decimals are  $\pm 0.020$  ( $\pm 0,51$ mm). 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).

  - E. Recommended keep out area for user components.
    F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material Copper Alloy

Finish — Tin (100%) over Nickel plate Solder Ball — See product data sheet.

J. Dimension prior to reflow solder.





- NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are  $\pm 0.020$  ( $\pm 0,51$ mm).
- D. 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
- E. Recommended keep out area for user components.
- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material Copper Alloy Finish — Tin (100%) over Nickel plate



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