- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**
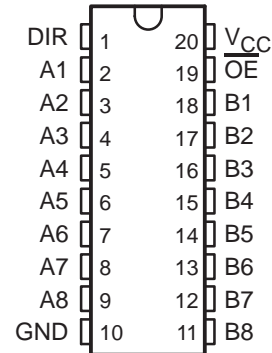
description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.
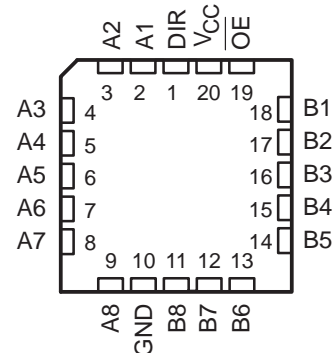
The SN74F245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F245 is characterized for operation from 0°C to 70°C.

SN54F245 . . . J PACKAGE
SN74F245 . . . DB, DW, OR N PACKAGE
(TOP VIEW)

```
         ┌────┬────┐
DIR  [ 1 │    │ 20 ] V_CC
A1   [ 2 │    │ 19 ] OE
A2   [ 3 │    │ 18 ] B1
A3   [ 4 │    │ 17 ] B2
A4   [ 5 │    │ 16 ] B3
A5   [ 6 │    │ 15 ] B4
A6   [ 7 │    │ 14 ] B5
A7   [ 8 │    │ 13 ] B6
A8   [ 9 │    │ 12 ] B7
GND  [ 10│    │ 11 ] B8
         └─────────┘
```

SN54F245 . . . FK PACKAGE
(TOP VIEW)

```
          A2  A1  DIR V_CC OE
           3   2   1   20  19
      ┌───────────────────────┐
A3 [ 4│                       │18 ] B1
A4 [ 5│                       │17 ] B2
A5 [ 6│                       │16 ] B3
A6 [ 7│                       │15 ] B4
A7 [ 8│                       │14 ] B5
      └───────────────────────┘
           9  10  11  12  13
          A8  GND B8  B7  B6
```

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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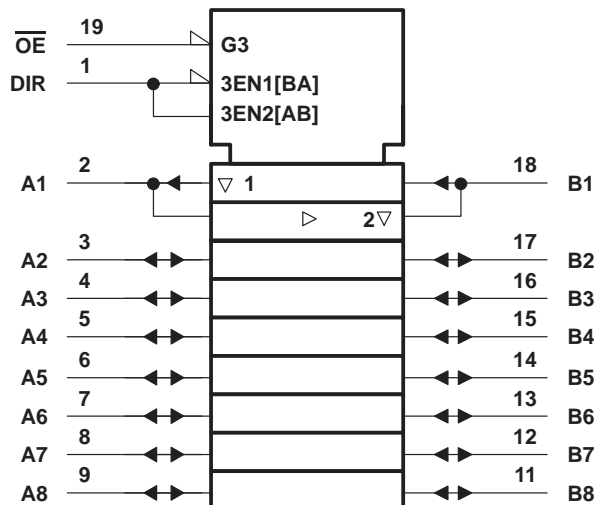**TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SN54F245, SN74F245
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SDFS010A – MARCH 1987 – REVISED OCTOBER 1993

logic symbol†

logic diagram (positive logic)

To Seven Other Channels

† This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.
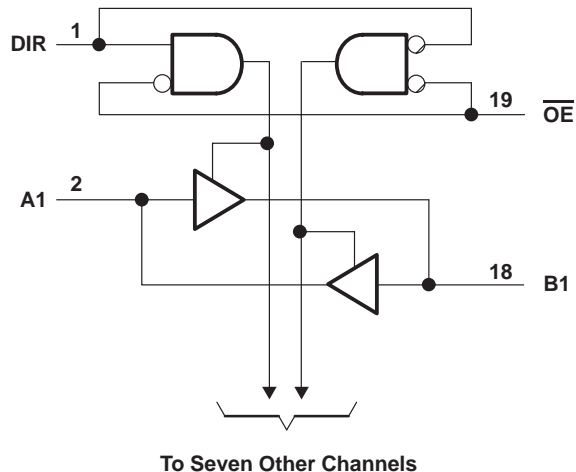
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . −1.2 V to 7 V
Input current range . . . . −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F245 (A1 thru A8) . . . . 40 mA
SN54F245 (B1 thru B8) . . . . 96 mA
SN74F245 (A1 thru A8) . . . . 48 mA
SN74F245 (B1 thru B8) . . . . 128 mA
Operating free-air temperature range: SN54F245 . . . . −55°C to 125°C
SN74F245 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions

			SN54F245			SN74F245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54F245			SN74F245			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}			$V_{CC} = 4.5$ V,	$I_I = −18$ mA			−1.2			−1.2	V
V_{OH}	A1 thru A8	$V_{CC} = 4.5$ V	$I_{OH} = −1$ mA		2.5	3.4		2.5	3.4		V
			$I_{OH} = −3$ mA		2.4	3.3		2.4	3.3		
	B1 thru B8	$V_{CC} = 4.5$ V	$I_{OH} = −12$ mA		2	3.2					
			$I_{OH} = −15$ mA					2	3.1		
	Any output	$V_{CC} = 4.75$ V,	$I_{OH} = −1$ mA to $−3$ mA					2.7			
V_{OL}	A1 thru A8	$V_{CC} = 4.5$ V	$I_{OL} = 20$ mA			0.3	0.5				V
			$I_{OL} = 24$ mA						0.35	0.5	
	B1 thru B8	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.38	0.55				
			$I_{OL} = 64$ mA						0.42	0.55	
I_I	A and B	$V_{CC} = 5.5$ V	$V_I = 5.5$ V				1			1	mA
	DIR, $\overline{OE}$		$V_I = 7$ V				0.1			0.1	
I_{IH}‡	A and B	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V				70			70	μA
	DIR, $\overline{OE}$						20			20	
I_{IL}‡	A and B	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V				−0.65			−0.65	mA
	DIR, $\overline{OE}$						−1.2			−1.2	
I_{OS}§	A1 thru A8	$V_{CC} = 5.5$ V,	$V_O = 0$		−60		−150	−60		−150	mA
	B1 thru B8				−100		−225	−100		−225	
I_{CC}		$V_{CC} = 5.5$ V	Outputs high			70	90		70	90	mA
			Outputs low			95	120		95	120	
			Outputs disabled			85	110		85	110	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F245			SN54F245		SN74F245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.7	3.8	6	1.2	7.5	1.7	7	ns
t_{PHL}			1.7	4.2	6	1.2	7.5	1.7	7	
t_{PZH}	$\overline{OE}$	A or B	2.2	4.9	7	1.7	9	2.2	8	ns
t_{PZL}			2.7	5.6	8	2.2	10	2.7	9	
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.6	6.5	1.7	9	2.2	7.5	ns
t_{PLZ}			1.2	4.6	6.5	1.2	10	1.2	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2:   Load circuits and waveforms are shown in Section 1.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
85511012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8551101RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
8551101SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/34803B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/34803BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
JM38510/34803BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN54F245J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SN74F245DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74F245DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F245N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74F245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F245NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54F245FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54F245J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54F245W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74F245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1
SN74F245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74F245NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F245DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74F245DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74F245DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74F245NSR	SO	NS	20	2000	346.0	346.0	41.0

DIM / PINS ∗∗	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

1   7

C

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

A

0°—15°

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R–GDFP–F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\frac{0.045\ (1,14)}{0.026\ (0,66)}$

$\frac{0.300\ (7,62)}{0.245\ (6,22)}$

$\frac{0.100\ (2,45)}{0.045\ (1,14)}$

$\frac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

1   20

$\frac{0.022\ (0,56)}{0.015\ (0,38)}$

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\frac{0.370\ (9,40)}{0.250\ (6,35)}$ $\frac{0.370\ (9,40)}{0.250\ (6,35)}$

4040180–4/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil–Std 1835 GDFP2–F20

FK (S−CQCC−N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
        D. Falls within JEDEC MS−004

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM / PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

⌒ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/G 01/11
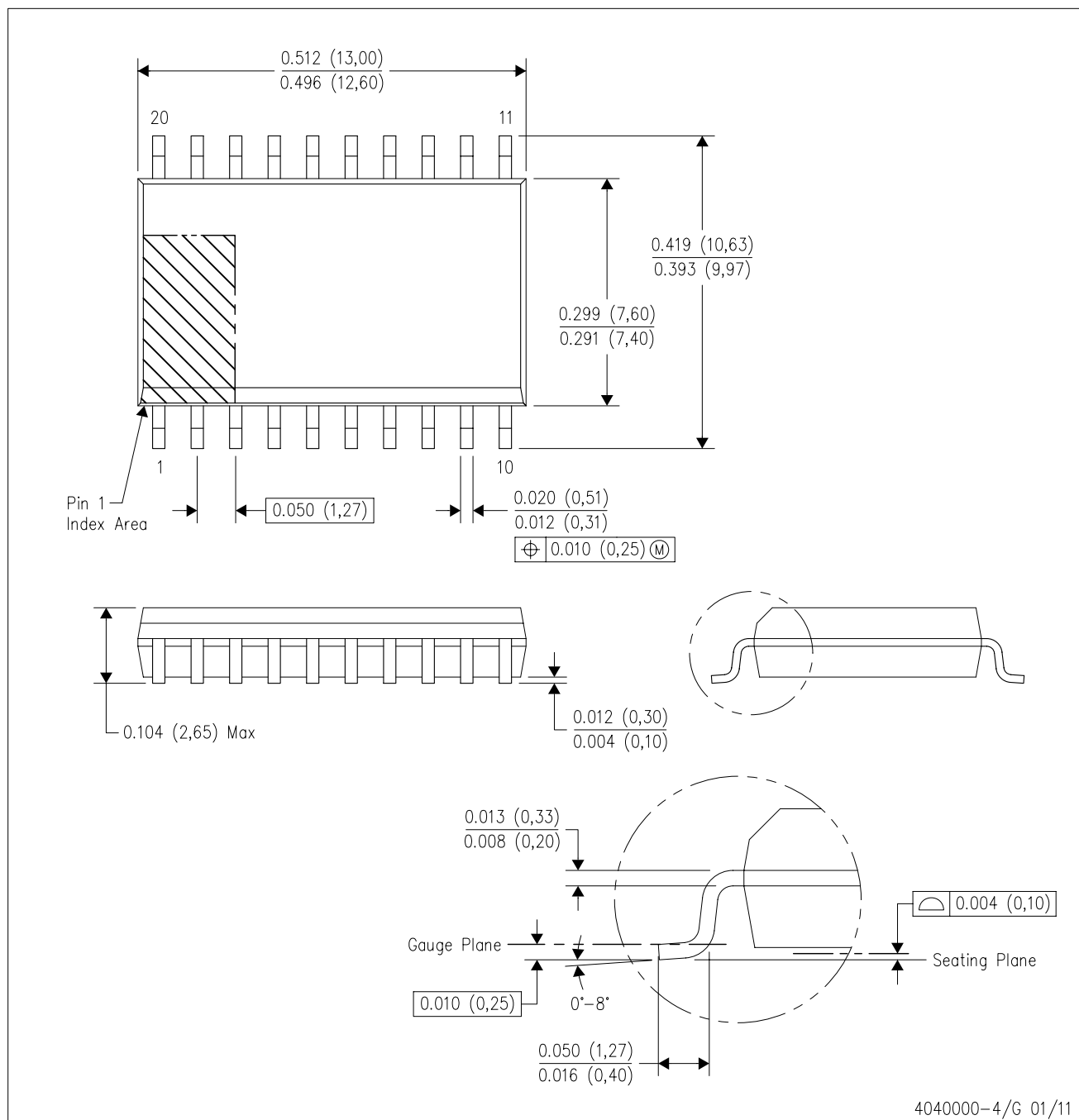
NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE
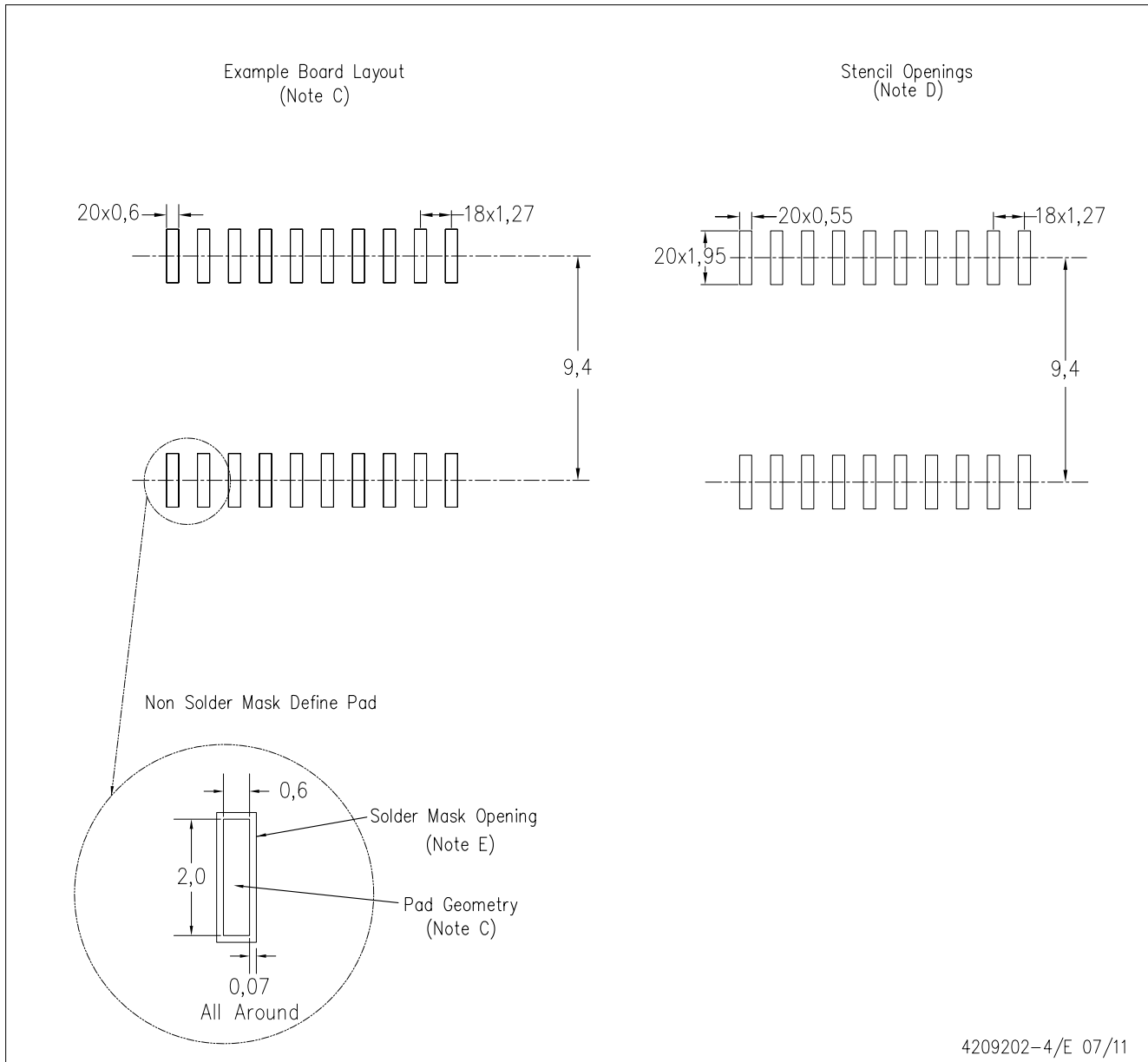
Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6   18x1,27

20x0,55   18x1,27

20x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−4/E 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Refer to IPC7351 for alternate board design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

1,27

0,51
0,35

⊕ 0,25 Ⓜ

0,15 NOM

Gage Plane

0,25

0°–10°

1,05
0,55

5,60
5,00

8,20
7,40

A

0,15
0,05

2,00 MAX

Seating Plane

⬠ 0,10

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

$\frac{0,38}{0,22}$ $\oplus$ 0,15 Ⓜ

28   15

$\frac{5,60}{5,00}$ $\frac{8,20}{7,40}$

$\frac{0,25}{0,09}$

Gage Plane

0,25

0°−8° $\frac{0,95}{0,55}$

1   14

A

2,00 MAX   0,05 MIN

Seating Plane

△ 0,10

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

IMPORTANT NOTICE