TEXAS INSTRUMENTS



### SN65HVD10, SN65HVD10Q, SN75HVD10 SN65HVD11, SN65HVD11Q, SN75HVD11 SN65HVD12, SN75HVD12

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# 3.3-V RS-485 TRANSCEIVERS

#### **FEATURES**

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- Operates With a 3.3-V Supply
- Bus-Pin ESD Protection Exceeds 16 kV HBM
- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Optional Driver Output Transition Times for Signaling Rates <sup>(1)</sup> of 1 Mbps, 10 Mbps, and 32 Mbps
- Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A
- Bus-Pin Short Circuit Protection From –7 V to 12 V
- Low-Current Standby Mode ... 1 µA Typical
- Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver
- Thermal Shutdown Protection
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- SN75176 Footprint

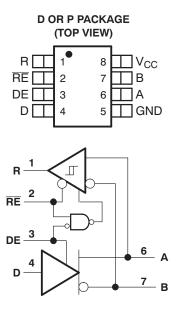
#### **APPLICATIONS**

- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnects
- Electronic Security Stations
- Industrial Process Control
- Building Automation
- Point-of-Sale (POS) Terminals and Networks

## DESCRIPTION

SN65HVD10, The SN75HVD10, SN65HVD11, SN75HVD11, SN65HVD12, and SN75HVD12 combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3-V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control. Very low device standby supply current can be achieved by disabling the driver and the receiver.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/ output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.



 The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### **ORDERING INFORMATION**

SIGNALING		Ŧ	PAC	KAGE	
RATE	UNIT LOADS	T <sub>A</sub>	SOIC <sup>(1)</sup>	PDIP	SOIC MARKING
32 Mbps	1/2		SN65HVD10D	SN65HVD10P	VP10
10 Mbps	1/8	–40°C to 85°C	SN65HVD11D	SN65HVD11P	VP11
1 Mbps	1/8		SN65HVD12D	SN65HVD12P	VP12
32 Mbps	1/2		SN75HVD10D	SN75HVD10P	VN10
10 Mbps	1/8	–0°C to 70°C	SN75HVD11D	SN75HVD11P	VN11
1 Mbps	1/8		SN75HVD12D	SN75HVD12P	VN12
32 Mbps	1/2	-40°C to 125°C	SN65HVD10QD	SN65HVD10QP	VP10Q
10 Mbps	1/8		SN65HVD11QD	SN65HVD11QP	VP11Q

(1) The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN75HVD11DR).

## **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted <sup>(1) (2)</sup>

				UNIT
V <sub>CC</sub>	Supply voltage rang	ge		–0.3 V to 6 V
	Voltage range at A	or B		–9 V to 14 V
	Input voltage range	at D, DE, R or RE		–0.5 V to V <sub>CC</sub> + 0.5 V
	Voltage input range	e, transient pulse, A and B, throug	h 100 Ω, see Figure 11	–50 V to 50 V
lo	Receiver output cur	rrent		-11 mA to 11 mA
		Human body model <sup>(3)</sup>	A, B, and GND	±16 kV
	Electrostatic discharge	Human body model	All pins	±4 kV
	uischarge	Charged-device model <sup>(4)</sup>	All pins charge	±1 kV
	Continuous total po	wer dissipation		See Dissipation Rating Table
	Electrical Fast Tran	isient/Burst <sup>(5)</sup>	A, B, and GND	±4 kV
TJ	Junction temperatu	re		170°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749-26.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.
- (5) Tested in accordance with IEC 61000-4-4.

## PACKAGE DISSIPATION RATINGS

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D <sup>(2)</sup>	597 mW	4.97 mW/°C	373 mW	298 mW	100 mW
D <sup>(3)</sup>	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW
Р	1290 mW	10.75 mW/°C	806 mW	645 mW	215 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7.

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#### **RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3		3.6	
$V_{I}$ or $V_{IC}$	Voltage at any bus terminal (separately o	r common mode)	-7 <sup>(1)</sup>		12	
V <sub>IH</sub>	High-level input voltage	D, DE, RE	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	D, DE, RE	0		0.8	
V <sub>ID</sub>	Differential input voltage	Figure 7	-12		12	
	I Path Jacob and an enter of	Driver	-60			
IOH	DH High-level output current	Receiver	-8			mA
	Level and a dead assumed	Driver			60	
I <sub>OL</sub>	Low-level output current	Receiver			8	mA
RL	Differential load resistance		54	60		Ω
CL	Differential load capacitance			50		pF
		HVD10			32	
	Signaling rate	HVD11			10	Mbps
		HVD12			1	
T <sub>J</sub> <sup>(2)</sup>	Junction temperature				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) See thermal characteristics table for information regarding this specification.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

	PARAMETER		TES	T CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage		I <sub>I</sub> = -18 mA		-1.5			V
			I <sub>O</sub> = 0		2		V <sub>CC</sub>	
V <sub>OD</sub>	Differential output voltage <sup>(2)</sup>		$R_L = 54 \Omega$ , See	$R_{\rm L} = 54 \ \Omega$ , See Figure 1				V
			$V_{\text{test}} = -7 \text{ V to } 1$	2 V, See Figure 2	1.5			
Δ V <sub>OD</sub>	Change in magnitude of differential voltage	output	See Figure 1 an	d Figure 2	-0.2		0.2	V
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output	t voltage				400		mV
V <sub>OC(SS)</sub>	Steady-state common-mode output	voltage	See Figure 3		1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-movel voltage	ode output			-0.0 5		0.05	V
OZ	High-impedance output current		See receiver inp	out currents				
1	Innut ourront	D			-100		0	۸
I	Input current	DE			0		100	μA
os	Short-circuit output current		$-7 \text{ V} \leq \text{V}_0 \leq 12$	V	-250		250	mA
C <sub>(OD)</sub>	Differential output capacitance		V <sub>OD</sub> = 0.4 sin (4	E6πt) + 0.5 V, DE at 0 V		16		pF
			RE at V <sub>CC</sub> , D & DE at V <sub>CC,</sub> No load	Receiver disabled and driver enabled		9	15.5	mA
I <sub>CC</sub>	Supply current		$\begin{tabular}{l} \hline \hline RE & at V_{CC}, \\ D & at V_{CC}, \\ DE & at 0 V, \\ No & load \end{tabular}$	Receiver disabled and driver disabled (standby)		1	5	μA
			RE at 0 V, D & DE at V <sub>CC</sub> , No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) For  $T_A > 85^{\circ}C$ ,  $V_{CC}$  is ±5%.

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#### DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

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	PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
		HVD10		5	8.5	16		
PLH	Propagation delay time, low-to-high-level output	HVD11		18	25	40	ns	
		HVD12		135	200	300		
		HVD10		5	8.5	16		
PHL	Propagation delay time, high-to-low-level output	HVD11		18	25	40	ns	
		HVD12		135	200	300		
		HVD10		3	4.5	10		
r	Differential output signal rise time	HVD11	$R_L = 54 \Omega, C_L = 50 pF,$ See Figure 4	10	20	30	ns	
		HVD12		100	170	300		
		HVD10		3	4.5	10		
ŀf	Differential output signal fall time	HVD11		10	20	30	ns	
		HVD12	-	100	170	300		
		HVD10	-			1.5		
sk(p)	Pulse skew ( t <sub>PHL</sub> – t <sub>PLH</sub>  )	HVD11				2.5	ns	
- 47	HVD12		-			7		
		HVD10				6		
sk(pp) <sup>(2)</sup>	Part-to-part skew	HVD11			ns			
- 417		HVD12	-	100				
		HVD10				31		
PZH	Propagation delay time,		-			55	ns	
	high-impedance-to-high-level output	HVD12	$R_{L} = 110 \Omega$ , $\overline{RE}$ at 0 V,	300 25 55			ns	
		HVD10	See Figure 5					
PHZ	Propagation delay time, high-level-to-high-impedance output	HVD11	-					
	high-level-to-high-impedance output	HVD12	-	300				
		HVD10				26		
PZL	Propagation delay time,	HVD11	-			55	ns	
	high-impedance-to-low-level output	HVD12	$R_{I} = 110 \Omega, \overline{RE} \text{ at } 0 \text{ V},$			300		
	Propagation delay time, Z low-level-to-high-impedance output		See Figure 6			26		
PLZ						75	ns	
				400				
PZH	Propagation delay time, standby-to-high-level outp	HVD12	$R_L = 110 \Omega$ , $\overline{RE}$ at 3 V, See Figure 5			6	μs	
PZL	Propagation delay time, standby-to-low-level output	ut	$R_L = 110 \Omega$ , $\overline{RE}$ at 3 V, See Figure 6			6	μs	

All typical values are at 25°C and with a 3.3-V supply.
t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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#### **RECEIVER ELECTRICAL CHARACTERISTICS**

over recommended operating conditions unless otherwise noted

	PARAMETER	Т	EST CONDITIO	NS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	I <sub>O</sub> = -8 mA					-0.01	
V <sub>IT-</sub>	Negative-going input threshold voltage	I <sub>O</sub> = 8 mA			-0.2			V
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )					35		mV
V <sub>IK</sub>	Enable-input clamp voltage	I <sub>I</sub> = -18 mA			-1.5			V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV,	I <sub>OH</sub> = -8 mA,	See Figure 7	2.4			V
V <sub>OL</sub>	Low-level output voltage	$V_{ID} = -200 \text{ mV},$	$I_{OL} = 8 \text{ mA},$	See Figure 7			0.4	V
I <sub>OZ</sub>	High-impedance-state output current	$V_{O} = 0 \text{ or } V_{CC}$	$\overline{\text{RE}}$ at V <sub>CC</sub>		-1		1	μA
		$V_A \text{ or } V_B = 12 \text{ V}$				0.05	0.11	
		$V_A \text{ or } V_B = 12 \text{ V},$	$V_{CC} = 0 V$	HVD11, HVD12,		0.06	0.13	mA
		$V_A$ or $V_B = -7 V$		Other input at 0 V	-0.1	-0.05		ШA
	Pue input ourrent	$V_A$ or $V_B = -7 V$ ,	$V_{CC} = 0 V$		-0.05	-0.04		
II.	Bus input current	$V_A \text{ or } V_B = 12 \text{ V}$				0.2	0.5	
		$V_A \text{ or } V_B = 12 \text{ V},$	$V_{CC} = 0 V$	HVD10,		0.25	0.5	
		$V_A$ or $V_B = -7 V$		Other input at 0 V	-0.4	-0.2		mA
		$V_A$ or $V_B = -7 V$ ,	$V_{CC} = 0 V$		-0.4	-0.15		
I <sub>IH</sub>	High-level input current, RE	V <sub>IH</sub> = 2 V			-30		0	μA
IIL	Low-level input current, RE	V <sub>IL</sub> = 0.8 V			-30		0	μA
C <sub>ID</sub>	Differential input capacitance	V <sub>ID</sub> = 0.4 sin (4E6	πt) + 0.5 V, DE a	at 0 V		15		pF
		RE at 0 V, D & DE at 0 V, No load	Receiver enabl disabled	led and driver		4	8	mA
I <sub>CC</sub>	Supply current	$\label{eq:relation} \begin{array}{ c c } \hline RE & at V_{CC}, \\ D & at V_{CC}, \\ DE & at 0 \ V, \\ No \ load \end{array}$	Receiver disab disabled (stand			1	5	μA
		RE at 0 V, D & DE at V <sub>CC</sub> , No load	Receiver enabl enabled	led and driver		9	15.5	mA

(1) All typical values are at  $25^{\circ}$ C and with a 3.3-V supply.

#### **RECEIVER SWITCHING CHARACTERISTICS**

over recommended operating conditions unless otherwise noted

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	PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	HVD10		12.5	20	25		
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	HVD10		12.5	20	25	ns	
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	HVD11 HVD12	V <sub>ID</sub> = −1.5 V to 1.5 V,	30	55	70	ns	
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	HVD11 HVD12	$C_L = 15 \text{ pF},$ See Figure 8	30	55	70	ns	
		HVD10				1.5		
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> – t <sub>PLH</sub>  )	HVD11				4	ns	
						4		
		HVD10				8		
t <sub>sk(pp)</sub> <sup>(2)</sup>	Part-to-part skew	HVD11				15	ns	
		HVD12				15		
t <sub>r</sub>	Output signal rise time		C <sub>L</sub> = 15 pF,	1	2	5	~~	
t <sub>f</sub>	Output signal fall time		See Figure 8	1	2	5	ns	
t <sub>PZH</sub> <sup>(1)</sup>	Output enable time to high level					15		
t <sub>PZL</sub> <sup>(1)</sup>	) Output enable time to low level		C <sub>L</sub> = 15 pF, DE at 3 V,			15		
t <sub>PHZ</sub>	Output disable time from high level		See Figure 9			20	ns	
t <sub>PLZ</sub>	Output disable time from low level					15		
t <sub>PZH</sub> <sup>(2)</sup>	Propagation delay time, standby-to-high-level output		C <sub>L</sub> = 15 pF, DE at 0,			6		
t <sub>PZL</sub> <sup>(2)</sup>	Propagation delay time, standby-to-low-level outp	ut	See Figure 10			6	μs	

(1) All typical values are at 25°C and with a 3.3-V supply

(2) t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

#### THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted <sup>(1)</sup>

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0	Junction-to-ambient thermal	High-K board <sup>(3)</sup> , No airflow	D pkg		121		
$\theta_{JA}$	resistance <sup>(2)</sup>	No airflow <sup>(4)</sup>	P pkg		93		
0	Junction-to-board thermal	High-K board	D pkg		67		0000
$\theta_{JB}$	resistance	See <sup>(4)</sup>	P pkg		57		°C/W
0	Junction-to-case thermal		D pkg		41		
$\theta_{\text{JC}}$	resistance		P pkg		55		
		$R_{l} = 60 \Omega, C_{l} = 50 pF,$	HVD10 (32 Mbps)		198	250	
P <sub>D</sub>	Device power dissipation	DE at V <sub>CC</sub> , RE at 0 V, Input to D a 50% duty cycle square	HVD11 (10 Mbps)		141	176	mW
		wave at indicated signaling rate	HVD12 (500 kbps)		133	161	
-		High-K board, No airflow	D pkg	-40		116	
T <sub>A</sub>	Ambient air temperature	No airflow <sup>(4)</sup>	P pkg	-40		123	°C
T <sub>JSD</sub>	Thermal shutdown junction temp	perature			165		

(1) See Application Information section for an explanation of these parameters.

(2) The intent of  $\theta_{JA}$  specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

(3) JSD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

(4) JESD51-10, Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.

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## SN65HVD10, SN65HVD10Q, SN75HVD10 SN65HVD11, SN65HVD11Q, SN75HVD11 SN65HVD12, SN75HVD12

 $\textbf{375} \ \Omega \pm \textbf{1\%}$ 

 $\Lambda \Lambda \Lambda$ 

 $\langle \Lambda \Lambda \rangle$ 

Figure 2. Driver V<sub>OD</sub> With Common-Mode Loading Test

Circuit

VOC(PP)

 $\textbf{375}~\Omega \pm \textbf{1\%}$ 

**60**  $\Omega \pm 1\%$ 

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< V<sub>(test)</sub> < 12 V

 $V_{\mathsf{A}}$ 

٧<sub>B</sub>

∆V<sub>OC(SS)</sub>

– 3 V

2 V

-2 V

1.5 V

0 V

10%

#### PARAMETER MEASUREMENT INFORMATION

Vcc

DF

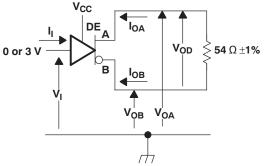
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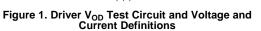
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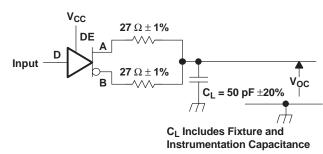
Voc

В

VOD

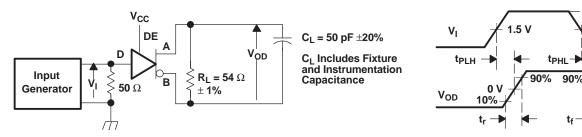






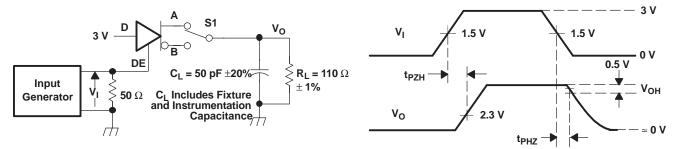
Input: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6ns,  $t_f$ <6ns,  $Z_O$  = 50  $\Omega$ 

# Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t<sub>r</sub> <6 ns, t<sub>f</sub> <6 ns, Z<sub>o</sub> = 50  $\Omega$ 





Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r$  <6 ns,  $t_f$  <6 ns,  $Z_o$  = 50  $\Omega$ 

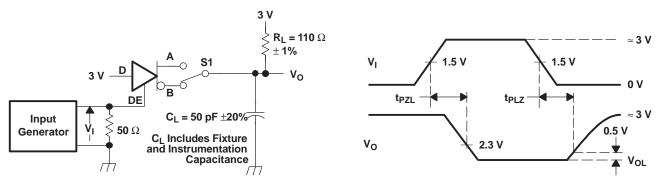
#### Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

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#### PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t<sub>r</sub> <6 ns, t<sub>f</sub> <6 ns, Z<sub>o</sub> = 50  $\Omega$ 

#### Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

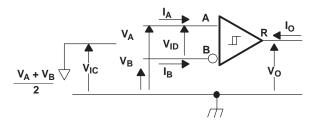
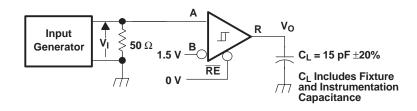


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t\_r <6 ns, t\_f <6 ns, Z\_o = 50  $\Omega$ 

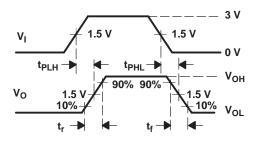


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms

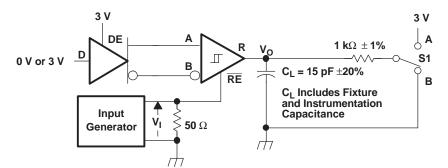
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#### PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_{\rm f}$  <6 ns,  $t_{\rm f}$  <6 ns,  $Z_{\rm o}$  = 50  $\Omega$ 

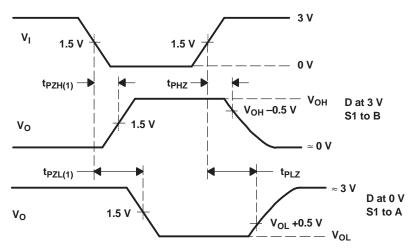
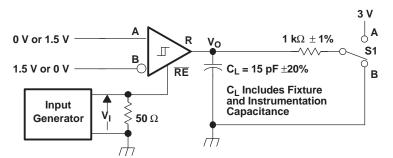


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled



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#### PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 100 kHz, 50% Duty Cycle, t<sub>r</sub> <6 ns, t<sub>f</sub> <6 ns, Z<sub>o</sub> = 50  $\Omega$ 

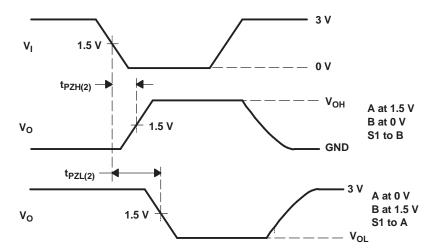
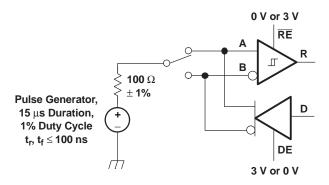


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



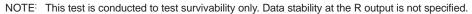


Figure 11. Test Circuit, Transient Over Voltage Test

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#### PARAMETER MEASUREMENT INFORMATION (continued)

#### **FUNCTION TABLES**

#### DRIVER<sup>(1)</sup>

		OUT	PUTS
INPUT D	ENABLE DE	Α	В
Н	Н	Н	L
L	Н	L	Н
Х	L	Z	Z
Open	Н	Н	L

(1) H = high level L = low level Z = high impedance

X = irrelevant

? = indeterminate

#### **RECEIVER**<sup>(1)</sup>

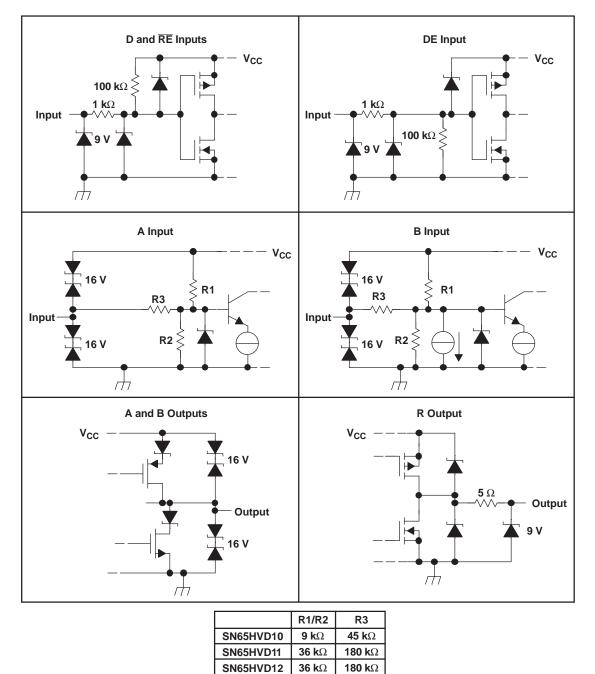
DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE RE	OUTPUT R
$V_{ID} \leq -0.2 V$	L	L
$-0.2 \text{ V} < \text{V}_{\text{ID}} < -0.01 \text{ V}$	L	?
−0.01 V ≤ V <sub>ID</sub>	L	Н
Х	Н	Z
Open Circuit	L	Н
Short circuit	L	Н

(1) H = high levelL = low level

Z = high impedance X = irrelevant

? = indeterminate

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## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



INSTRUMENTS

Texas

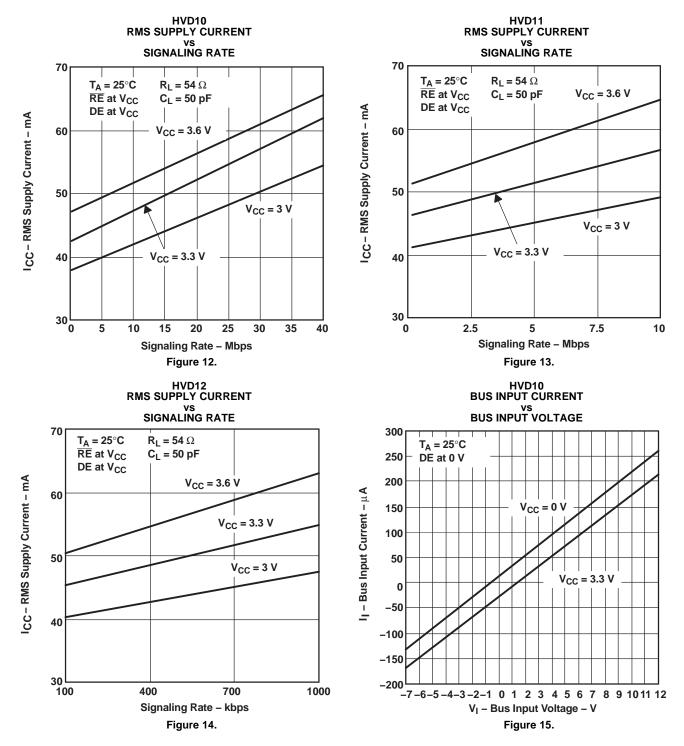
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## SN65HVD10, SN65HVD10Q, SN75HVD10 SN65HVD11, SN65HVD11Q, SN75HVD11 SN65HVD12, SN75HVD12

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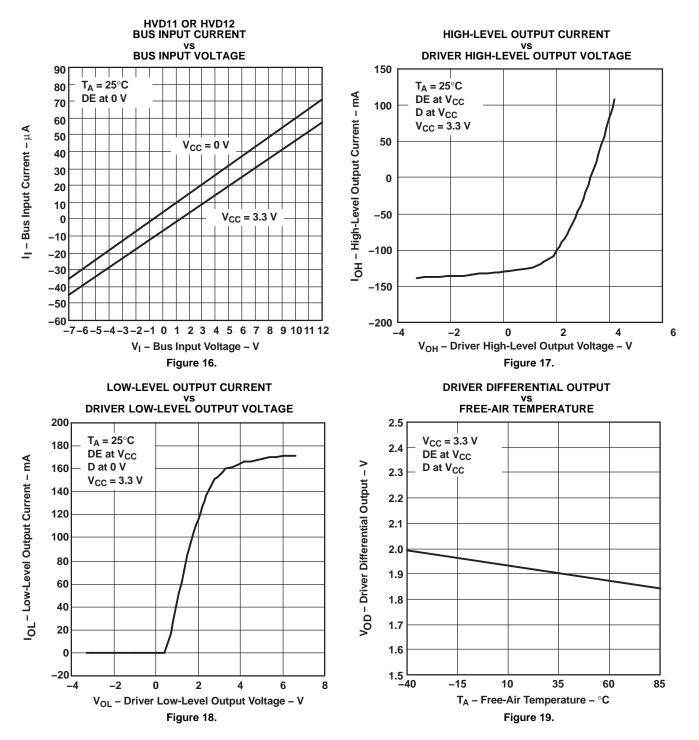
#### **TYPICAL CHARACTERISTICS**



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#### **TYPICAL CHARACTERISTICS (continued)**

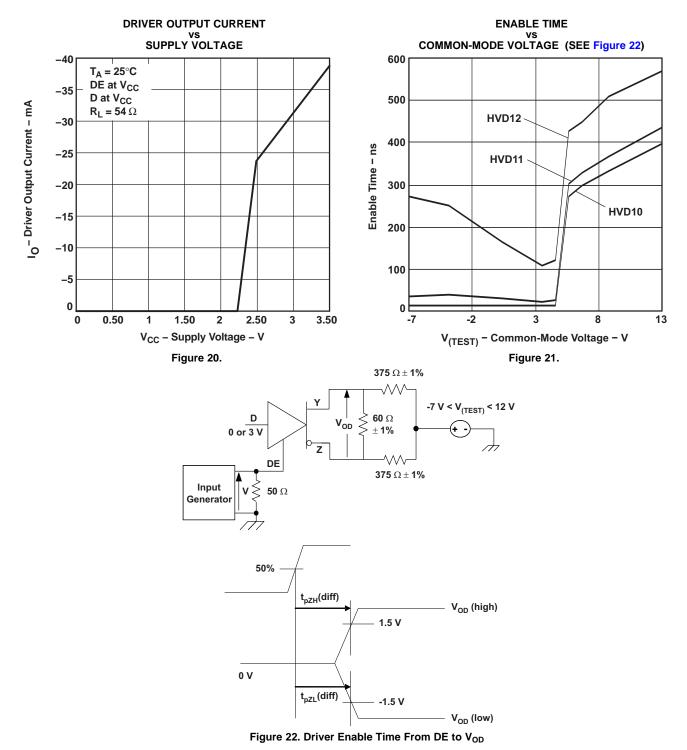
14



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#### **TYPICAL CHARACTERISTICS (continued)**



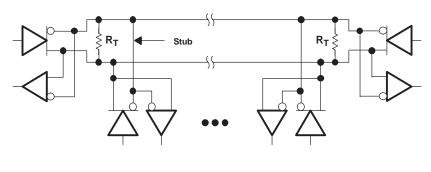
The time  $t_{pZL}(x)$  is the measure from DE to  $V_{OD}(x)$ .  $V_{OD}$  is valid when it is greater than 1.5 V.

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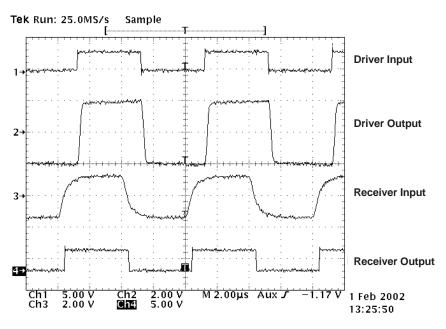
www.ti.com

#### **APPLICATION INFORMATION**



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance ( $R_T = Z_O$ ). Stub lengths off the main line should be kept as short as possible.



#### Figure 23. Typical Application Circuit

Figure 24. HVD12 Input and Output Through 2000 Feet of Cable

An example application for the HVD12 is illustrated in Figure 23. Two HVD12 transceivers are used to communicate data through a 2000 foot (600 m)

length of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a  $100-\Omega$  resistor, matching the cable characteristic impedance. Figure 24 illustrates operation at a signaling rate of 250 kbps.

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# THERMAL CHARACTERISTICS OF IC PACKAGES

 $\theta_{JA}$  (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

 $\theta_{JA}$  is *not* a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

 $\theta_{JA}$  can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures.  $\theta_{JA}$  is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in  $\theta_{JA}$  can be measured between these two test cards.

 $\theta_{JC}$  (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

 $\theta_{JC}$  is a useful thermal characteristic when a heatsink is applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with  $\theta_{JB}$  in 1-dimensional thermal simulation of a package system.

 $\theta_{JB}$  (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure.  $\theta_{JB}$  is only defined for the high-k test card.

 $\theta_{JB}$  provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see Figure 25.

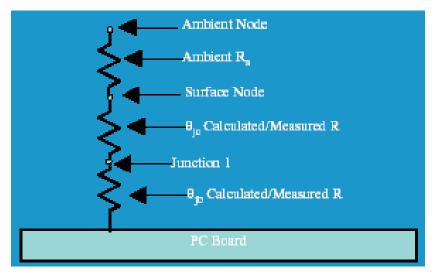


Figure 25. Thermal Resistance

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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65HVD10D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD10PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD10QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD10QP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD10QPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD11PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD11QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD11QDRG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI
SN65HVD11QP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD11QPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD12D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

# PACKAGE OPTION ADDENDUM

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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65HVD12DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD12DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD12DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD12P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD12PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD10D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD10DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD10DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD10DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD10P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD10PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD11DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD11DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD11P	ACTIVE	PDIP	Р	8		TBD	Call TI	Call TI
SN75HVD11PE4	ACTIVE	PDIP	Р	8		TBD	Call TI	Call TI
SN75HVD12D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD12DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD12DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD12DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75HVD12P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75HVD12PE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs. **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN65HVD10, SN65HVD12 :

• Enhanced Product: SN65HVD10-EP, SN65HVD12-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

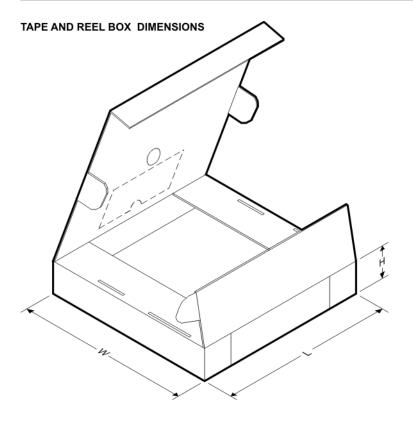


*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD10DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD10QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD12DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD10DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD12DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



# PACKAGE MATERIALS INFORMATION

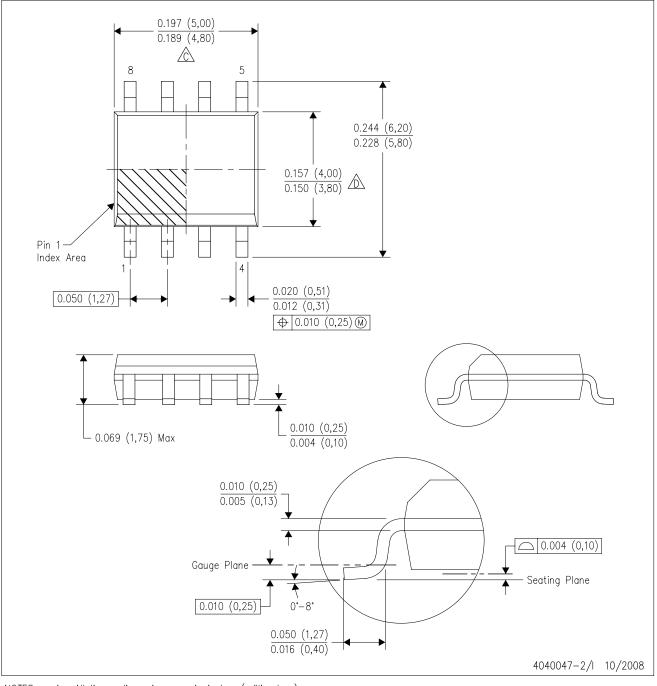
12-Feb-2009



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD10DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD10QDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD11DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD11QDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD12DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD10DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD11DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD12DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.



## **MECHANICAL DATA**

MPDI001A - JANUARY 1995 - REVISED JUNE 1999



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg\_info.htm



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DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

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