# CAN Transceiver with Fast Loop Times for Highly Loaded Networks

**Check for Samples: SN65HVD255, SN65HVD256**

## FEATURES

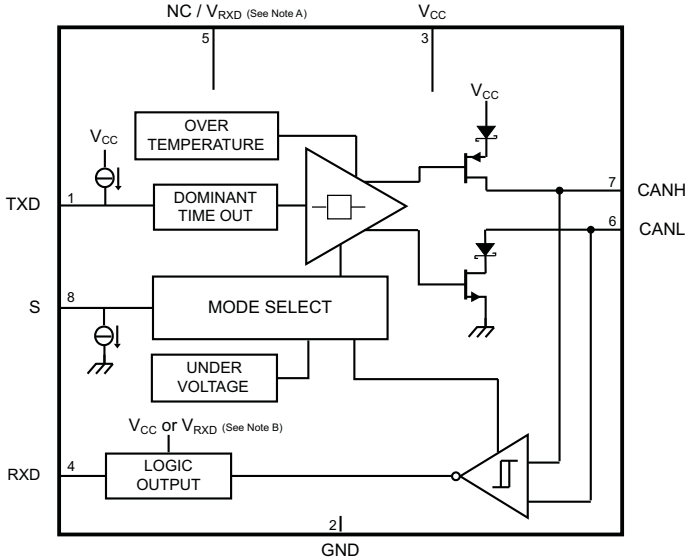
- **Meets the Requirements of ISO11898-2**
- **"Turbo CAN":**
  - **Short Propagation Delay Times and Fast Loop Times**
  - **Higher Data Rates in Network**
  - **Enhances System Timing Margins**
- **I/O Voltage Range Supports 3.3V and 5V MCUs**
- **Ideal Passive Behavior When Unpowered**
  - **Bus Pins are High Impedance (no load to operating bus)**
  - **Logic Pins are High Impedance**
  - **Power Up/Down With Glitch Free Operation On Bus**
- **Protection Features:**
  - **ESD Protection of Bus Pins**
    - **HBM ESD Protection Exceeds ±12 kV**
  - **Bus Fault Protection –27V to 40V**
  - **Under Voltage Protection on Supply Pins**
  - **TXD (Driver) Dominant Time Out (DTO)**
  - **Thermal Shutdown Protection**
- **Characterized for –40°C to 125°C Operation**

## APPLICATIONS

- **1Mbps Operation in Highly Loaded CAN Networks Down to 10kbps Networks With TXD DTO**
- **Industrial Automation, Control, Sensors and Drive Systems**
- **Building and Climate Control Automation**
- **Security Systems**
- **Telecom Base Station Status and Control**
- **CAN Bus Standards Such as CANopen, CAN Kingdom, DeviceNet, NMEA2000**

## DESCRIPTION

This CAN transceiver meets the ISO1189-2 High Speed CAN (Controller Area Network) Physical Layer standard. It is designed for data rates in excess of 1 megabit per second (Mbps) in short networks and enhanced timing margin and higher data rates in long and highly loaded networks. The device includes many protection features providing device and CAN network robustness.



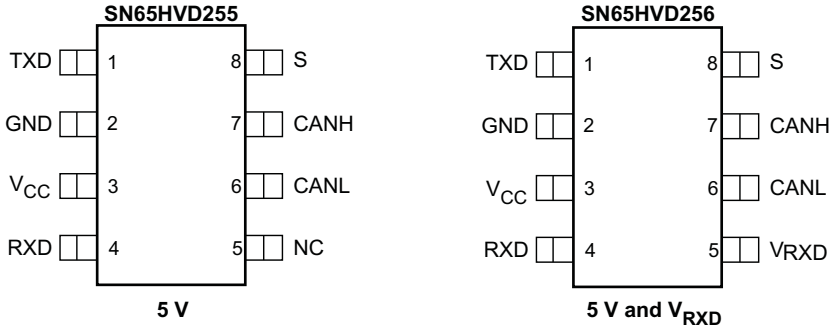

A. Pin 5 use is device dependent. NC for 5V-only devices and $V_{RXD}$ for RXD output level-shifting devices.

B. RXD logic output is driven to 5V $V_{CC}$ on 5V-only devices and driven to $V_{RXD}$ on output level-shifting devices.

**Figure 1. Functional Block Diagram**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## D PACKAGE (TOP VIEW)




## DEVICE OPTIONS

| PART NUMBER | I/O SUPPLY for RXD | COMMENT |
|---|---|---|
| SN65HVD255 | No | `251 and `1050 functional upgrade with “Turbo” CAN fast loop times and TXD DTO protection allowing data rates down to 10kbps |
| SN65HVD256 | Yes | `251 and `1050 functional upgrade with “Turbo” CAN fast loop times and TXD DTO protection allowing data rates down to 10kbps. RXD output level shifting via RXD supply input. |

## PIN FUNCTIONS

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| TXD | 1 | I | CAN transmit data input (LOW for dominant and HIGH for recessive bus states) |
| GND | 2 | GND | Ground connection |
| $V_{CC}$ | 3 | Supply | Transceiver 5V supply voltage |
| RXD | 4 | O | CAN receive data output (LOW for dominant and HIGH for recessive bus states) |
| NC | 5 | NC | SN65HVD255: No Connect |
| $V_{RXD}$ | | Supply | SN65HVD256: RXD output supply voltage |
| CANL | 6 | I/O | Low level CAN bus line |
| CANH | 7 | I/O | High level CAN bus line |
| S | 8 | I | Mode select: S (Silent Mode) select pin (active high) |

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | ORDERABLE PART NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| –40°C to 125°C | SOIC – D | SN65HVD255D and SN65HVD255DR | HVD255 |
| | | SN65HVD256D and SN65HVD256DR | HVD256 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

# FUNCTIONAL DESCRIPTION

## OPERATING MODES

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made via the S input pin.

**Table 1. Operating Modes**

| S Pin | MODE | DRIVER | RECEIVER | RXD Pin |
|---|---|---|---|---|
| LOW | Normal Mode | Enabled (ON) | Enabled (ON) | Mirrors Bus State(1) |
| HIGH | Silent Mode | Disabled (OFF) | Enabled (ON) | Mirrors Bus State |

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

## CAN BUS STATES

The CAN bus has two states during powered operation of the device: dominant and recessive. Dominant bus state is when the bus is driven differentially. Dominant bus state corresponds to logic low on the TXD and RXD pins. Recessive bus states is when the bus is biased to $V_{CC}/2$ via the high-ohmic internal input resistors $R_{IN}$ of the receiver. Recessive bus state corresponds to logic high on the TXD and RXD pins. See Figure 2 and Figure 3.

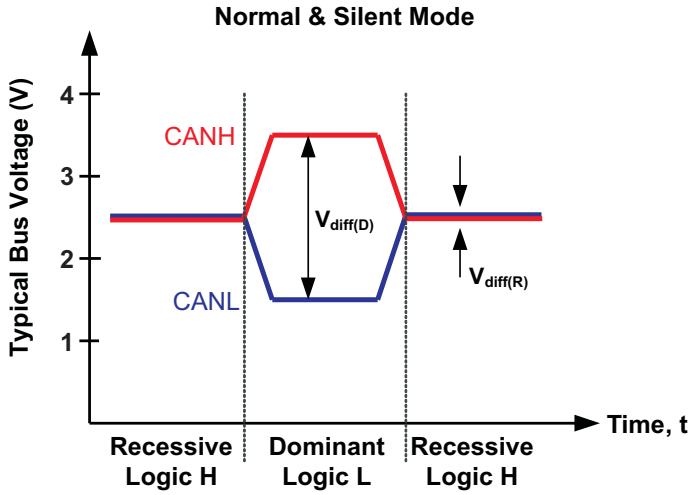



**Figure 2. Bus States (Physical Bit Representation)**

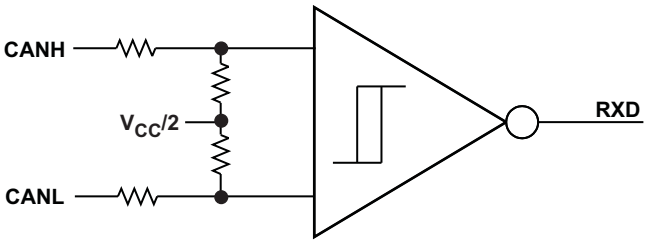



**Figure 3. Simplified Recessive Common Mode Bias and Receiver**

## NORMAL MODE

This is the normal operating mode of the device, selected by setting S low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

## SILENT MODE

This is the silent (receive only) mode of the device, selected by setting S high. The CAN driver is turned off while the receiver remains active and RXD will output the received bus state.

**APPLICATION NOTE:** Silent mode may be used to implement *babbling idiot* protection, to ensure that the driver does not disrupt the network in case of a local fault. Silent mode may also be used in redundant systems to select or de-select the redundant transceiver (driver) when needed.

## DRIVER AND RECEIVER FUNCTION TABLES

**Table 2. Driver Function Table**

| DEVICE | INPUTS | | OUTPUTS | | DRIVEN BUS STATE |
|---|---|---|---|---|---|
| | S(1)(2) | TXD(1)(3) | CANH(1) | CANL(1) | |
| All Devices | L or Open | L | H | L | Dominant |
| | | H or Open | Z | Z | Recessive |
| | H | X | Z | Z | Recessive |

(1) H = high level, L = low level, X= irrelevant, Z = common mode (recessive) bias to $V_{CC}$ / 2. See Figure 2 and Figure 3 for bus state and common mode bias information.
(2) Devices have an internal pull down to GND on S pin. If S pin is open the pin will be pulled low and the device will be in normal mode.
(3) Devices have an internal pull up to $V_{CC}$ on TXD pin. If the TXD pin is open the pin will be pulled high and the transmitter will remain in recessive (non-driven) state.

**Table 3. Receiver Function Table**

| DEVICE MODE | CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$ | BUS STATE | RXD PIN(1) |
|---|---|---|---|
| Normal or Silent | $V_{ID} \geq 0.9$ V | Dominant | L |
| | 0.5 V < $V_{ID}$ < 0.9 V | ? | ? |
| | $V_{ID} \leq 0.5$ V | Recessive | H |
| | Open ($V_{ID} \approx 0$ V) | Open | H |

(1) H = high level, L = low level, ? = indeterminate.

## DIGITAL INPUTS AND OUTPUTS

### 5V $V_{CC}$ Only Device (SN65HVD255):

The 5V $V_{CC}$ device is supplied by a single 5V rail and has digital inputs that are 5V and 3.3V compatible. This device has a 5V ($V_{CC}$) level RXD output. TXD is internally pulled up to $V_{CC}$ and S is internally pulled down to GND.

**APPLICATION NOTE:** While the TXD is internally pulled up to $V_{CC}$ and S pin is internally pulled down to GND care should be take that the strength of the internal biasing is strong enough in application situations. The internal bias is there to put the device in a known state if the pin floats and not to provide system level biasing. Special consideration should be taken on pull up strength and timing if the TXD output pin on the microprocessor's CAN controller is open drain.

### 5V $V_{CC}$ with $V_{RXD}$ RXD output Supply Devices (SN65HVD256):

This device is a 5V $V_{CC}$ CAN transceiver with a separate supply for the RXD output, $V_{RXD}$. The digital inputs are 5V and 3.3V compatible. These devices have a $V_{RXD}$ level RXD output. TXD remains weakly pulled up to $V_{CC}$.

**APPLICATION NOTE:** On device versions with $V_{RXD}$ supply which shifts the RXD output level the input pins of the device remain the same. TXD remains weakly pulled up to $V_{CC}$ internally and thus a small $I_{IH}$ current will flow if TXD input is used below $V_{CC}$ levels.

## PROTECTION FEATURES

### TXD DOMINANT TIME OUT (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD dominant time out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period $t_{TXD\_DTO}$. The dominant time out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out period of the circuit expires, the CAN bus driver is disabled. This keeps the bus free for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the TXD dominant time out. The receiver and RXD pin will still reflect the CAN bus and the bus pins will be biased to recessive level during a TXD dominant time out.

**APPLICATION NOTE:** The minimum dominant TXD time allowed by the TXD dominant time out limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{TXD\_DTO}$ minimum, limits the minimum data rate. The minimum transmitted data rate may be calculated by: Minimum Data Rate = 11/ $t_{TXD\_DTO}$.

### THERMAL SHUTDOWN

If the junction temperature of the device exceeds the thermal shut down threshold the device will turn off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared once the junction temperature drops below the thermal shutdown temperature of the device.

**APPLICATION NOTE:** During thermal shutdown the CAN bus drivers will be turned off thus no transmission is possible from TXD to the bus. The CAN bus pins will be biased to recessive level during a thermal shutdown and the receiver to RXD path will remain operational.

### UNDER VOLTAGE LOCKOUT

The supply pins have undervoltage detection which place the device in protected mode. This protects the bus during an undervoltage event on either the $V_{CC}$ or $V_{RXD}$ supply pins.

**Table 4. Undervoltage Lockout 5V Only Device**

| $V_{CC}$ | DEVICE STATE | BUS OUTPUT | RXD |
|---|---|---|---|
| GOOD | Normal | Per Device State and TXD | Mirrors Bus |
| BAD | Protected | High Impedance | High Impedance (3-state) |

**Table 5. Undervoltage Lockout 5V and $V_{RXD}$ Device**

| $V_{CC}$ | $V_{RXD}$ | DEVICE STATE | BUS OUTPUT | RXD |
|---|---|---|---|---|
| GOOD | GOOD | Normal | Per Device State and TXD | Mirrors Bus |
| BAD | GOOD | Protected | High Impedance | High (Recessive) |
| GOOD | BAD | Protected | Recessive | High Impedance (3-state) |
| BAD | BAD | Protected | High Impedance | High Impedance (3-state) |

**APPLICATION NOTE:** Once an undervoltage condition is cleared and the supplies have returned to valid levels the device will typically need 300 µs to transition to normal operation.

### UNPOWERED DEVICE

The device is designed to be an "ideal passive" or “no load” to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered so they will not load down the bus. This is critical if some nodes of the network will be unpowered while the rest of the of network remains in operation. Logic pins will also have extremely low leakage currents when the device is unpowered so they will not load down other circuits which may remain powered.

## FLOATING PINS

The device has internal pull ups and pull downs on critical pins to place the device into known states if the pins float. The TXD pin is pulled up to $V_{CC}$ to force a recessive input level if the pin floats. The S pin is pulled down to GND to force the device into normal mode if the pin floats.

## CAN BUS SHORT CIRCUIT CURRENT LIMITING

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant state time out which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant time out which prevents permanently driving dominant and CAN protocol has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

**APPLICATION NOTE:** The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$I_{OS(AVG)}$ = %Transmit × [(%REC_Bits × $I_{OS(SS)\_REC}$) + (%DOM_Bits × $I_{OS(SS)\_DOM}$)] + [%Receive × $I_{OS(SS)\_REC}$]

Where $I_{OS(AVG)}$ is the average short circuit current, %Transmit is the percentage the node is transmitting CAN messages, %Receive is the percentage the node is receiving CAN messages, %REC_Bits is the percentage of recessive bits in the transmitted CAN messages, %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages, $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current and $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current.

**APPLICATION NOTE:** The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components

## ABSOLUTE MAXIMUM RATINGS(1)(2)

| 1.0 | | | | RATING | UNIT |
|---|---|---|---|---|---|
| 1.1 | $V_{CC}$ | Supply voltage range | | –0.3 to 6 | V |
| 1.2 | $V_{RXD}$ | RXD Output supply voltage range | (SN65HVD256 only) | –0.3 to 6 and $V_{RXD} \le V_{CC} + 0.3$ | V |
| 1.3 | $V_{BUS}$ | CAN Bus I/O voltage range (CANH, CANL) | | –27 to 40 | V |
| 1.4 | $V_{Logic\_Input}$ | Logic input pin voltage range (TXD, S) | | –0.3 to 6 | V |
| 1.5 | $V_{Logic\_Output}$ | Logic output pin voltage range (RXD) | SN65HVD255 | –0.3 to 6 | V |
| 1.6 | $V_{Logic\_Output}$ | Logic output pin voltage range (RXD) | SN65HVD256 | –0.3 to 6 and $V_I \le V_{RXD} + 0.3$ | V |
| 1.7 | $I_{O(RXD)}$ | RXD (Receiver) output current | | 12 | mA |
| 1.8 | $T_J$ | Operating virtual junction temperature range | | –40 to 150 | °C |
| 1.9 | $T_A$ | Ambient temperature range | | –40 to 125 | °C |
| 1.10 | $T_{LEAD}$ | Lead temperature (soldering, 10sec) | | 260 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

## TRANSIENT AND ELECTROSTATIC DISCHARGE PROTECTION

| 2.0 | | TEST CONDITIONS | | RATING | UNIT |
|---|---|---|---|---|---|
| 2.1 | Human-Body Model | All pins(1) | | ±2.5 | kV |
| | | CAN bus pins (CANH, CANL)(2) | | ±12 | |
| 2.2 | Charged-Device Model | All pins(3) | | ±750 | V |
| 2.3 | Machine Model | All pins(4) | | ±250 | V |
| 2.4 | IEC 61400-4-2 according to GIFT-ICT CAN EMC test spec(5) | CAN bus pins (CANH, CANL) to GND | | ±8 | kV |
| 2.5 | ISO7637 Transients according to GIFT - ICT CAN EMC test spec(6) | CAN bus pins (CANH, CANL) | Pulse 1 | –100 | V |
| 2.6 | | | Pulse 2 | +75 | V |
| 2.7 | | | Pulse 3a | –150 | V |
| 2.8 | | | Pulse 3b | +100 | V |

(1) Tested in accordance to JEDEC Standard 22, Test Method A114.
(2) Test method based upon JEDEC Standard 22 Test Method A114, CAN bus pins stressed with respect to GND.
(3) Tested in accordance to JEDEC Standard 22, Test Method C101.
(4) Tested in accordance to JEDEC Standard 22, Test Method A115.
(5) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.
(6) ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

## RECOMMENDED OPERATING CONDITIONS

| 3.0 | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 3.1 | $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| 3.2 | $V_{RXD}$ | RXD supply (SN65HVD256 only) | 2.8 | 5.5 | V |
| 3.3 | $V_I$ or $V_{IC}$ | CAN bus terminal voltage (separately or common mode) | –2 | 7 | V |
| 3.4 | $V_{ID}$ | CAN bus differential voltage | -6 | 6 | V |
| 3.5 | $V_{IH}$ | Logic HIGH level input (TXD, S) | 2 | 5.5 | V |
| 3.6 | $V_{IL}$ | Logic LOW level input (TXD, S) | 0 | 0.8 | V |
| 3.7 | $I_{OH(DRVR)}$ | CAN BUS Driver High level output current | –70 | | mA |
| 3.8 | $I_{OL(DRVR)}$ | CAN BUS Driver Low level output current | | 70 | mA |
| 3.9 | $I_{OH(RXD)}$ | RXD pin HIGH level output current | –2 | | mA |
| 3.10 | $I_{OL(RXD)}$ | RXD pin LOW level output current | | 2 | mA |
| 3.11 | $T_A$ | Operational free-air temperature (see Thermal Characteristics table) | –40 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, $T_A$ = –40°C to 125°C (unless otherwise noted). SN65HVD256 device $V_{RXD}$ = $V_{CC}$.

| | PARAMETER | | | TEST CONDITIONS / COMMENT | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **4.0** | **SUPPLY CHARACTERISTICS** | | | | | | | |
| 4.1 | $I_{CC}$ | 5-V Supply current | Normal Mode (Driving Dominant) | See Figure 4, TXD = 0 V, $R_L$ = 50-Ω, $C_L$ = open, $R_{CM}$ = open, S = 0V | | 60 | 85 | mA |
| 4.2 | | | Normal Mode (Driving Dominant – bus fault) | See Figure 4, TXD = 0 V, S = 0V, CANH = -12V, RL = open, $C_L$ = open, $R_{CM}$ = open | | 130 | 180 | |
| 4.3 | | | Normal Mode (Driving Dominant) | See Figure 4, TXD = 0 V, $R_L$ = open (no load), $C_L$ = open, $R_{CM}$ = open, S = 0V | | 10 | 20 | |
| 4.4 | | | Normal Mode (Recessive) | See Figure 4, TXD = $V_{CC}$, $R_L$ = 50-Ω, $C_L$ = open, $R_{CM}$ = open, S = 0V | | 10 | 20 | |
| 4.5 | | | Silent Mode | See Figure 4, TXD = $V_{CC}$, $R_L$ = 50-Ω,$C_L$ = open, $R_{CM}$ = open, S = $V_{CC}$ | | 2.5 | 5 | |
| 4.6 | $I_{RXD}$ | RXD Supply current (SN65HVD256 only) | All modes | RXD Floating, TXD = 0V | | | 500 | µA |
| 4.7 | $UV_{VCC}$ | Undervoltage detection on $V_{CC}$ for protected mode | | | 3.5 | | 4.45 | V |
| 4.8 | $V_{HYS(UVVCC)}$ | Hysteresis voltage on $UV_{VCC}$ | | | | 200 | | mV |
| 4.9 | $UV_{RXD}$ | Undervoltage detection on $V_{RXD}$ for protected mode (SN65HVD256 only) | | | 1.3 | | 2.75 | V |
| 4.10 | $V_{HYS(UVRXD)}$ | Hysteresis voltage on $UV_{RXD}$ (SN65HVD256 only) | | | | 80 | | mV |
| **5.0** | **S PIN (MODE SELECT INPUT)** | | | | | | | |
| 5.1 | $V_{IH}$ | HIGH-level input voltage | | | 2 | | | V |
| 5.2 | $V_{IL}$ | LOW-level input voltage | | | | | 0.8 | V |
| 5.3 | $I_{IH}$ | HIGH-level input leakage current | | S = $V_{CC}$ = 5.5 V | 7 | | 100 | µA |
| 5.4 | $I_{IL}$ | Low-level input leakage current | | S = 0 V, $V_{CC}$ = 5.5 V | –1 | 0 | 1 | µA |
| 5.5 | $I_{LKG(OFF)}$ | Unpowered leakage current | | S = 5.5 V, $V_{CC}$ = 0 V, $V_{RXD}$ = 0 V | 7 | 35 | 100 | µA |
| **6.0** | **TXD PIN (CAN TRANSMIT DATA INPUT)** | | | | | | | |
| 6.1 | $V_{IH}$ | HIGH level input voltage | | | 2 | | | V |
| 6.2 | $V_{IL}$ | LOW level input voltage | | | | | 0.8 | V |
| 6.3 | $I_{IH}$ | HIGH level input leakage current | | TXD = $V_{CC}$ = 5.5 V | –2.5 | 0 | 1 | µA |
| 6.4 | $I_{IL}$ | Low level input leakage current | | TXD = 0 V, $V_{CC}$ = 5.5 V | –100 | -25 | –7 | µA |
| 6.5 | $I_{LKG(OFF)}$ | Unpowered leakage current | | TXD = 5.5 V, $V_{CC}$ = 0 V, $V_{RXD}$ = 0 V | –1 | 0 | 1 | µA |
| 6.6 | $C_I$ | Input Capacitance | | | | 3.5 | | pF |
| **7.0** | **RXD Pin (CAN RECEIVE DATA OUTPUT)** | | | | | | | |
| 7.1 | $V_{OH}$ | HIGH level output voltage | | See Figure 5, $I_O$ = –2mA. For devices with $V_{RXD}$ supply $V_{OH}$ = 0.8 × $V_{RXD}$ | 0.8×$V_{CC}$ | | | V |
| 7.2 | $V_{OL}$ | LOW level output voltage | | See Figure 5, $I_O$ = 2mA. | | | 0.4 | V |
| 7.3 | $I_{LKG(OFF)}$ | Unpowered leakage current | | RXD = 5.5 V, $V_{CC}$ = 0 V, $V_{RXD}$ = 0 V | –1 | 0 | 1 | µA |
| 7.4 | $t_R$ | Output signal rise time | | See Receiver Rise Time | | | | |
| 7.5 | $t_F$ | Output signal fall time | | See Receiver Fall Time | | | | |

(1) All typical values are at 25°C and supply voltages of $V_{CC}$ = 5 V and $V_{RXD}$ = 5 V, $R_L$ = 60Ω.

## ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, $T_A$ = –40°C to 125°C (unless otherwise noted). SN65HVD256 device $V_{RXD}$ = $V_{CC}$.

| | PARAMETER | | | TEST CONDITIONS / COMMENT | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **8.0** | **DEVICE SWITCHING CHARACTERISTICS** | | | | | | | |
| 8.1 | $t_{PROP(LOOP1)}$ | Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant | | See Figure 7, S = 0 V, $R_L$ = 60Ω, $C_L$ = 100pF, $C_{L\_RXD}$ = 15pF | | | 150 | ns |
| 8.2 | $t_{PROP(LOOP2)}$ | Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive | | | | | 150 | |
| 8.3 | $I_{MODE}$ | Mode change time, from Normal to Silent or from Silent to Normal | | See Figure 6 | | | 20 | µS |
| **9.0** | **DRIVER ELECTRICAL CHARACTERISTICS** | | | | | | | |
| 9.1 | $V_{O(D)}$ | Bus output voltage (dominant | CANH | See Figure 2 and Figure 4, TXD = 0 V, S = 0 V, $R_L$ = 60Ω, $C_L$ = open, $R_{CM}$ = open | 2.75 | | 4.5 | V |
| 9.2 | | | CANL | | 0.5 | | 2.25 | |
| 9.3 | $V_{O(R)}$ | Bus output voltage (recessive) | | See Figure 2 and Figure 4, TXD = $V_{CC}$, $V_{RXD}$ = $V_{CC}$, S = $V_{CC}$ or 0 V (2), $R_L$ = open (no load), $R_{CM}$ = open | 2 | 0.5×$V_{CC}$ | 3 | V |
| 9.4 | $V_{OD(D)}$ | Differential output voltage (dominant) | | See Figure 2 and Figure 4, TXD = 0 V, S = 0 V, 45Ω ≤ $R_L$ ≤ 65Ω, $C_L$ = open, $R_{CM}$ = 330Ω, –2 V ≤ $V_{CM}$ ≤ 7 V, 4.75 V≤ $V_{CC}$ ≤ 5.25 V | 1.5 | | 3 | V |
| 9.5 | | | | See Figure 2 and Figure 4, TXD = 0 V, S = 0 V, 45Ω ≤ $R_L$ ≤ 65Ω, $C_L$ = open, $R_{CM}$ = 330Ω, –2 V ≤ $V_{CM}$ ≤ 7 V, 4.5V ≤ $V_{CC}$ ≤ 5.5 V | 1.25 | | 3.2 | |
| 9.6 | $V_{OD(R)}$ | Differential output voltage (recessive) | | See Figure 2 and Figure 4, TXD = $V_{CC}$, S = 0 V, $R_L$ = 60Ω, $C_L$ = open, $R_{CM}$ = open | –0.12 | | 0.012 | V |
| 9.7 | | | | See Figure 2 and Figure 4, TXD = $V_{CC}$, S = 0 V, $R_L$ = open (no load), $C_L$ = open, $R_{CM}$ = open, –40°C ≤ $T_A$ ≤ 85°C | –0.100 | | 0.050 | |
| 9.8 | $V_{SYM}$ | Output symmetry (dominant or recessive) ($V_{CC}$ – $V_{O(CANH)}$ – $V_{O(CANL)}$) | | See Figure 2 and Figure 4, S at 0 V, $R_L$ = 60Ω, $C_L$ = open, $R_{CM}$ = open | –0.4 | | 0.4 | V |
| 9.9 | $I_{OS(SS)\_DOM}$ | Short-circuit steady-state output current, Dominant | | See Figure 2 and Figure 9, $V_{CANH}$ = 0 V, CANL = open, TXD = 0V | –160 | | | mA |
| 9.10 | | | | See Figure 2 and Figure 9, $V_{CANL}$ = 32 V, CANH = open, TXD = 0V | | | 160 | |
| 9.11 | $I_{OS(SS)\_REC}$ | Short-circuit steady-state output current, Recessive | | See Figure 2 and Figure 9, –20 V ≤ $V_{BUS}$ ≤ 32 V, Where $V_{BUS}$ = CANH = CANL, TXD = $V_{CC}$, Normal and Silent Modes | –8 | | 8 | mA |
| 9.12 | $C_O$ | Ouatput capacitance | | See receiver input capacitance | | | | |
| **10.0** | **DRIVER SWITCHING CHARACTERISTICS** | | | | | | | |
| 10.1 | $t_{pHR}$ | Propagation delay time,HIGH TXD to Driver Recessive | | See Figure 4, S = 0 V, $R_L$ = 60Ω, $C_L$ = 100pF, $R_{CM}$ = open | | 50 | 70 | ns |
| 10.2 | $t_{pLD}$ | Propagation delay time,LOW TXD to Driver Dominant | | | | 40 | 70 | |
| 10.3 | $t_{sk(p)}$ | Pulse skew ($\|t_{pHR} - t_{pLD}\|$) | | | | 10 | | |
| 10.4 | $t_R$ | Differential output signal rise time | | | | 10 | 30 | |
| 10.5 | $t_F$ | Differential output signal fall time | | | | 17 | 30 | |

(2) For the bus output voltage (recessive) will be the same if the device is in normal mode with S pin LOW or if the device is in silent mode with the S pin is HIGH.

## ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, $T_A$ = –40°C to 125°C (unless otherwise noted). SN65HVD256 device $V_{RXD} = V_{CC}$.

| | PARAMETER | | TEST CONDITIONS / COMMENT | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| 10.6 | $t_{R(10k)}$ | Differential output signal rise time, $R_L$ = 10kΩ | See Figure 4, S = 0 V, $R_L$ = 10kΩ, $C_L$ = 10pF, $R_{CM}$ = open | | | 35 | ns |
| 10.7 | $t_{F(10k)}$ | Differential output signal fall time, $R_L$ = 10kΩ | | | | 100 | |
| 10.8 | $t_{TXD\_DTO}$ | Dominant time out(3) | See Figure 8, $R_L$ = 60Ω, $C_L$ = open | 1175 | | 3700 | µs |
| **11.0** | **RECEIVER ELECTRICAL CHARACTERISTICS** | | | | | | |
| 11.1 | $V_{IT+}$ | Positive-going input threshold voltage, normal mode | See Figure 5 and Table 3. | | | 900 | mV |
| 11.2 | $V_{IT–}$ | Negative-going input threshold voltage, normal mode | | 500 | | | mV |
| 11.3 | $V_{HYS}$ | Hysteresis voltage ($V_{IT+}$ - $V_{IT–}$) | | | 125 | | mV |
| 11.4 | $I_{IOFF(LKG)}$ | Power-off (unpowered) bus input leakage current | CANH = CANL = 5 V, $V_{CC}$ = 0 V, $V_{RXD}$ = 0 V | | | 5.5 | µA |
| 11.5 | $C_I$ | Input capacitance to ground (CANH or CANL) | TXD = $V_{CC}$, $V_{RXD}$ = $V_{CC}$, $V_I$ = 0.4 sin (4E6 π t) + 2.5 V | | 25 | | pF |
| 11.6 | $C_{ID}$ | Differential input capacitance | TXD = $V_{CC}$, $V_{RXD}$ = $V_{CC}$, VI = 0.4 sin (4E6 π t) | | 10 | | pF |
| 11.7 | $R_{ID}$ | Differential input resistance | TXD = $V_{CC}$ = $V_{RXD}$ = 5 V, S = 0 V | 3 | | 80 | kΩ |
| 11.8 | $R_{IN}$ | Input resistance (CANH or CANL) | | 15 | | 40 | kΩ |
| 11.9 | $R_{IN(M)}$ | Input resistance matching: [1 – ($R_{IN(CANH)}$) / $R_{IN(CANL)}$)] × 100% | $V_{(CANH)}$ = $V_{(CANL)}$, –40°C ≤ $T_A$ ≤ 85°C | –3% | | 3% | |
| **12.0** | **RECEIVER SWITCHING CHARACTERISTICS** | | | | | | |
| 12.1 | $t_{PRH}$ | Propagation delay time, recessive input to high output | See Figure 5, $C_{L\_RXD}$ = 15pF | | 70 | 90 | ns |
| 12.2 | $t_{PDL}$ | Propagation delay time, dominant input to low output | | | 70 | 90 | ns |
| 12.3 | $t_R$ | Output signal rise time | | | 4 | 20 | ns |
| 12.4 | $t_F$ | Output signal fall time | | | 4 | 20 | ns |

(3) The TXD dominant time out ($t_{TXD\_DTO}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{TXD\_DTO}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{TXD\_DTO}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{TXD\_DTO}$ = 11 bits / 1175 µs = 9.4 kbps.

## THERMAL CHARACTERISTICS

| 13.0 | THERMAL METRIC(1) | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| 13.1 | $\theta_{JA}$ | Junction-to-air thermal resistance | High-K thermal resistance(2) | 107.5 | °C/W |
| 13.2 | $\theta_{JB}$ | Junction-to-board thermal resistance(3) | | 48.9 | |
| 13.3 | $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance(4) | | 56.7 | |
| 13.4 | $\Psi_{JT}$ | Junction-to-top characterization parameter(5) | | 12.1 | |
| 13.5 | $\Psi_{JB}$ | Junction-to-board characterization parameter(6) | | 48.2 | |
| 13.6 | $P_D$ | Average power dissipation | $V_{CC}$ = 5 V, $V_{RXD}$ = 5 V, $T_J$ = 27°C, $R_L$ = 60Ω, S at 0 V, Input to TXD at 250 kHz, 25% duty cycle square wave, $C_{L\_RXD}$ = 15 pF. Typical CAN operating conditions at 500kbps with 25% transmission (dominant) rate. | 115 | mW |
| 13.7 | | | $V_{CC}$ = 5.5 V, $V_{RXD}$ = 5.5 V, $T_J$ = 150°C, $R_L$ = 50Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF. Typical high load CAN operating conditions at 1mbps with 50% transmission (dominant) rate and loaded network. | 268 | |
| 13.8 | | Thermal shutdown temperature | | 170 | °C |
| 13.9 | | Thermal shutdown hysteresis | | 5 | °C |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) he junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-top characterization parameter, $\Psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\Psi_{JB}$ estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

## PARAMETER MEASUREMENT INFORMATION

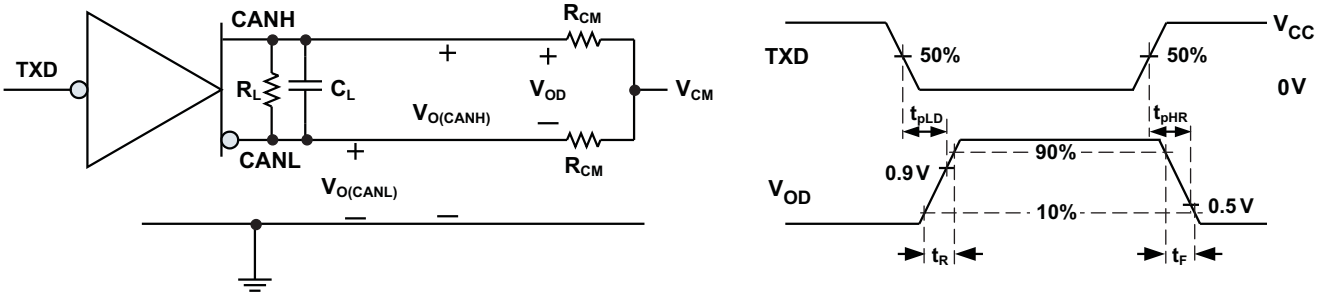



**Figure 4. Driver Test Circuit and Measurement**

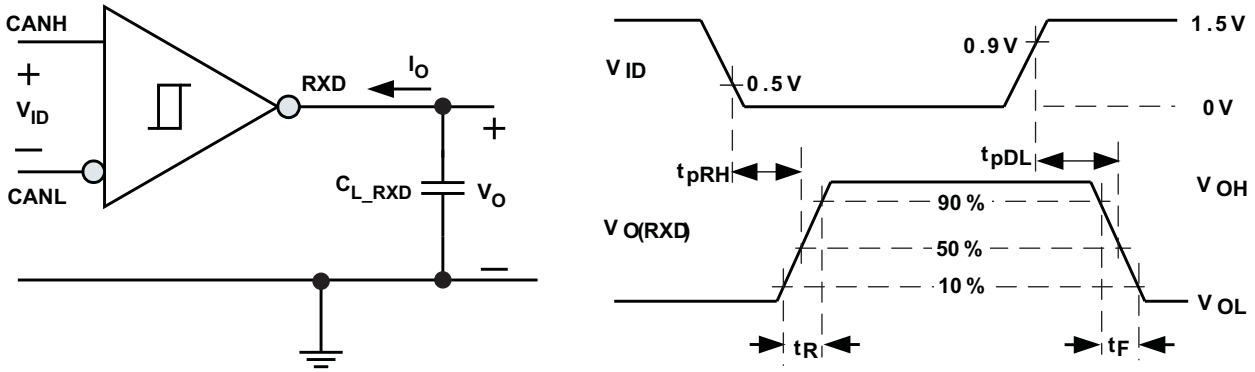



**Figure 5. Receiver Test Circuit and Measurement**

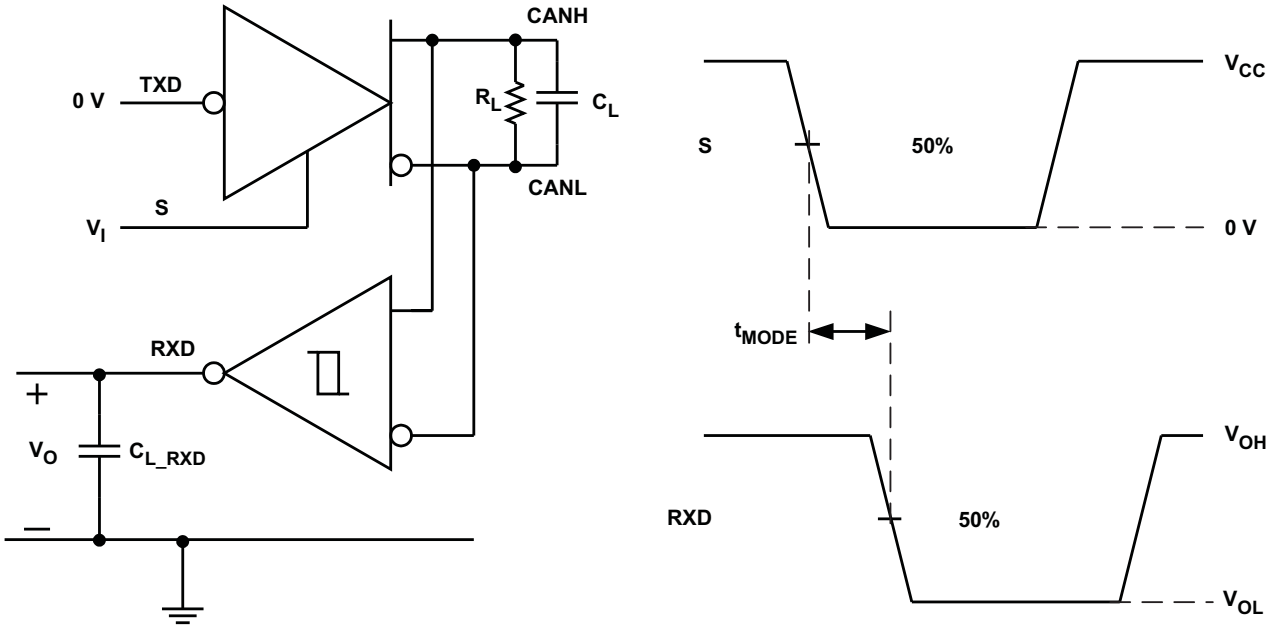



**Figure 6. $t_{MODE}$ Test Circuit and Measurement**

## PARAMETER MEASUREMENT INFORMATION (continued)

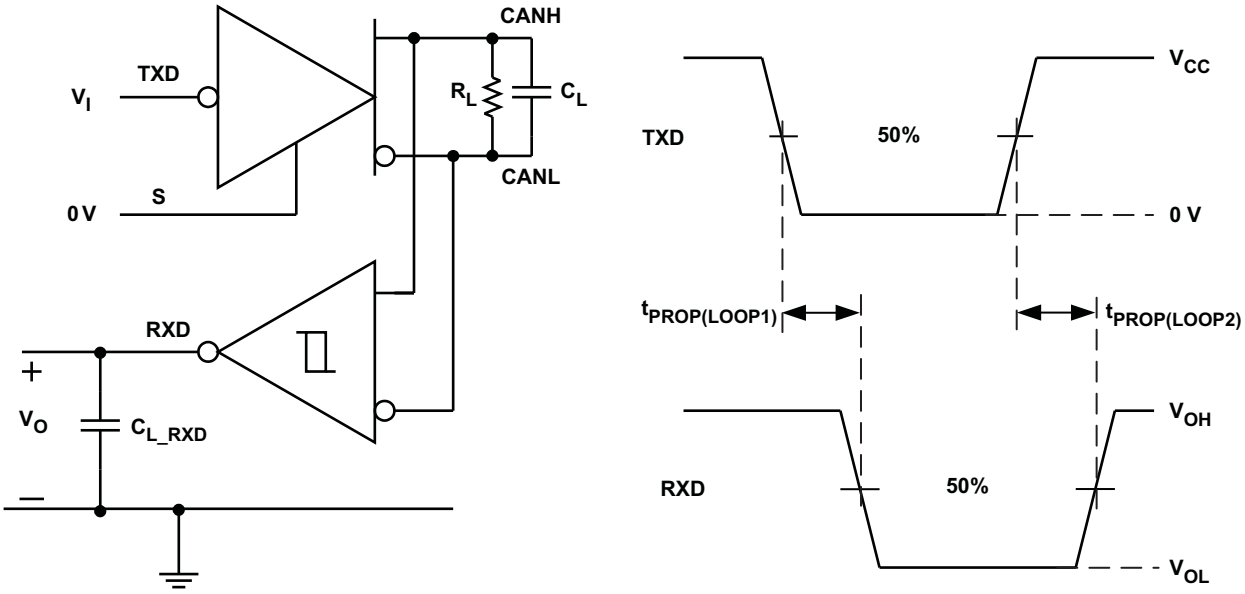



**Figure 7. $T_{PROP(LOOP)}$ Test Circuit and Measurement**

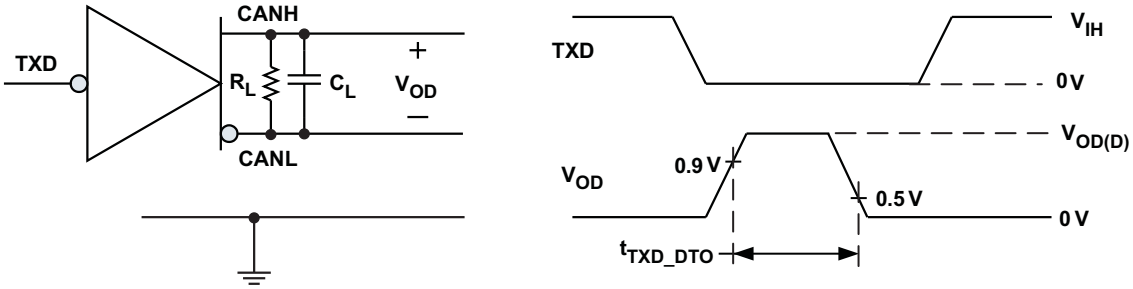



**Figure 8. TXD Dominant Time Out Test Circuit and Measurement**

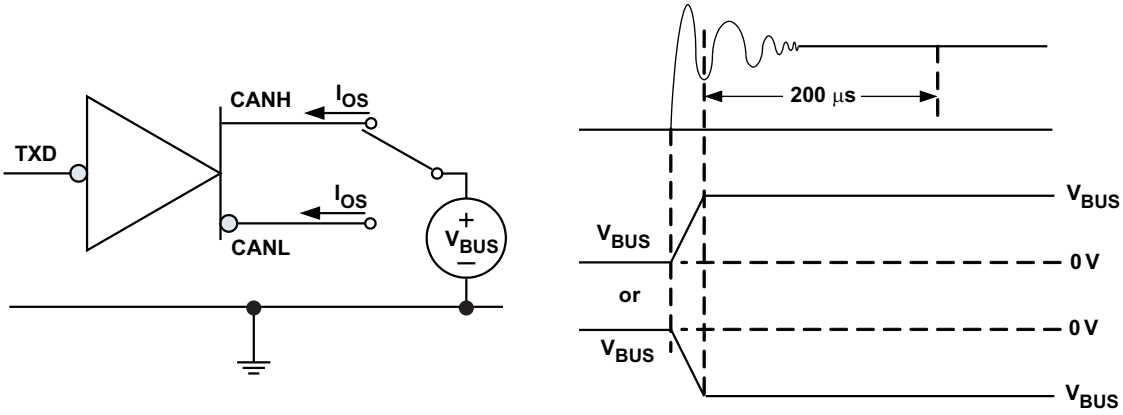



**Figure 9. Driver Short-Circuit Current Test and Measurement**

## APPLICATION INFORMATION

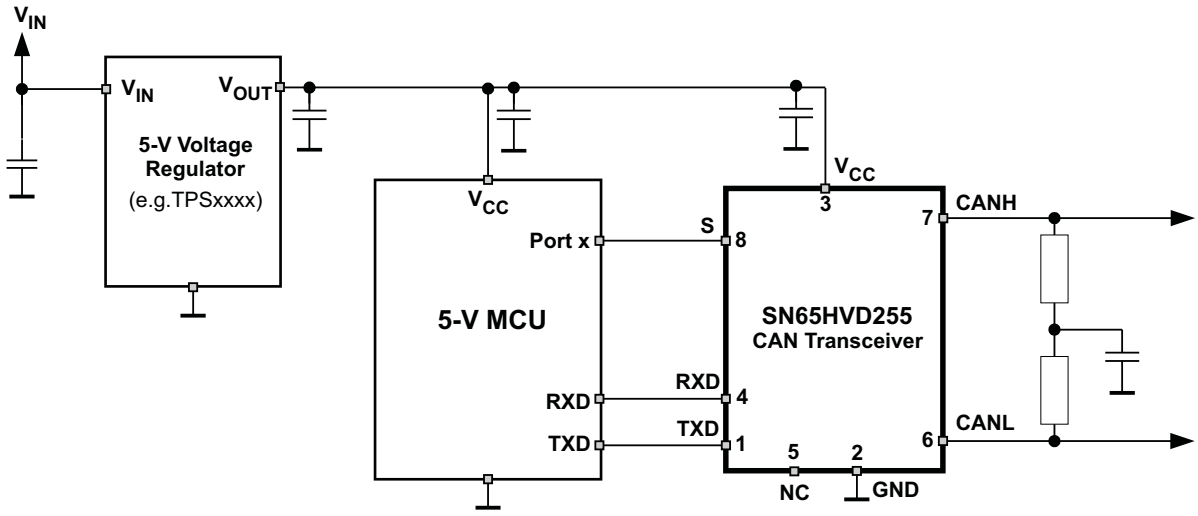



**Figure 10. Typical 5V Application**

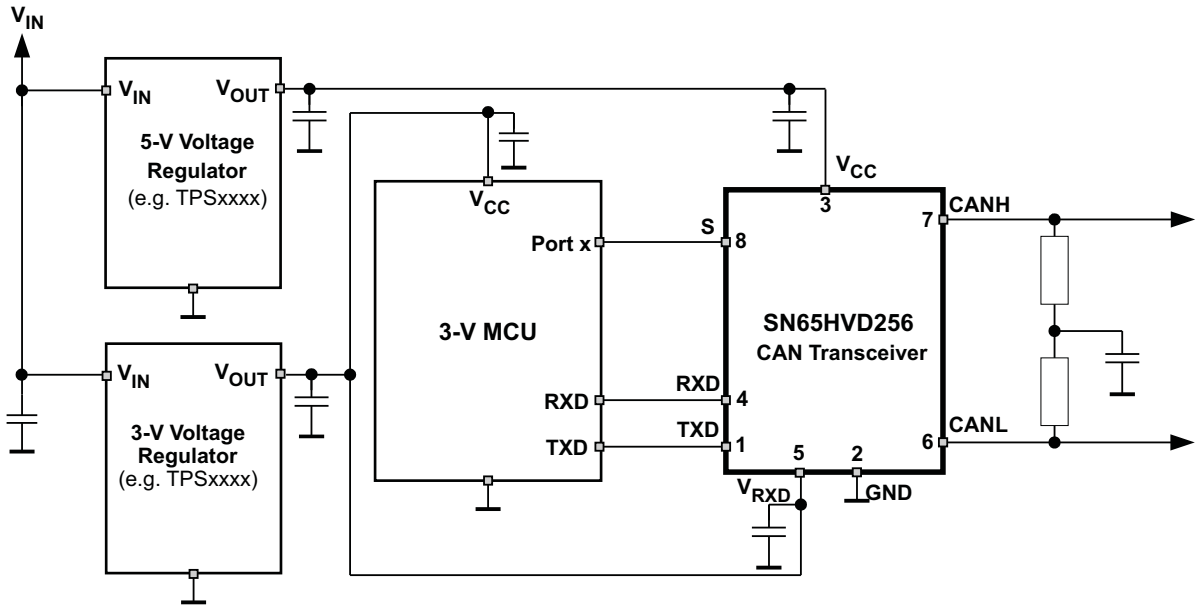



**Figure 11. Typical 3.3V Application**

## CAN TERMINATION

CAN is designed for use with twisted pair cabling of 120Ω characteristic impedance in a bus topology. The bus should be properly terminated at both ends with 120Ω resistors that match this impedance to avoid signal reflections. If nodes may be removed from the bus care must be used where to place the termination such that it is not removed from the bus.

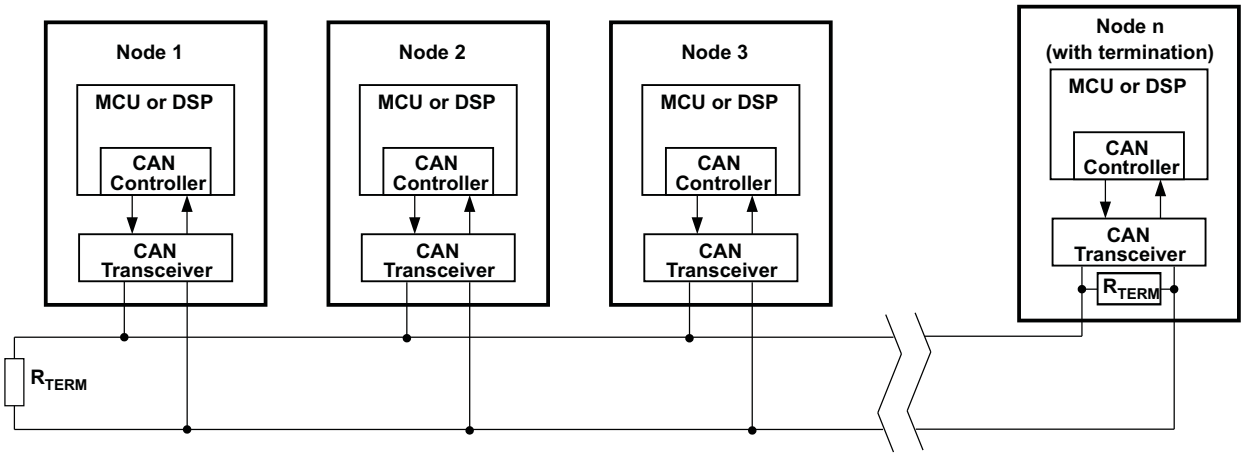



**Figure 12. Typical CAN Bus**

Termination may be a single 120Ω resistor at the end of the bus either on the cable or in a "terminating node". If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” may used, see Figure 13. Utilizing split termination in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

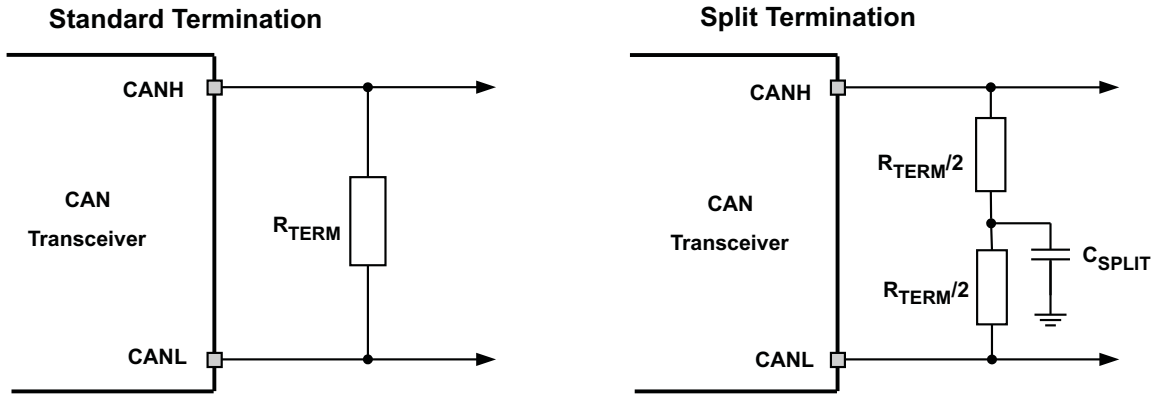



**Figure 13. CAN Bus Termination Concepts**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN65HVD255D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN65HVD255DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN65HVD256D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN65HVD256DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

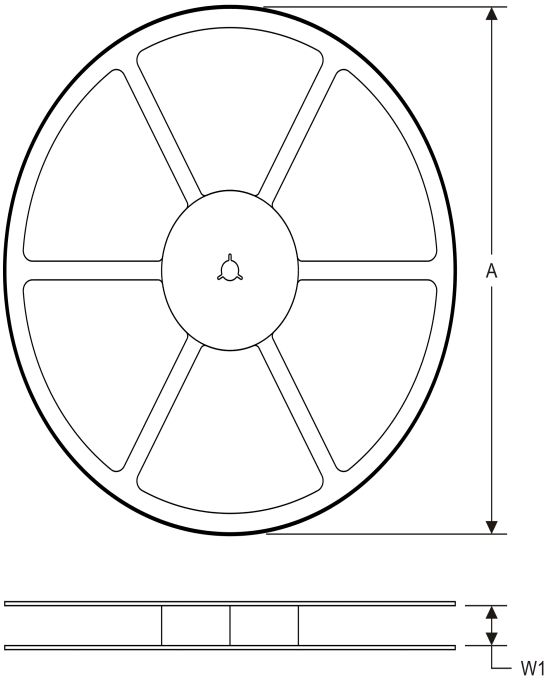
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

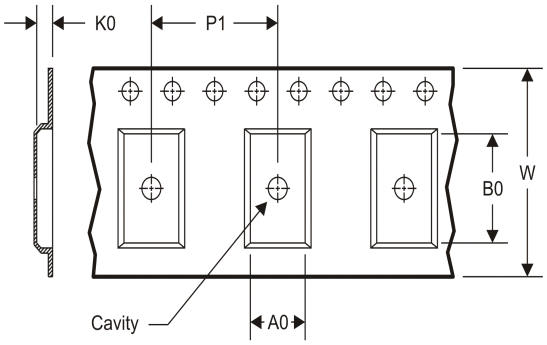
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



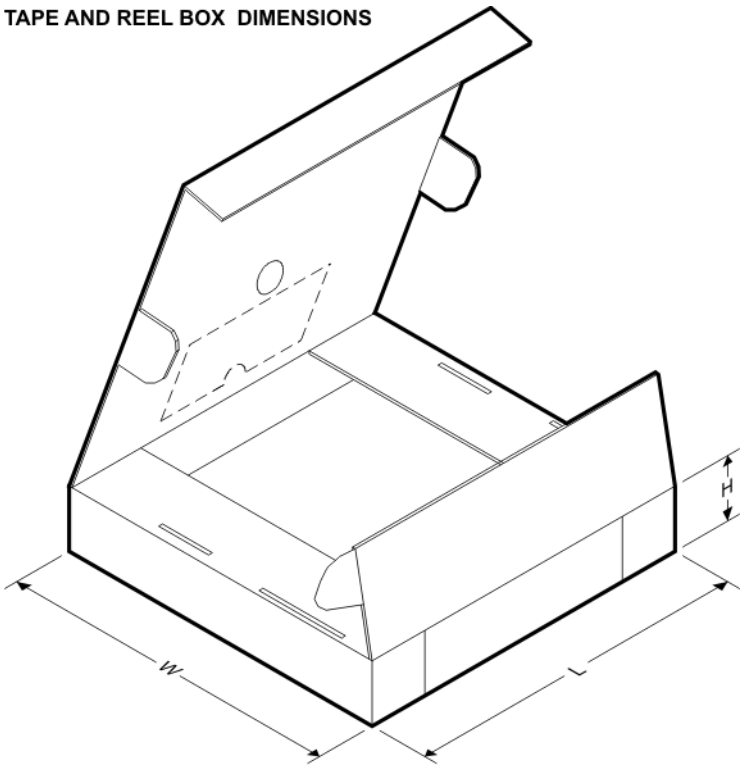

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD255DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD256DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

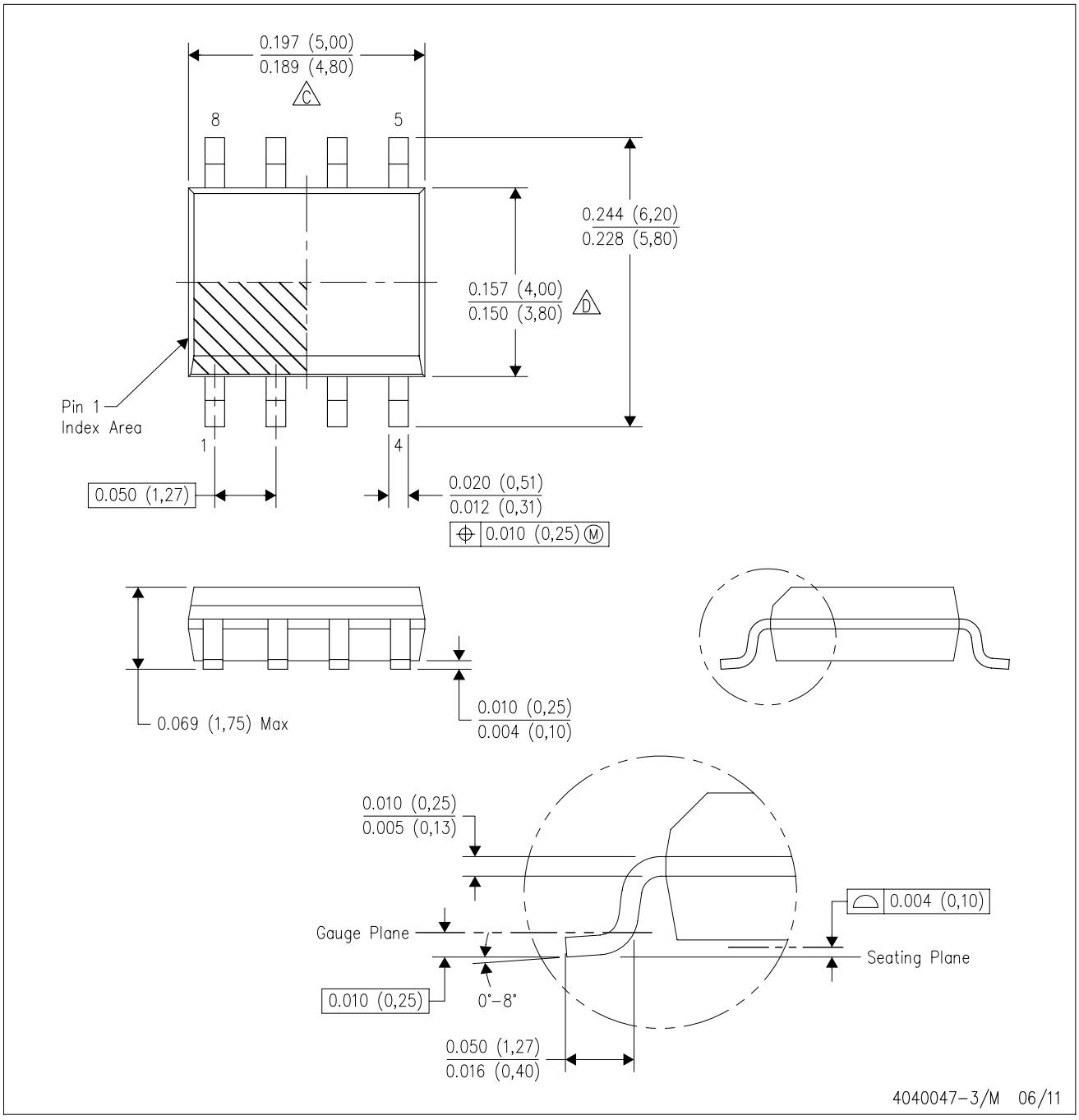
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

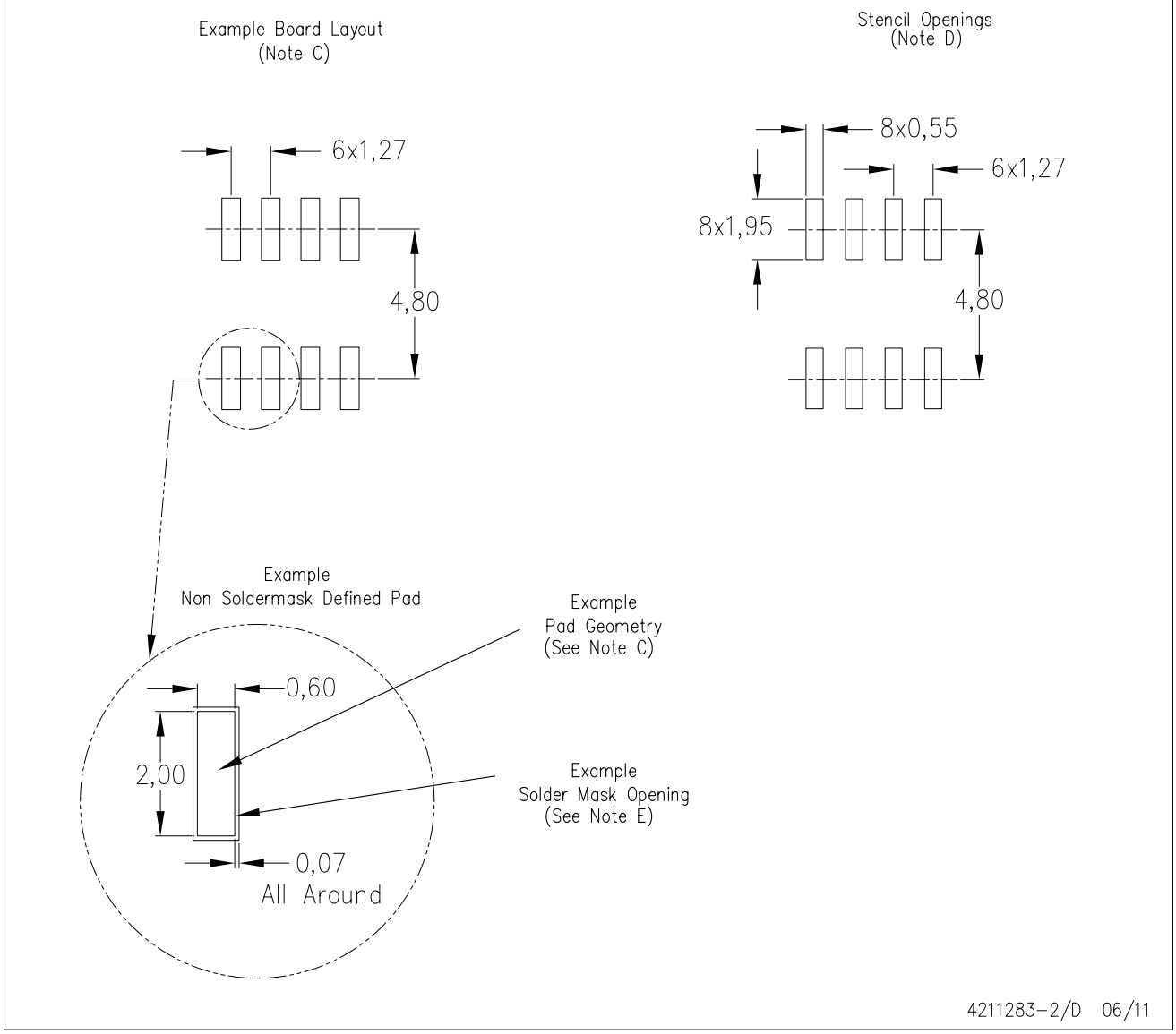
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVD255DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65HVD256DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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