

# SN54ABT240, SN74ABT240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS098I – JANUARY 1991 – REVISED JUNE 2002

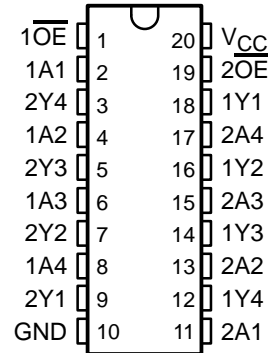
- Typical  $V_{OLP}$  (Output Ground Bounce)  
 $<1\text{ V}$  at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description

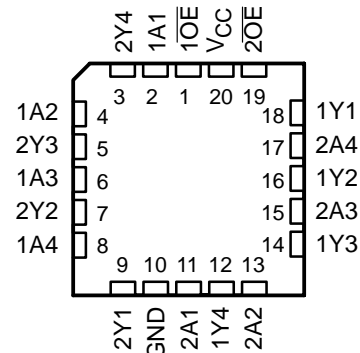
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT241, SN74ABT241A, SN54ABT244, and SN74ABT244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs.

The SN54ABT240 and SN74ABT240A are organized as two 4-bit buffers/line drivers with separate  $\overline{OE}$  inputs. When  $\overline{OE}$  is low, the devices pass inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

SN54ABT240 . . . J OR W PACKAGE  
 SN74ABT240A . . . DB, DW, N, NS, OR PW PACKAGE  
 (TOP VIEW)



SN54ABT240 . . . FK PACKAGE  
 (TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	PDIP – N	Tube	SN74ABT240AN	SN74ABT240AN
	SOIC – DW	Tube	SN74ABT240ADW	ABT240A
		Tape and reel	SN74ABT240ADWR	
	SOP – NS	Tape and reel	SN74ABT240ANSR	ABT240A
	SSOP – DB	Tape and reel	SN74ABT240ADBR	AB240A
$-55^\circ\text{C}$ to $125^\circ\text{C}$	TSSOP – PW	Tape and reel	SN74ABT240APWR	AB240A
	CDIP – J	Tube	SNJ54ABT240J	SNJ54ABT240J
	CFP – W	Tube	SNJ54ABT240W	SNJ54ABT240W
	LCCC – FK	Tube	SNJ54ABT240FK	SNJ54ABT240FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description (continued)

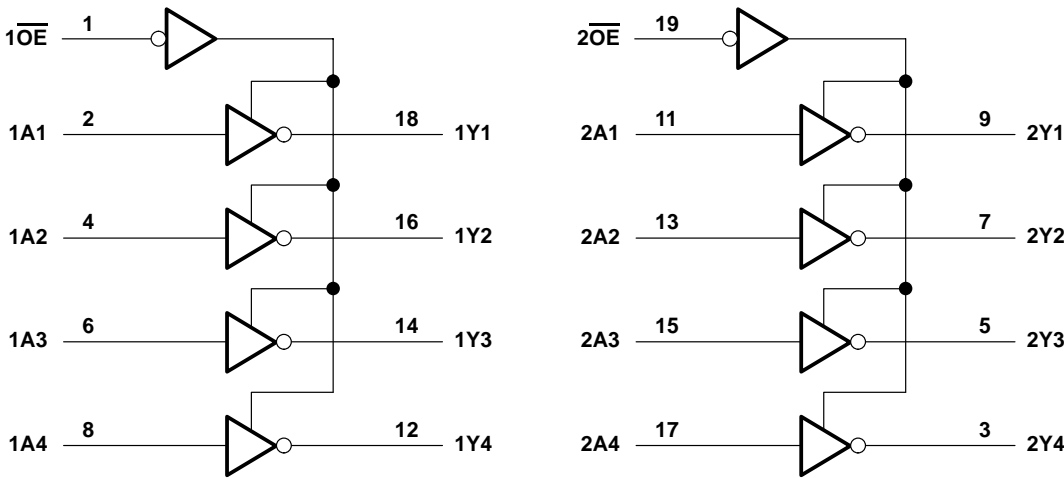
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT240	96 mA
SN74ABT240A	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54ABT240, SN74ABT240A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

			SN54ABT240		SN74ABT240A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			–24		–32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT240		SN74ABT240A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA			–1.2		–1.2		–1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA	2.5			2.5		2.5		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA	3			3		3		
		V <sub>CC</sub> = 4.5 V			2	2				
					2*			2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V			0.55	0.55				V
					0.55*			0.55		
V <sub>hys</sub>				100						mV
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			10	10		10		μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			–10	–10		–10		μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100			±100		μA
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50	50		50		μA
I <sub>O†</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			1	250	250	250		μA
					24	30	30	30		mA
					0.5	250	250	250		μA
ΔI <sub>CC</sub> §	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5	1.5		1.5		mA
					0.05	0.05		0.05		
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5	1.5		1.5		
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V			4					pF
C <sub>o</sub>		V <sub>O</sub> = 2.5 V or 0.5 V			7.5					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



# SN54ABT240, SN74ABT240A

## OCTAL BUFFERS/DRIVERS

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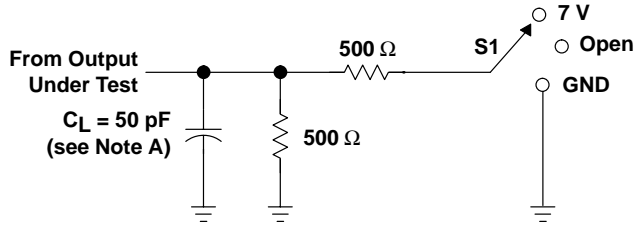
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT240					UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	1	2.9	4.3	0.8	5.5	ns
t <sub>PHL</sub>			1.6	3.1	4.5	1	5.5	
t <sub>PZH</sub>	OE	Y	1.1	3.1	5.8	0.8	7.5	ns
t <sub>PZL</sub>			1.1	2.7	6.2	0.8	7.7	
t <sub>PHZ</sub>	OE	Y	1.8	4.6	5.9	1.7	7	ns
t <sub>PLZ</sub>			1.6	4	5.9	1.3	7.2	

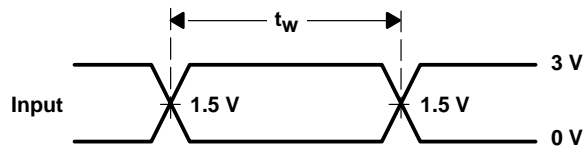
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT240A					UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	1	2.9	4.1	1	4.8	ns
t <sub>PHL</sub>			1.6	3.1	4.6	1.6	4.8	
t <sub>PZH</sub>	OE	Y	1.1	3.1	4.7	1.1	5.2	ns
t <sub>PZL</sub>			1.1	2.7	5.8	1.1	6.2	
t <sub>PHZ</sub>	OE	Y	1.8	4.6	5.7	1.8	6.4	ns
t <sub>PLZ</sub>			1.6	4	5.4	1.6	5.8	

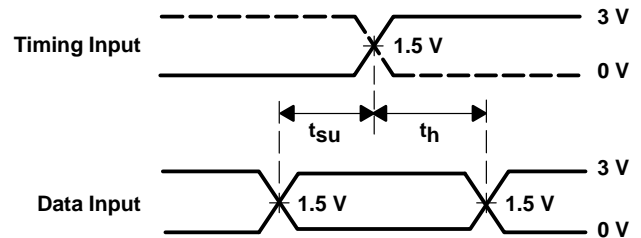
## PARAMETER MEASUREMENT INFORMATION



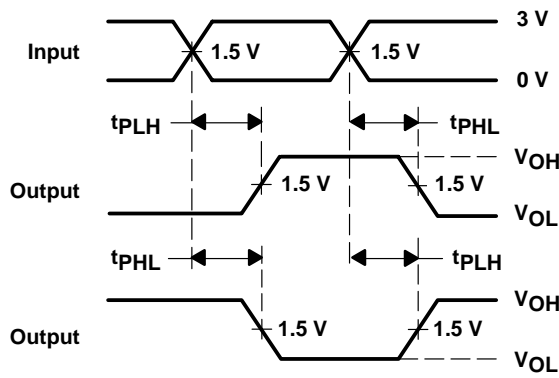
LOAD CIRCUIT



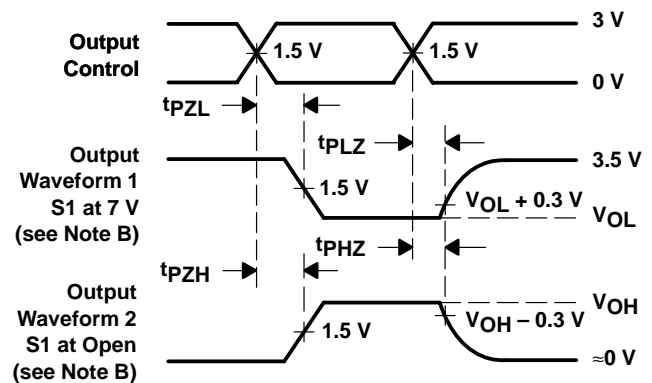
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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