

SN74AVCAH164245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A – JULY 2002 – REVISED MAY 2004

- Member of the Texas Instruments Widebus™ Family
- DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCA} Voltage
- If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A-port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B-port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCAH164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCAH164245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA} .

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, then both ports are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVCAH164245GR	AVCAH164245
	TVSOP – DGV	Tape and reel	SN74AVCAH164245VR	WAH4245
	VFBGA – GQL	Tape and reel	SN74AVCAH164245KR	WAH4245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DOC and Widebus are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

SN74AVCAH164245

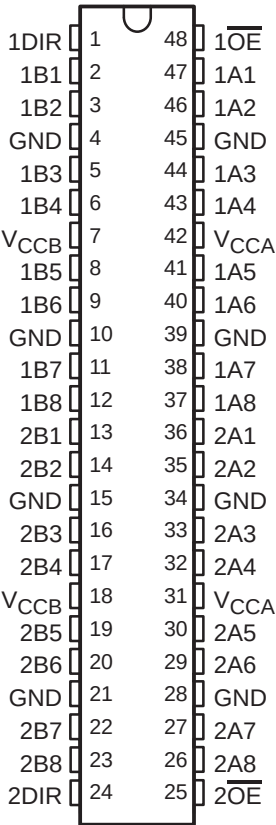
16-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

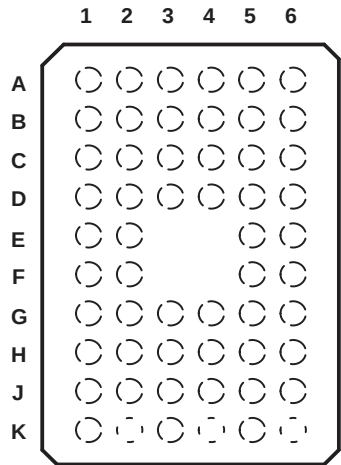
SCES396A – JULY 2002 – REVISED MAY 2004

terminal assignments

DGG OR DGV PACKAGE
(TOP VIEW)



GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1OE
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	VCCB	VCCA	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2OE

NC – No internal connection

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Logic diagram of the 2A1 channel in the 74181 ALU. The diagram shows inputs 2DIR (pin 24) and 2A1 (pin 36) connected to two AND gates and two inverters. The output of the top AND gate is 2OE (pin 25). The output of the bottom AND gate is 2B1 (pin 13). The outputs of the two inverters are connected to a bracket labeled 'To Seven Other Channels'.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CCA} and V_{CCB}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): I/O ports (A port)	–0.5 V to 4.6 V
I/O ports (B port)	–0.5 V to 4.6 V
Control inputs	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O	
(see Note 1): (A port)	–0.5 V to 4.6 V
(B port)	–0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O	
(see Notes 1 and 2): (A port)	–0.5 V to $V_{CCA} + 0.5$ V
(B port)	–0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CCA} , V_{CCB} , or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	28°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AVCAH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A – JULY 2002 – REVISED MAY 2004

recommended operating conditions (see Notes 4 through 6)

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.4	3.6	V
V _{CCB}	Supply voltage				1.4	3.6	V
V _{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		V _{CCI} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V		V _{CCI} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _{IH}	High-level input voltage	Control inputs (Referenced to V _{CCA})	1.4 V to 1.95 V		V _{CCA} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Control inputs (Referenced to V _{CCA})	1.4 V to 1.95 V		V _{CCA} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _I	Input voltage				0	3.6	V
V _O	Output voltage	Active state			0	V _{CCO}	V
		3-state			0	3.6	
I _{OH}	High-level output current			1.4 V to 1.6 V	−2		mA
				1.65 V to 1.95 V	−4		
				2.3 V to 2.7 V	−8		
				3 V to 3.6 V	−12		
I _{OL}	Low-level output current			1.4 V to 1.6 V	2		mA
				1.65 V to 1.95 V	4		
				2.3 V to 2.7 V	8		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T _A	Operating free-air temperature				−40	85	°C

- NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 7 and 8)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	MIN	TYP [†]	MAX	UNIT
V _{OH}			I _{OH} = -100 μA V _I = V _{IH}	1.4 V to 3.6 V	1.4 V to 3.6 V	V _{CCO} -0.2 V			V
			I _{OH} = -2 mA V _I = V _{IH}	1.4 V	1.4 V	1.05			
			I _{OH} = -4 mA V _I = V _{IH}	1.65 V	1.65 V	1.2			
			I _{OH} = -8 mA V _I = V _{IH}	2.3 V	2.3 V	1.75			
			I _{OH} = -12 mA V _I = V _{IH}	3 V	3 V	2.3			
V _{OL}			I _{OH} = 100 μA V _I = V _{IL}	1.4 V to 3.6 V	1.4 V to 3.6 V	0.2			V
			I _{OH} = 2 mA V _I = V _{IL}	1.4 V	1.4 V	0.35			
			I _{OH} = 4 mA V _I = V _{IL}	1.65 V	1.65 V	0.45			
			I _{OH} = 8 mA V _I = V _{IL}	2.3 V	2.3 V	0.55			
			I _{OH} = 12 mA V _I = V _{IL}	3 V	3 V	0.7			
I _I	Control inputs	V _I = V _{CCA} or GND		1.4 V to 3.6 V	3.6 V	±2.5			μA
I _{BHL} [‡]			V _I = 0.49 V	1.4 V	1.4 V	11			μA
			V _I = 0.57 V	1.65 V	1.65 V	30			
			V _I = 0.7 V	2.3 V	2.3 V	45			
			V _I = 0.8 V	3 V	3 V	75			
I _{BHH} [§]			V _I = 0.91 V	1.4 V	1.4 V	-11			μA
			V _I = 1.07 V	1.65 V	1.65 V	-30			
			V _I = 1.7 V	2.3 V	2.3 V	-45			
			V _I = 2 V	3 V	3 V	-75			
I _{BHLO} [¶]			V _I = 0 to V _{CC}	1.6 V	1.6 V	100			μA
				1.95 V	1.95 V	200			
				2.7 V	2.7 V	300			
				3.6 V	3.6 V	525			
I _{BHHO} [#]			V _I = 0 to V _{CC}	1.6 V	1.6 V	-100			μA
				1.95 V	1.95 V	-200			
				2.7 V	2.7 V	-300			
				3.6 V	3.6 V	-525			
I _{off}	A port	V _I or V _O = 0 to 3.6 V		0 V	0 to 3.6 V	±10			μA
	B port			0 to 3.6 V	0 V	±10			
I _{OZ}	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{\text{OE}}$ = V _{IH}	3.6 V	3.6 V	±12.5			μA
	B port		$\overline{\text{OE}}$ = don't care	0 V	3.6 V	±12.5			
	A port			3.6 V	0 V	±12.5			

[†] All typical values are at T_A = 25°C.

[‡] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[§] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.

^{||} For I/O ports, the parameter I_{OZ} includes the input leakage current.

NOTES: 7. V_{CCO} is the V_{CC} associated with the output port.

8. V_{CCI} is the V_{CC} associated with the input port.

SN74AVCAH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A – JULY 2002 – REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (continued)
(unless otherwise noted) (see Note 9)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP [†]	MAX	UNIT
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.6 V	1.6 V			20	μA
			1.95 V	1.95 V			20	
			2.7 V	2.7 V			30	
			0 V	3.6 V			–40	
			3.6 V	0 V			40	
			3.6 V	3.6 V			40	
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.6 V	1.6 V			20	μA
			1.95 V	1.95 V			20	
			2.7 V	2.7 V			30	
			0 V	3.6 V			40	
			3.6 V	0 V			–40	
			3.6 V	3.6 V			40	
C _i	Control inputs	V _I = 3.3 V or GND	3.3 V	3.3 V		4		pF
C _{io}	A or B ports	V _O = 3.3 V or GND	3.3 V	3.3 V		5		pF

[†] All typical values are at T_A = 25°C.

NOTE 9: V_{CCI} is the V_{CC} associated with the input port.

switching characteristics over recommended operating free-air temperature range,
V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t _{en}	$\overline{\text{OE}}$	A	2.6	8.4	2.7	8.2	2.3	6.3	2.1	5.6	ns
	$\overline{\text{OE}}$	B	2.7	8.6	3.2	10.2	3.2	10.8	3.2	10.7	
t _{dis}	$\overline{\text{OE}}$	A	2.1	7	2.5	7	1.7	5.3	2	6.1	ns
	$\overline{\text{OE}}$	B	2.1	7.1	2.5	7.1	2.1	6.5	2.1	6.4	

switching characteristics over recommended operating free-air temperature range,
V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.4	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t _{en}	$\overline{\text{OE}}$	A	2.5	8	2.7	7.8	2.2	5.8	2	5.1	ns
	$\overline{\text{OE}}$	B	1.8	6.7	2.7	7.8	2.7	8.1	2.7	8.1	
t _{dis}	$\overline{\text{OE}}$	A	2.1	6.4	2.5	6.4	1.5	4.5	1.8	5	ns
	$\overline{\text{OE}}$	B	2.1	6.6	2.5	6.4	2	5.5	2	5.5	



switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	$\overline{OE}$	A	2.6	7.4	2.7	7.2	2.2	5.3	2	4.5	ns
	$\overline{OE}$	B	1.2	4.1	2.2	5.1	2.2	5.3	2.2	5.3	
t_{dis}	$\overline{OE}$	A	2	5.7	2.3	5.7	1.4	3.7	1.6	4	ns
	$\overline{OE}$	B	0.9	4.5	1.7	4.5	1.4	3.7	1.4	3.7	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	$\overline{OE}$	A	2.5	7	2.6	6.9	2.1	5	1.9	4.1	ns
	$\overline{OE}$	B	0.8	2.6	1.9	4	2	4.1	1.9	4.1	
t_{dis}	$\overline{OE}$	A	1.2	5.4	2.2	5.2	1.2	3.3	1.5	3.6	ns
	$\overline{OE}$	B	1.2	5.4	1.7	4.4	1.5	3.6	1.5	3.6	

operating characteristics, V_{CCA} and $V_{CCB} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA}	Power dissipation capacitance per transceiver, A port input, B port output	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B port input, A port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB}	Power dissipation capacitance per transceiver, A port input, B port output	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B port input, A port output	Outputs enabled		20	
		Outputs disabled		7	

SN74AVCAH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A – JULY 2002 – REVISED MAY 2004

output description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

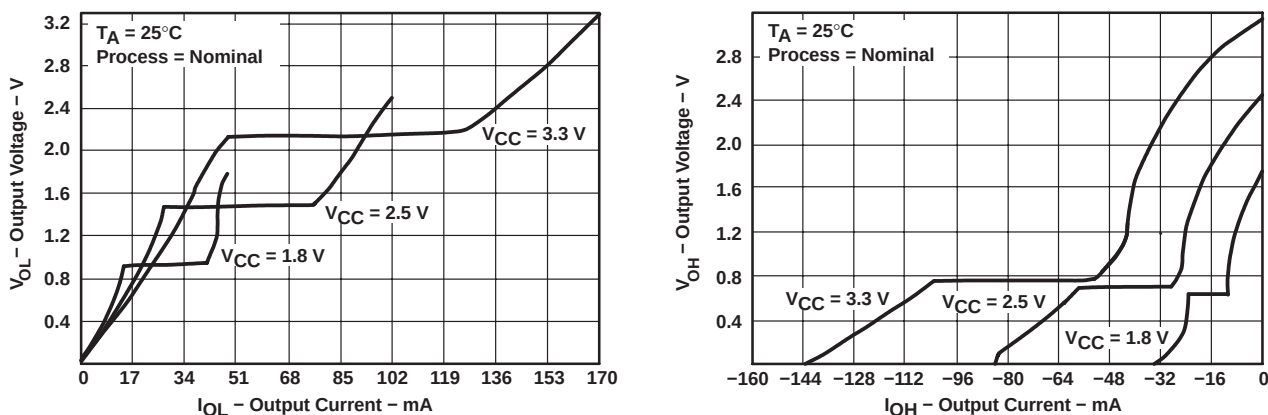


Figure 1. Output Voltage vs Output Current

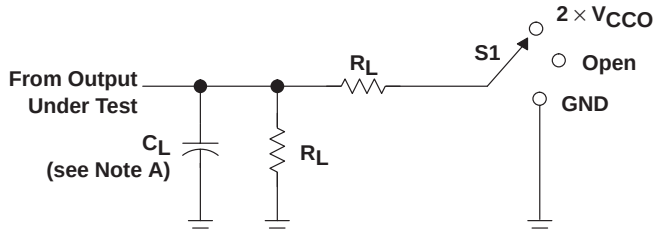
SN74AVCAH164245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A – JULY 2002 – REVISED MAY 2004

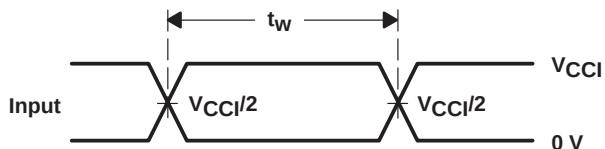
PARAMETER MEASUREMENT INFORMATION



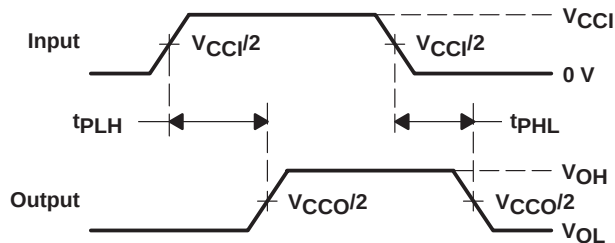
LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
$1.5 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k Ω	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	30 pF	500 Ω	0.3 V

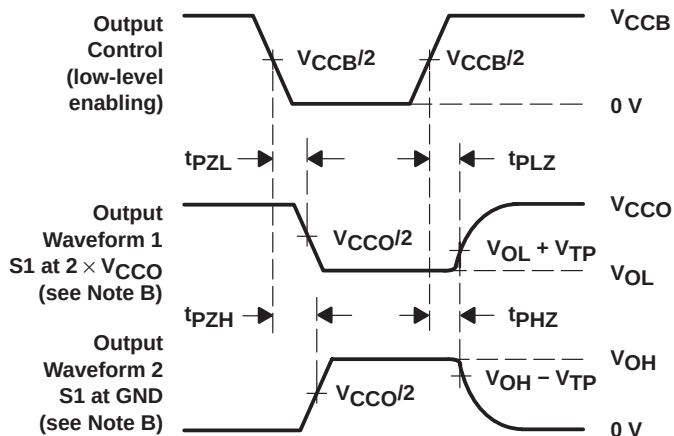
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



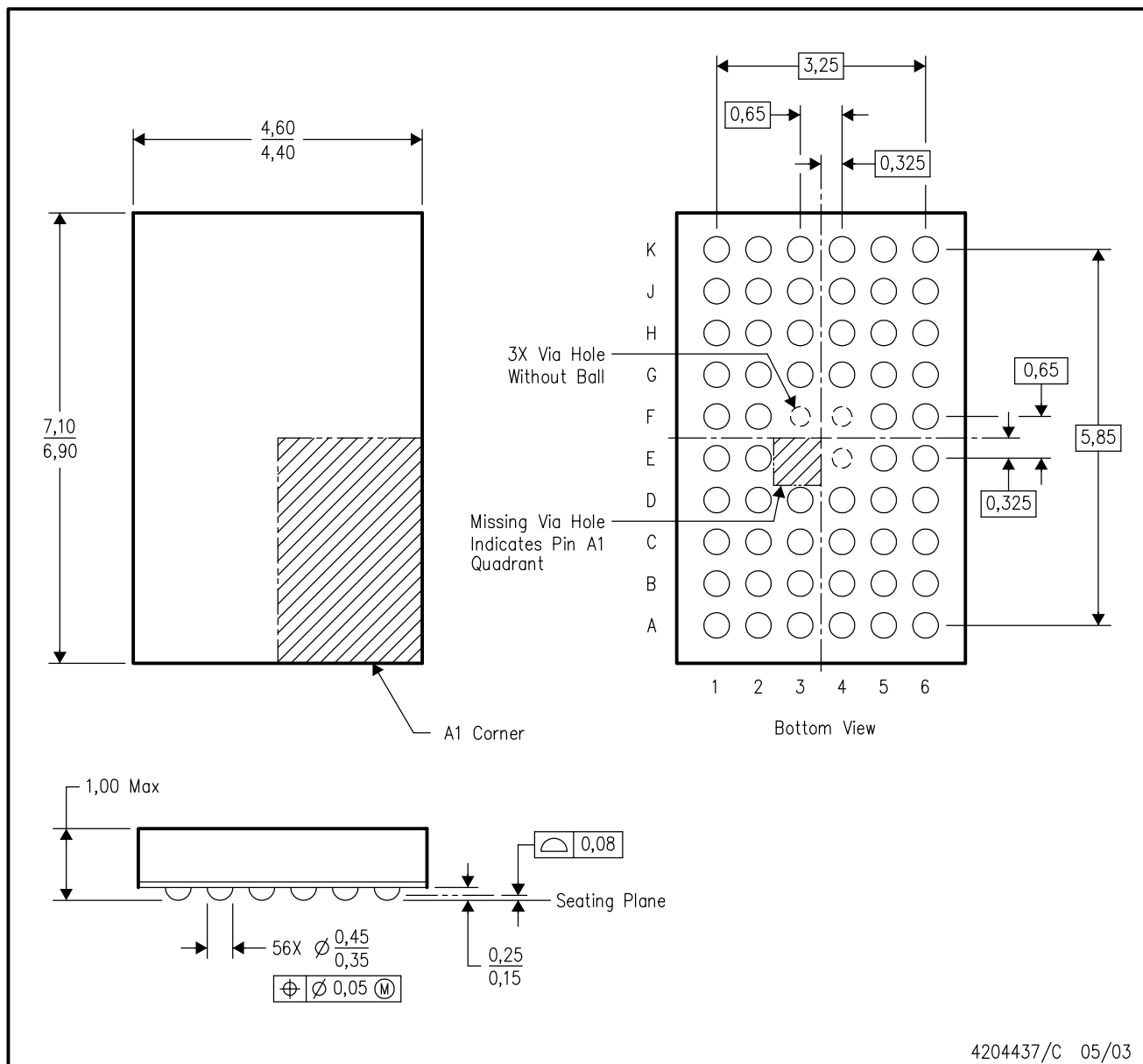
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$, $dv/dt \geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

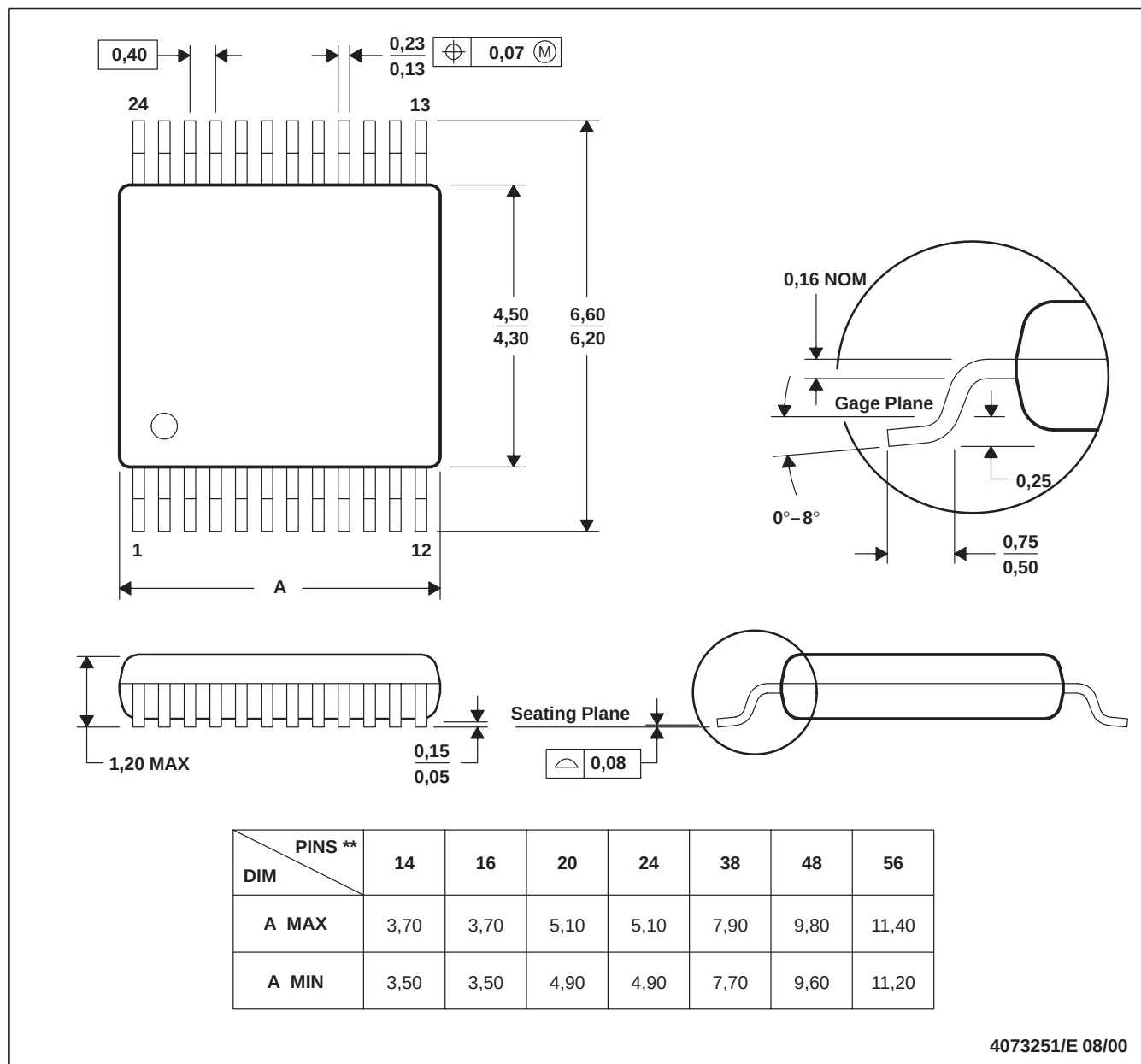


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - MicroStar Junior™ BGA configuration.
 - Falls within JEDEC MO-225 variation BA.
 - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

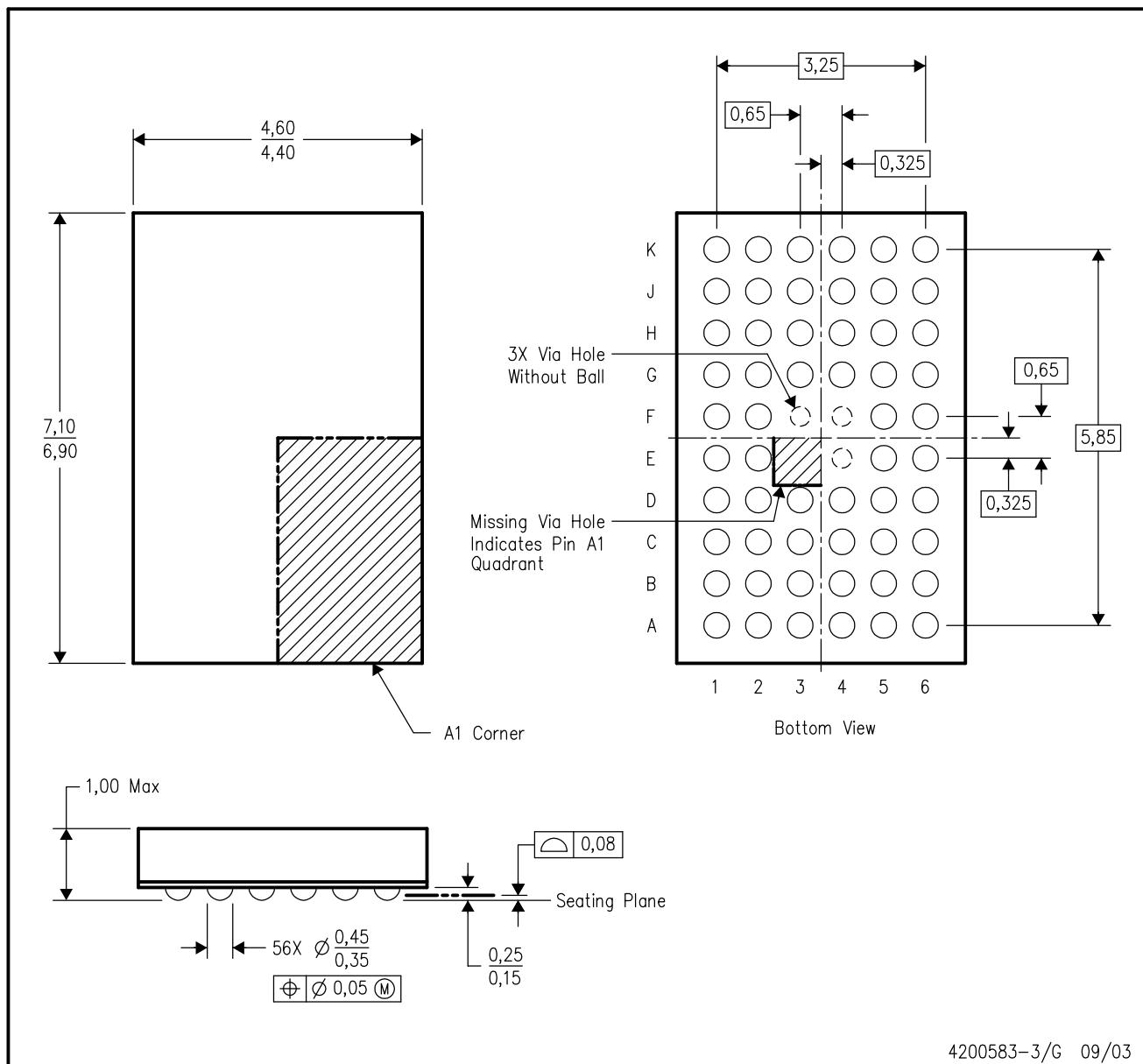
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



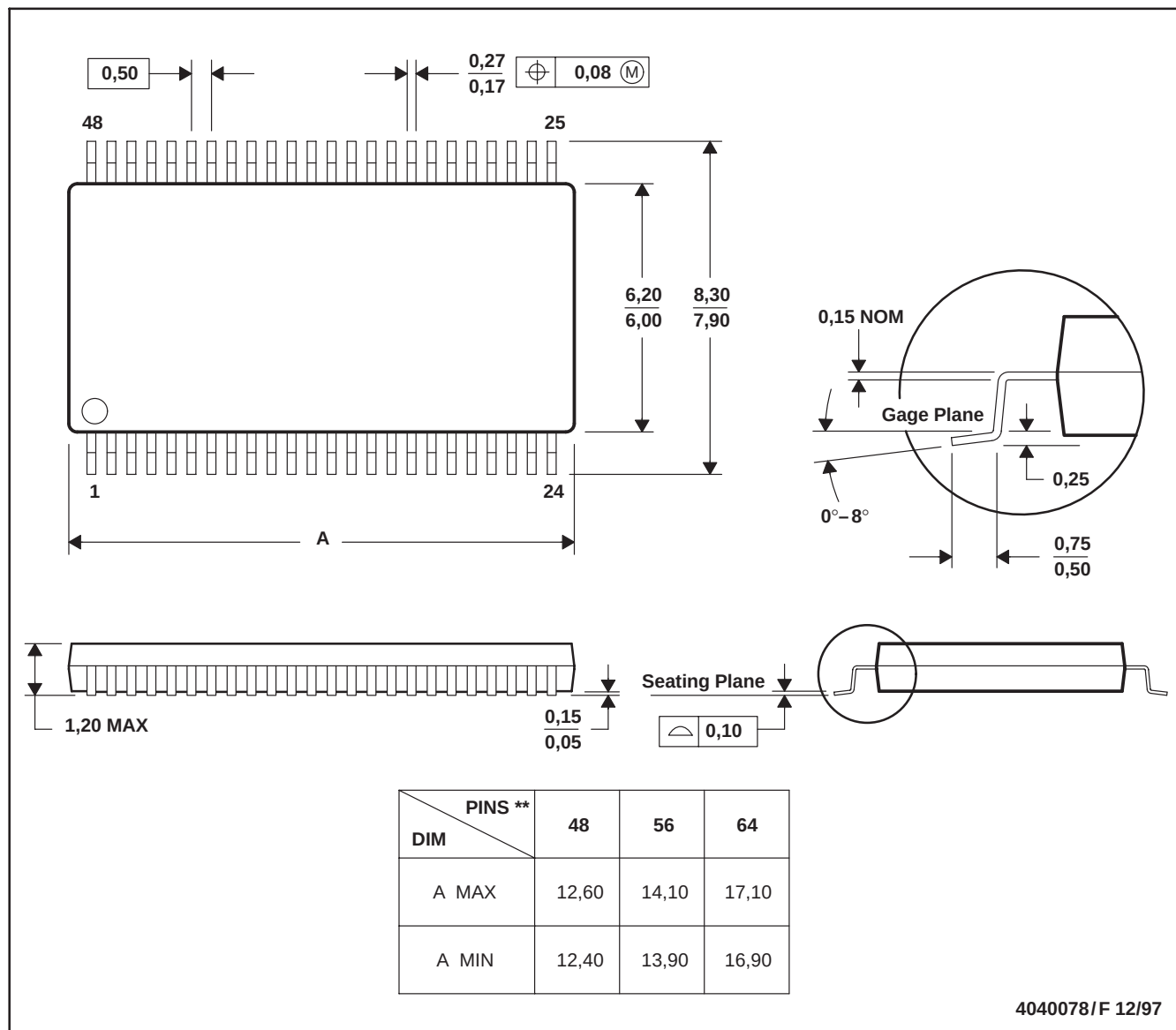
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - MicroStar Junior™ BGA configuration.
 - Falls within JEDEC MO-225 variation BA.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated