

# SN74AVCH1T45

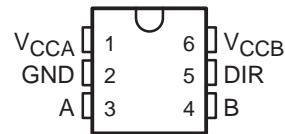
## SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

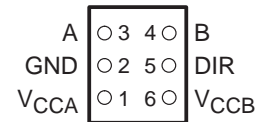
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- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE  
(TOP VIEW)



YEP OR YZP PACKAGE  
(BOTTOM VIEW)



#### description/ordering information

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCH1T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

The SN74AVCH1T45 is designed so that the DIR input is powered by  $V_{CCA}$ .

#### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AVCH1T45YEPR	___TF_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AVCH1T45YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74AVCH1T45DBVR	ET1_
	SOT (SC-70) – DCK	Tape and reel	SN74AVCH1T45DCKR	TF_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**description/ordering information (continued)**

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

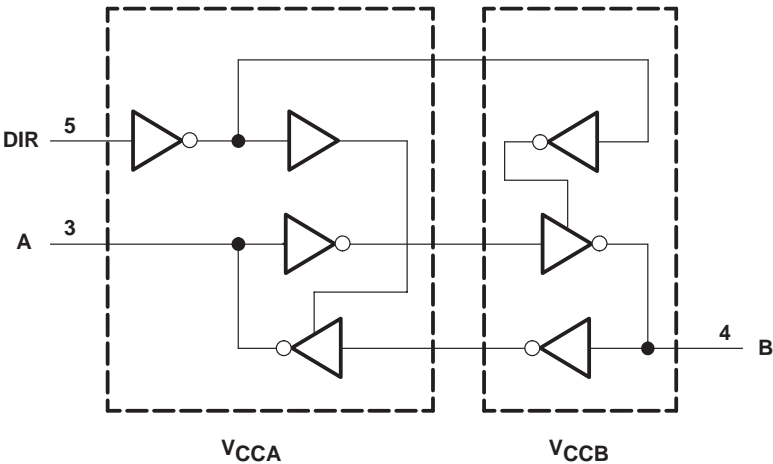
The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLE	
INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

**logic diagram (positive logic)**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CCA}$ and $V_{CCB}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): I/O ports (A port)	–0.5 V to 4.6 V
I/O ports (B port)	–0.5 V to 4.6 V
Control inputs	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	
(see Note 1): A port	–0.5 V to 4.6 V
B port	–0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, $V_O$	
(see Notes 1 and 2): A port	–0.5 V to $V_{CCA} + 0.5$ V
B port	–0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	165°C/W
DCK package	259°C/W
YEP/YZP package	123°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Notes 4 through 8)

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>IH</sub>	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) (see Note 8)	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) (see Note 8)	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	3.6	
I <sub>OH</sub>	High-level output current			1.2 V	−3		mA
				1.4 V to 1.6 V	−6		
				1.65 V to 1.95 V	−8		
				2.3 V to 2.7 V	−9		
				3 V to 3.6 V	−12		
I <sub>OL</sub>	Low-level output current			1.2 V	3		mA
				1.4 V to 1.6 V	6		
				1.65 V to 1.95 V	8		
				2.3 V to 2.7 V	9		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T <sub>A</sub>	Operating free-air temperature				−40	85	°C

- NOTES: 4. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.  
5. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.  
6. All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.  
7. For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V.  
8. For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 µA	V <sub>I</sub> = V <sub>IH</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V				V <sub>CCO</sub> – 0.2 V		V
	I <sub>OH</sub> = –3 mA		1.2 V	1.2 V		0.95				
	I <sub>OH</sub> = –6 mA		1.4 V	1.4 V				1.05		
	I <sub>OH</sub> = –8 mA		1.65 V	1.65 V				1.2		
	I <sub>OH</sub> = –9 mA		2.3 V	2.3 V				1.75		
	I <sub>OH</sub> = –12 mA		3 V	3 V				2.3		
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	V <sub>I</sub> = V <sub>IL</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V				0.2		V
	I <sub>OL</sub> = 3 mA		1.2 V	1.2 V		0.15				
	I <sub>OL</sub> = 6 mA		1.4 V	1.4 V				0.35		
	I <sub>OL</sub> = 8 mA		1.65 V	1.65 V				0.45		
	I <sub>OL</sub> = 9 mA		2.3 V	2.3 V				0.55		
	I <sub>OL</sub> = 12 mA		3 V	3 V				0.7		
I <sub>I</sub>	DIR input	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I <sub>BHL</sub> <sup>†</sup>	V <sub>I</sub> = 0.42 V		1.2 V	1.2 V		25				µA
	V <sub>I</sub> = 0.49 V		1.4 V	1.4 V				15		
	V <sub>I</sub> = 0.58 V		1.65 V	1.65 V				25		
	V <sub>I</sub> = 0.7 V		2.3 V	2.3 V				45		
	V <sub>I</sub> = 0.8 V		3.3 V	3.3 V				100		
I <sub>BHH</sub> <sup>‡</sup>	V <sub>I</sub> = 0.78 V		1.2 V	1.2 V		25				µA
	V <sub>I</sub> = 0.91 V		1.4 V	1.4 V				15		
	V <sub>I</sub> = 1.07 V		1.65 V	1.65 V				25		
	V <sub>I</sub> = 1.6 V		2.3 V	2.3 V				45		
	V <sub>I</sub> = 2 V		3.3 V	3.3 V				100		
I <sub>BHLO</sub> <sup>§</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.2 V	1.2 V		50				µA
			1.6 V	1.6 V				125		
			1.95 V	1.95 V				200		
			2.7 V	2.7 V				300		
			3.6 V	3.6 V				500		
I <sub>BHHO</sub> <sup>¶</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.2 V	1.2 V		50				µA
			1.6 V	1.6 V				125		
			1.95 V	1.95 V				200		
			2.7 V	2.7 V				300		
			3.6 V	3.6 V				500		

<sup>†</sup> The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

<sup>‡</sup> The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

<sup>§</sup> An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

<sup>¶</sup> An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

NOTES: 9. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

10. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10) (continued)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 to 3.6 V		±0.1	±1		±5	μA
	B port		0 to 3.6 V	0 V		±0.1	±1		±5	
I <sub>OZ</sub>	A or B ports	V <sub>O</sub> = V <sub>CCO</sub> or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.5	±2.5		±5	μA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					10	μA
			0 V	3.6 V					–2	
			3.6 V	0 V					10	
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					10	μA
			0 V	3.6 V					10	
			3.6 V	0 V					–2	
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					20	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V		2.5				pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 3.3 V or GND	3.3 V	3.3 V		6				pF

NOTES: 9. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

10. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

switching characteristics over recommended operating free-air temperature range, V<sub>CCA</sub> = 1.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V	V <sub>CCB</sub> = 1.8 V	V <sub>CCB</sub> = 2.5 V	V <sub>CCB</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t <sub>PLH</sub>	A	B	3.3	2.7	2.4	2.3	2.4	ns
t <sub>PHL</sub>			3.3	2.7	2.4	2.3	2.4	
t <sub>PLH</sub>	B	A	3.3	3.1	2.9	2.8	2.7	ns
t <sub>PHL</sub>			3.3	3.1	2.9	2.8	2.7	
t <sub>PHZ</sub>	DIR	A	5.1	5.2	5.3	5.2	3.7	ns
t <sub>PLZ</sub>			5.1	5.2	5.3	5.2	3.7	
t <sub>PHZ</sub>	DIR	B	5.3	4.3	4	3.3	3.7	ns
t <sub>PLZ</sub>			5.3	4.3	4	3.3	3.7	
t <sub>PZH</sub> <sup>†</sup>	DIR	A	8.5	6.9	6.4	5.5	6.1	ns
t <sub>PZL</sub> <sup>†</sup>			8.5	6.9	6.4	5.5	6.1	
t <sub>PZH</sub> <sup>†</sup>	DIR	B	8.3	7.8	7.7	7.5	5.9	ns
t <sub>PZL</sub> <sup>†</sup>			8.3	7.8	7.7	7.5	5.9	

<sup>†</sup> The enable time is a calculated value, derived using the formula shown in the *enable times* section.



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**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (see Figure 11)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	ns
$t_{PHL}$			2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	
$t_{PLH}$	B	A	2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	ns
$t_{PHL}$			2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	
$t_{PHZ}$	DIR	A	3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	ns
$t_{PLZ}$			3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	
$t_{PHZ}$	DIR	B	5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	ns
$t_{PLZ}$			5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	
$t_{PZH}^{\dagger}$	DIR	A	7.7		13.6		12.4		9.6		9.3	ns
$t_{PZL}^{\dagger}$			7.7		13.6		12.4		9.6		9.3	
$t_{PZH}^{\dagger}$	DIR	B	6.7		12.3		12		11.1		10.7	ns
$t_{PZL}^{\dagger}$			6.7		12.3		12		11.1		10.7	

<sup>†</sup> The enable time is a calculated value, derived using the formula shown in the *enable times* section.

**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see Figure 11)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.8	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	ns
$t_{PHL}$			2.8	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	
$t_{PLH}$	B	A	2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	ns
$t_{PHL}$			2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	
$t_{PHZ}$	DIR	A	3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	ns
$t_{PLZ}$			3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	
$t_{PHZ}$	DIR	B	5	1.8	7.7	1.4	6.8	1	4.4	1.4	4.3	ns
$t_{PLZ}$			5	1.89	7.7	1.4	6.8	1	4.4	1.4	4.3	
$t_{PZH}^{\dagger}$	DIR	A	7.3		12.9		11.8		9		8.7	ns
$t_{PZL}^{\dagger}$			7.3		12.9		11.8		9		8.7	
$t_{PZH}^{\dagger}$	DIR	B	6.5		11.2		10.9		9.8		9.4	ns
$t_{PZL}^{\dagger}$			6.5		11.2		10.9		9.8		9.4	

<sup>†</sup> The enable time is a calculated value, derived using the formula shown in the *enable times* section.



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	ns
$t_{PHL}$			2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	
$t_{PLH}$	B	A	2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	ns
$t_{PHL}$			2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	
$t_{PHZ}$	DIR	A	2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	ns
$t_{PLZ}$			2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	
$t_{PHZ}$	DIR	B	4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	ns
$t_{PLZ}$			4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	
$t_{PZH}^{\dagger}$	DIR	A	7.1		11.8		10.3		7.5		7.3	ns
$t_{PZL}^{\dagger}$			7.1		11.8		10.3		7.5		7.3	
$t_{PZH}^{\dagger}$	DIR	B	5.4		8.6		8.1		7		6.6	ns
$t_{PZL}^{\dagger}$			5.4		8.6		8.1		7		6.6	

<sup>†</sup> The enable time is a calculated value, derived using the formula shown in the *enable times* section.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	ns
$t_{PHL}$			2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	
$t_{PLH}$	B	A	2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	ns
$t_{PHL}$			2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	
$t_{PHZ}$	DIR	A	3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	ns
$t_{PLZ}$			3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	
$t_{PHZ}$	DIR	B	4	0.7	7.4	0.6	6.5	0.7	4	1.5	3.9	ns
$t_{PLZ}$			4	0.7	7.4	0.6	6.5	0.7	4	1.5	3.9	
$t_{PZH}^{\dagger}$	DIR	A	6.2		11.2		9.9		7		6.7	ns
$t_{PZL}^{\dagger}$			6.2		11.2		9.9		7		6.7	
$t_{PZH}^{\dagger}$	DIR	B	5.7		8.9		8.5		7.2		6.8	ns
$t_{PZL}^{\dagger}$			5.7		8.9		8.5		7.2		6.8	

<sup>†</sup> The enable time is a calculated value, derived using the formula shown in the *enable times* section.



**SN74AVCH1T45**

**SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2\text{ V}$	$V_{CCA} = V_{CCB} = 1.5\text{ V}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	$V_{CCA} = V_{CCB} = 2.5\text{ V}$	$V_{CCA} = V_{CCB} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^\dagger$	A-port input, B-port output	$C_L = 0\text{ pF}$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	3	3	3	3	4	pF
	B-port input, A-port output		14	14	14	15	16	
$C_{pdB}^\dagger$	A-port input, B-port output	$C_L = 0\text{ pF}$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	14	14	14	15	16	pF
	B-port input, A-port output		3	3	3	3	4	

$^\dagger$  Power-dissipation capacitance per transceiver

# SN74AVCH1T45

## SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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#### power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up  $V_{CCA}$ .
3.  $V_{CCB}$  can be ramped up along with or after  $V_{CCA}$ .

#### typical total static power consumption ( $I_{CCA} + I_{CCB}$ )

Table 1

$V_{CCB}$	$V_{CCA}$						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	$\mu A$
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

**SN74AVCH1T45**  
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**TYPICAL CHARACTERISTICS**

**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.2\text{ V}$

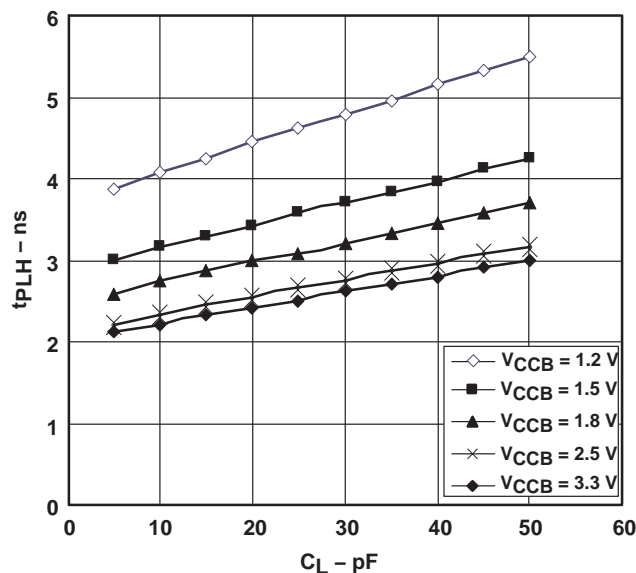


Figure 1

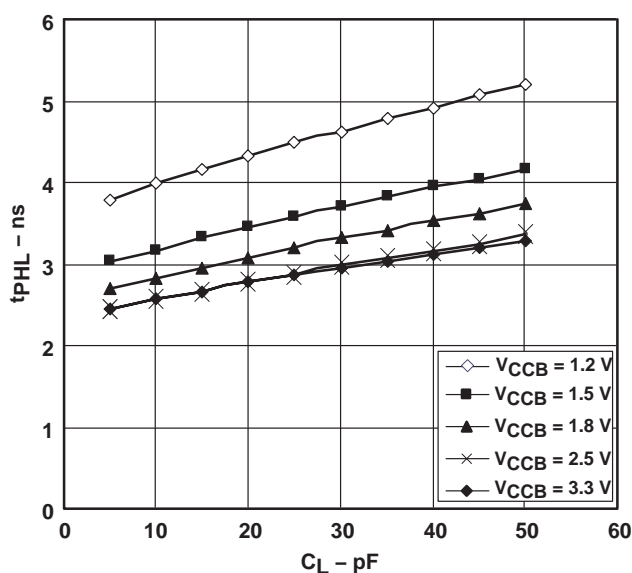


Figure 2

**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.5\text{ V}$

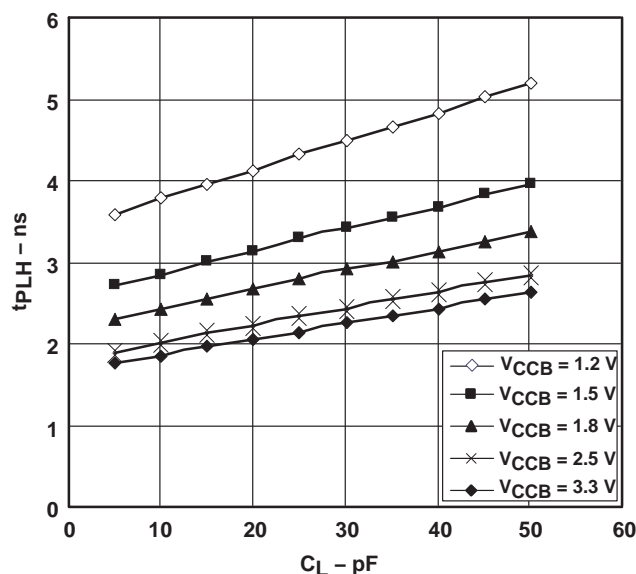


Figure 3

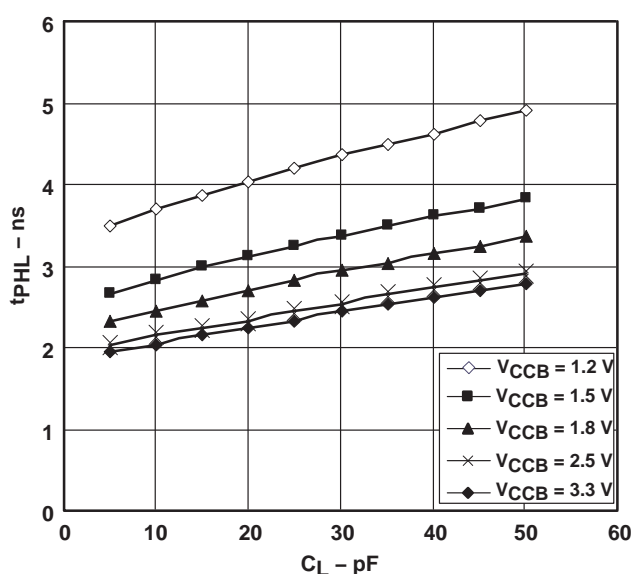


Figure 4

# SN74AVCH1T45

## SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.8\text{ V}$

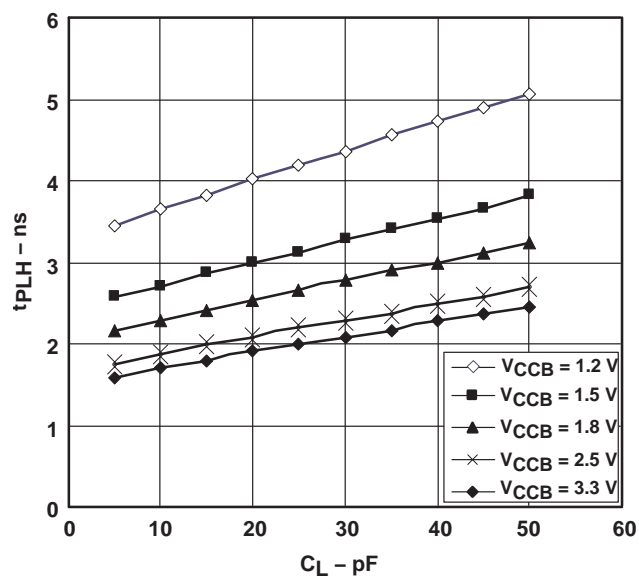


Figure 5

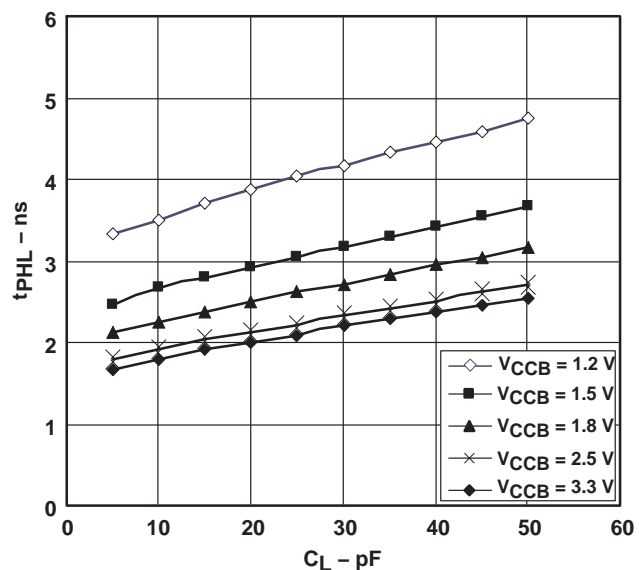


Figure 6

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 2.5\text{ V}$

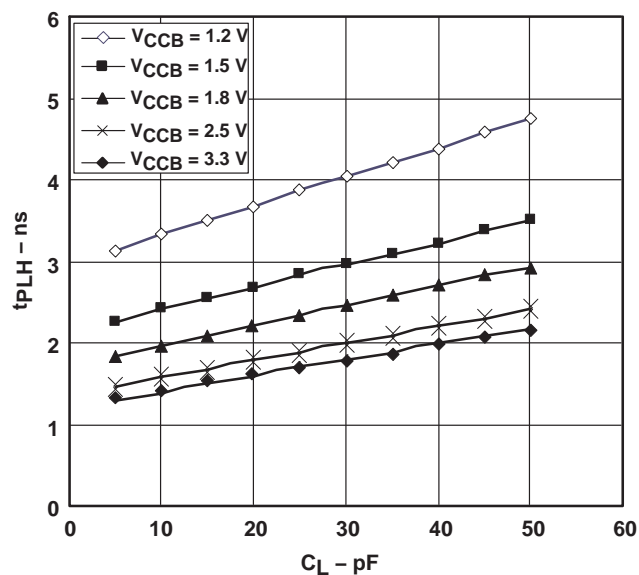


Figure 7

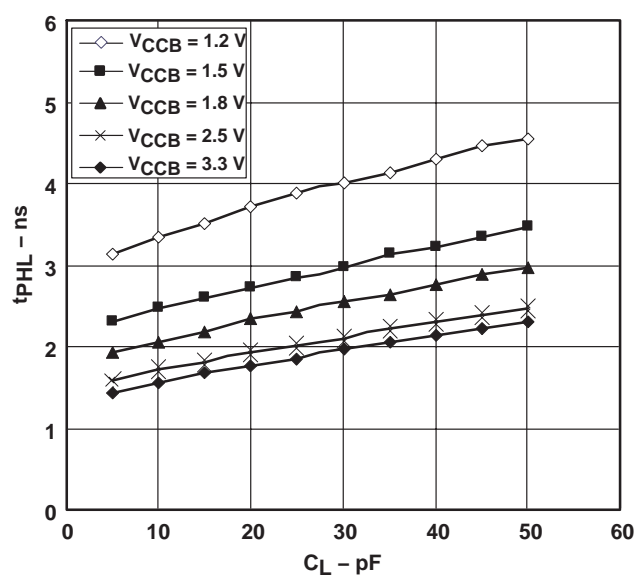


Figure 8

**SN74AVCH1T45**  
**SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**  
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**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V}$

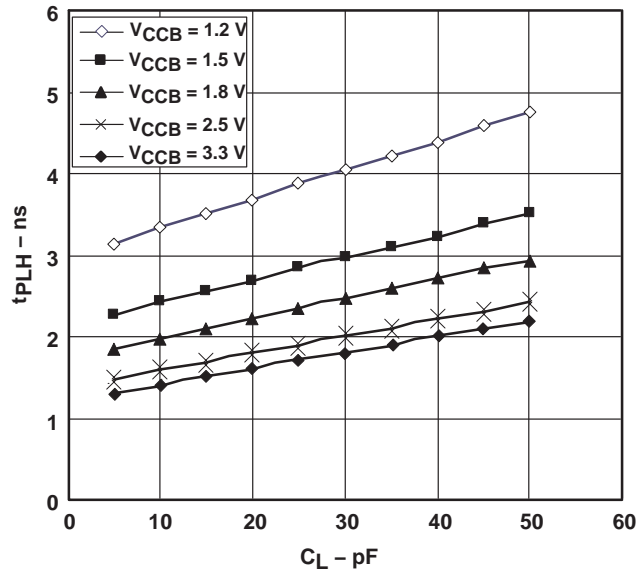


Figure 9

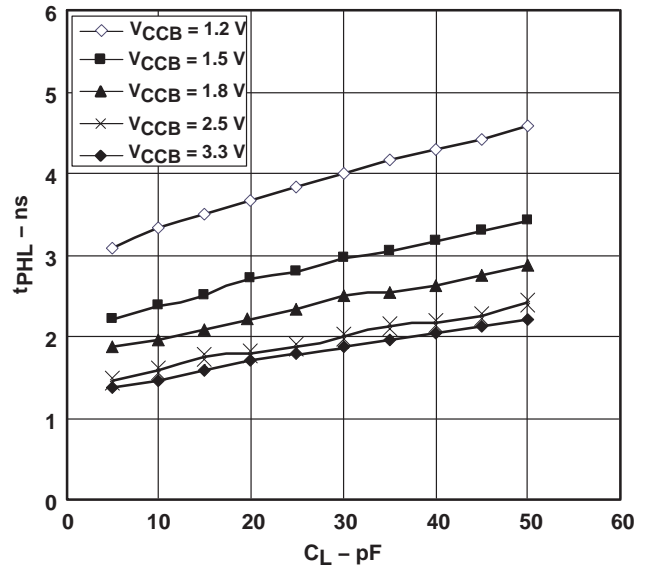


Figure 10

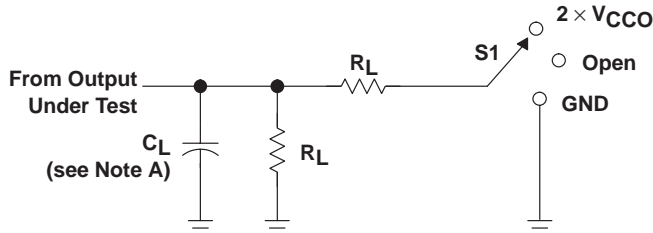
# SN74AVCH1T45

## SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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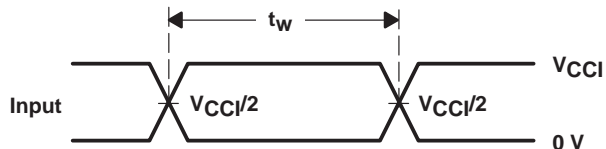
#### PARAMETER MEASUREMENT INFORMATION



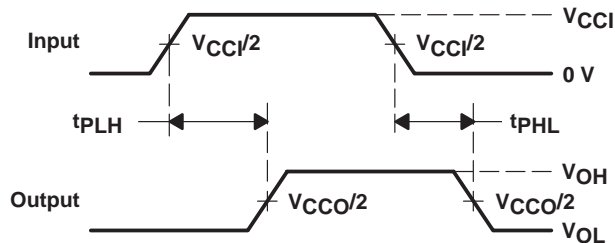
LOAD CIRCUIT

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V

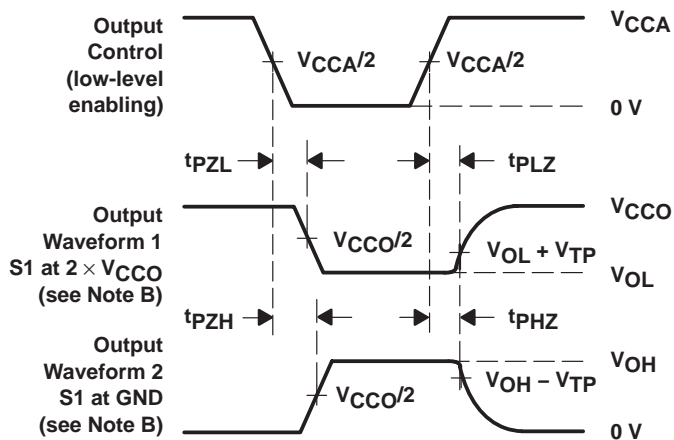
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



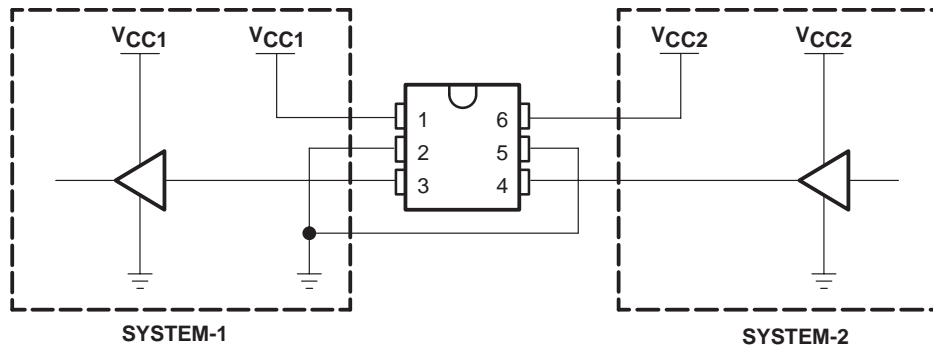
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1 \text{ V/ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

## APPLICATION INFORMATION

Figure 12 shows an example of the SN74AVCH1T45 being used in a unidirectional logic level-shifting application.

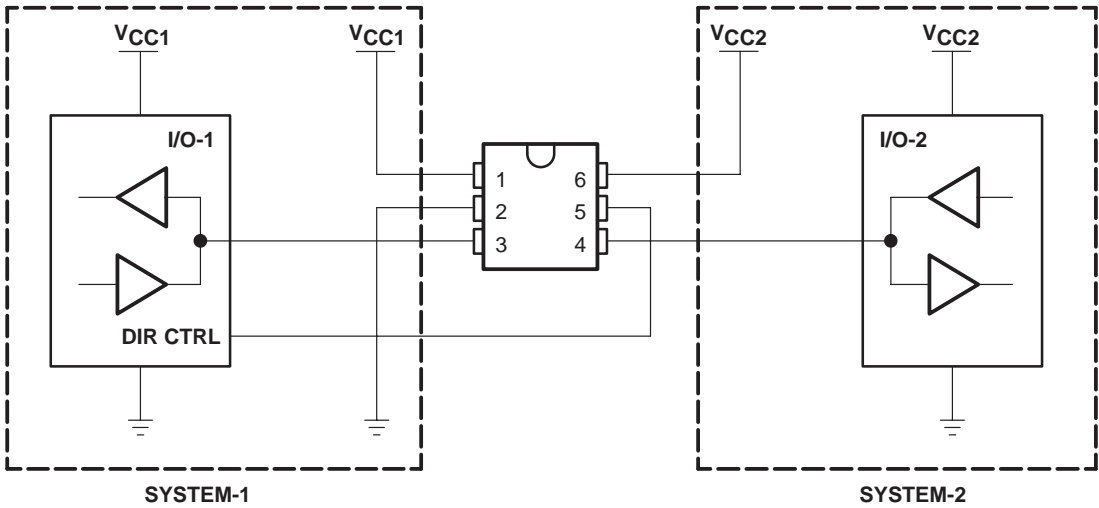


PIN	NAME	FUNCTION	DESCRIPTION
1	V <sub>CCA</sub>	V <sub>CC1</sub>	SYSTEM-1 supply voltage (1.2 V to 3.6 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V <sub>CC1</sub> voltage.
4	B	IN	Input threshold value depends on V <sub>CC2</sub> voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V <sub>CCB</sub>	V <sub>CC2</sub>	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

**Figure 12. Unidirectional Logic Level-Shifting Application**

APPLICATION INFORMATION

Figure 13 shows the SN74AVCH1T45 being used in a bidirectional logic level-shifting application. Since the SN74AVCH1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



Following is a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 are still disabled. The bus-line state depends on bus hold.
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

Figure 13. Bidirectional Logic Level-Shifting Application

enable times

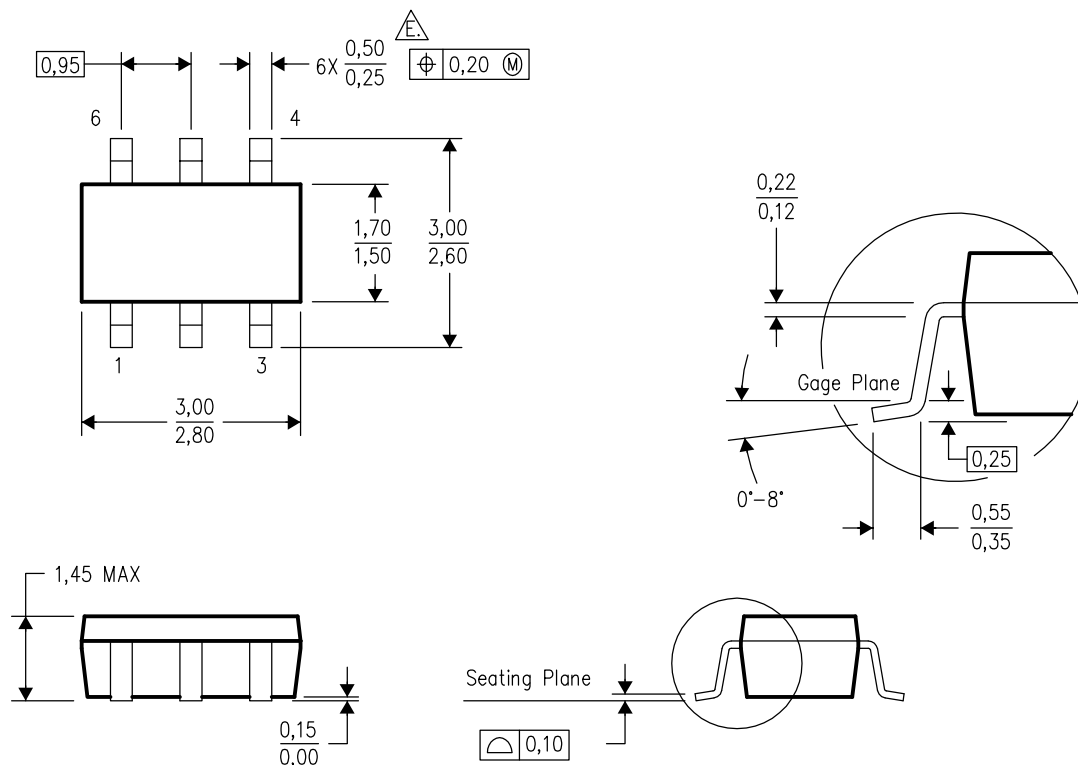
Calculate the enable times for the SN74AVCH1T45 using the following formulas:

$$\begin{aligned}
t_{PZH} \text{ (DIR to A)} &= t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \\
t_{PZL} \text{ (DIR to A)} &= t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \\
t_{PZH} \text{ (DIR to B)} &= t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \\
t_{PZL} \text{ (DIR to B)} &= t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}
\end{aligned}$$


In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVCH1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

## DBV (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE

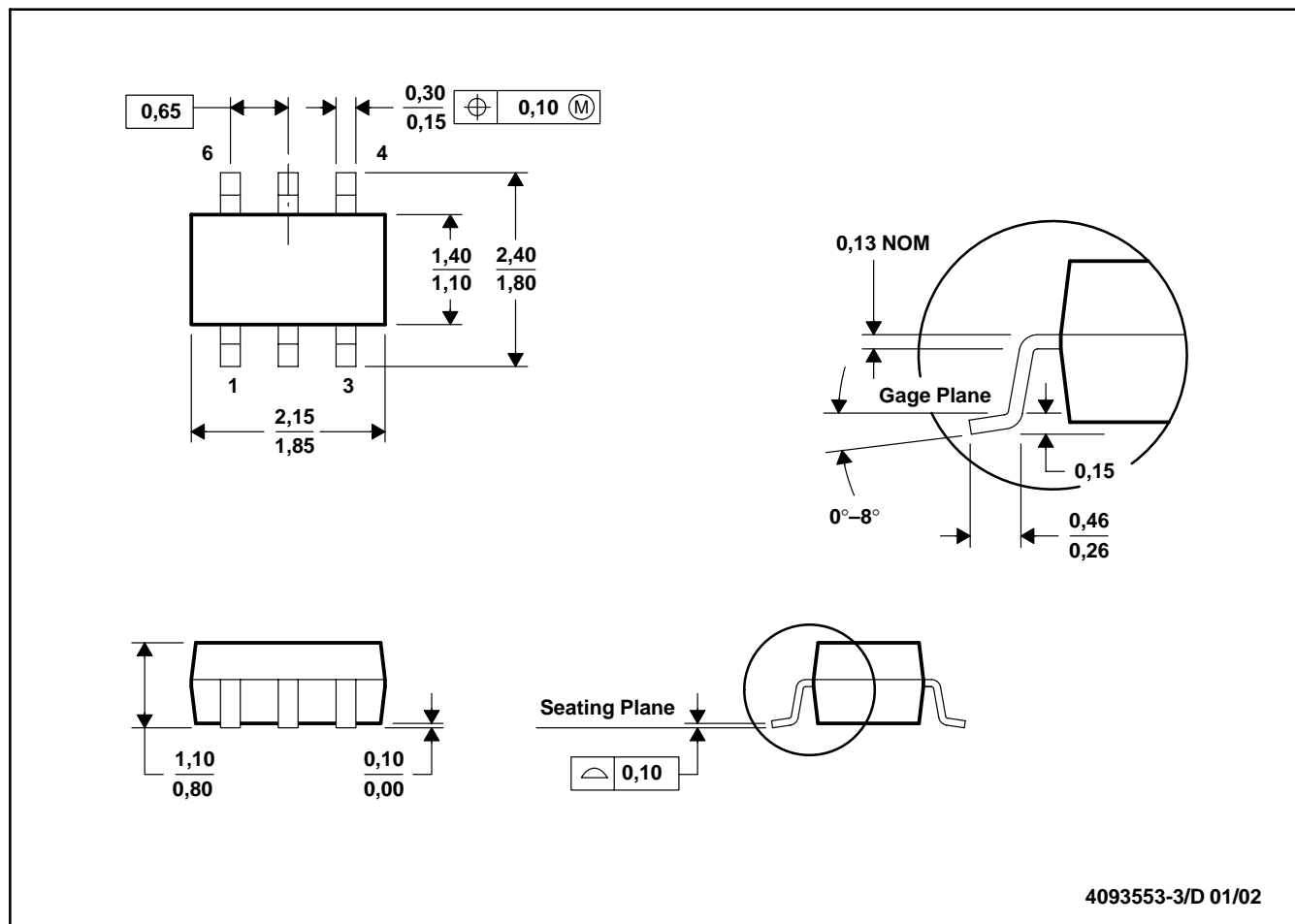


4073253-5/H 10/2003

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  -  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

## DCK (R-PDSO-G6)

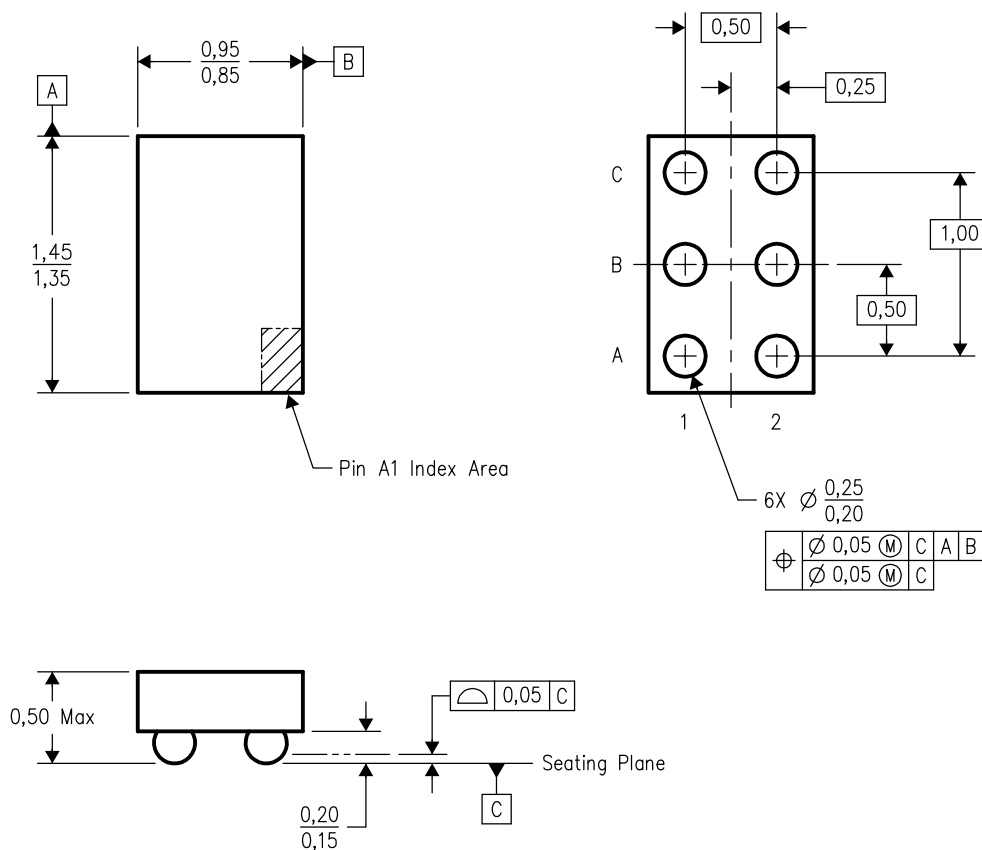
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-203

## YZP (R-XBGA-N6)

## DIE-SIZE BALL GRID ARRAY



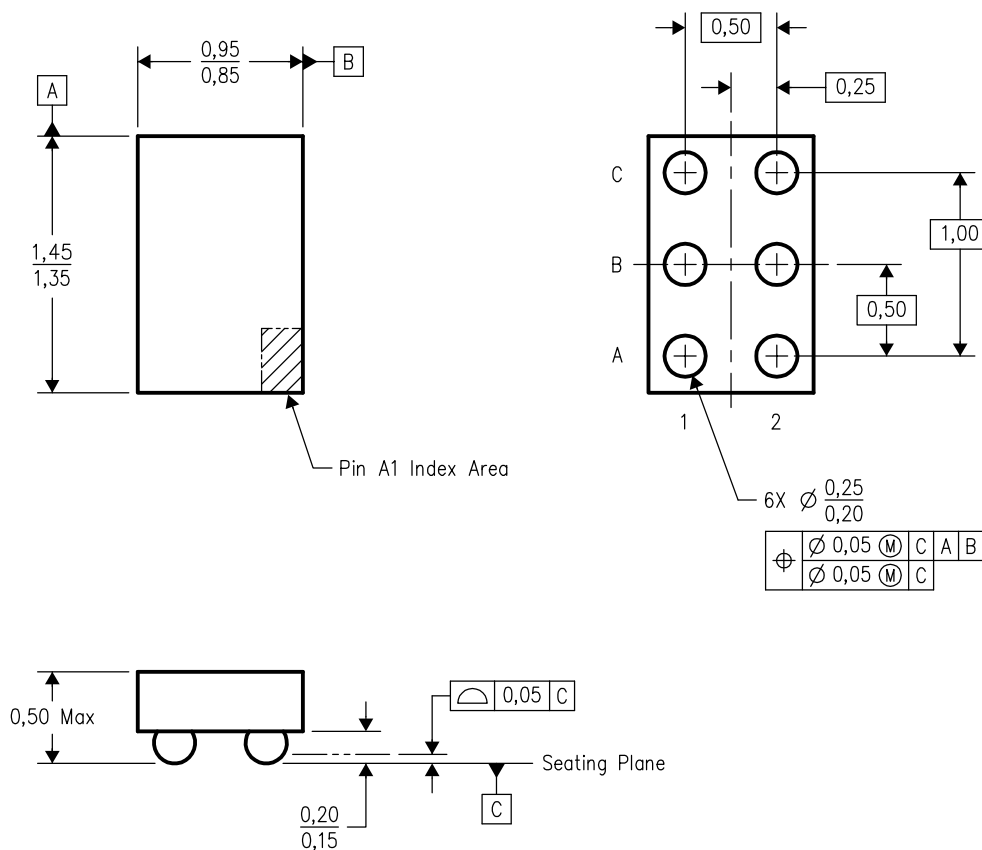
4204741-3/A 10/2002

- NOTES:
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  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4204725-3/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. This package is tin-lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead-free.

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