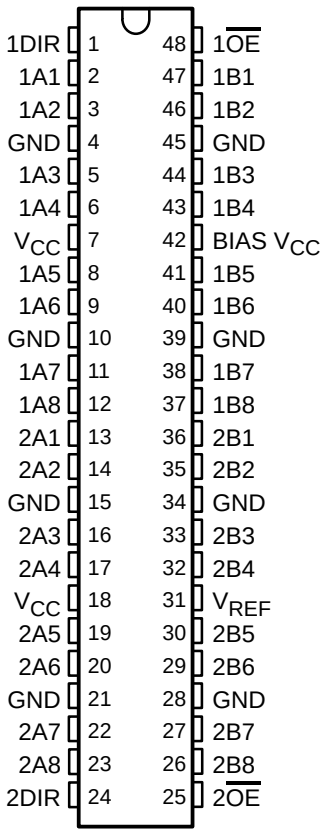
- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLPH16945 is a medium-drive, 16-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as two 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16945 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

description (continued)

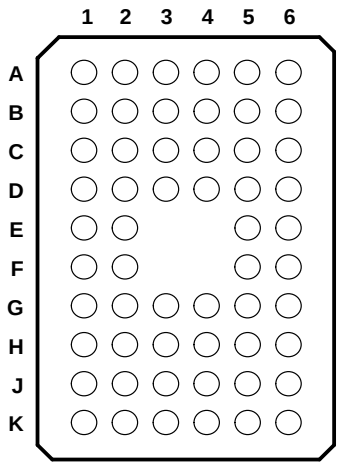
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1A2	1A1	GND	GND	1B1	1B2
C	1A4	1A3	V_{CC}	BIAS V_{CC}	1B3	1B4
D	1A6	1A5	GND	GND	1B5	1B6
E	2A8	1A7			1B7	1B8
F	2A1	2A2			2B2	2B1
G	2A3	2A4	GND	GND	2B4	2B3
H	2A5	2A6	V_{CC}	V_{REF}	2B6	2B5
J	2A7	2A8	GND	GND	2B8	2B7
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH16945GR	GTLPH16945
	TVSOP – DGV	Tape and reel	SN74GTLPH16945VR	GL945
	VFBGA – GQL	Tape and reel	SN74GTLPH16945KR	GL945

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH16945 is a medium-drive (50 mA), 16-bit bus transceiver partitioned as two 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

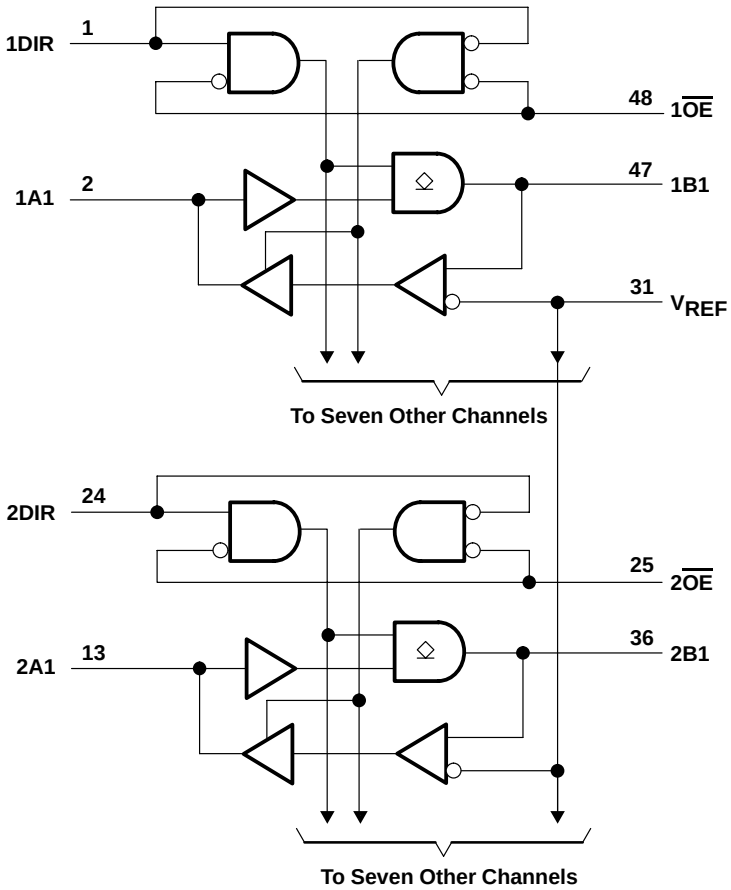
For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{OE}$ and DIR are low.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port and control inputs . . . . . –0.5 V to 7 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 100 mA
Current into any A port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
GQL package . . . . . 42°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			μs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}‡	A port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4.5	5	pF
C_{io}	A port	V_O = 3.15 V or 0			7.5	9	pF
	B port	V_O = 1.5 V or 0			7.5	9	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

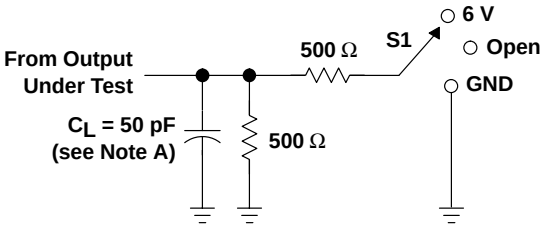
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	μA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		μA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

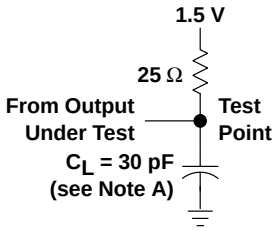
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	B	2.1		6.3	ns
t_{PHL}			2.1		6.3	
t_{en}	$\overline{OE}$	B	2		6.9	ns
t_{dis}			2		6.9	
t_r	Rise time, B outputs (20% to 80%)			2.5		ns
t_f	Fall time, B outputs (80% to 20%)			2.1		ns
t_{PLH}	B	A	2.1		5.3	ns
t_{PHL}			2.1		5.3	
t_{en}	$\overline{OE}$	A	0.3		5.7	ns
t_{dis}			0.3		5.7	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

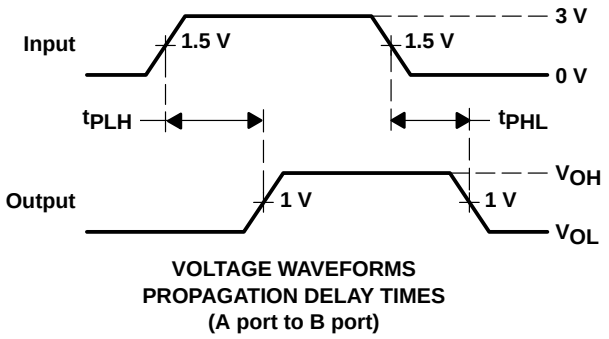


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

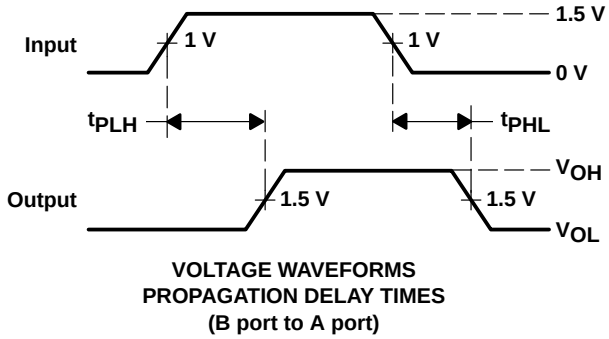


LOAD CIRCUIT FOR A OUTPUTS

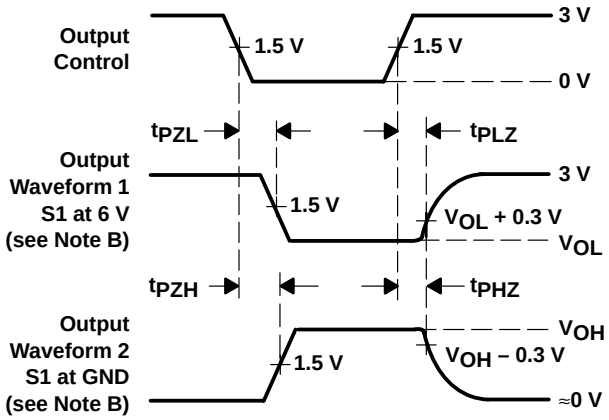
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

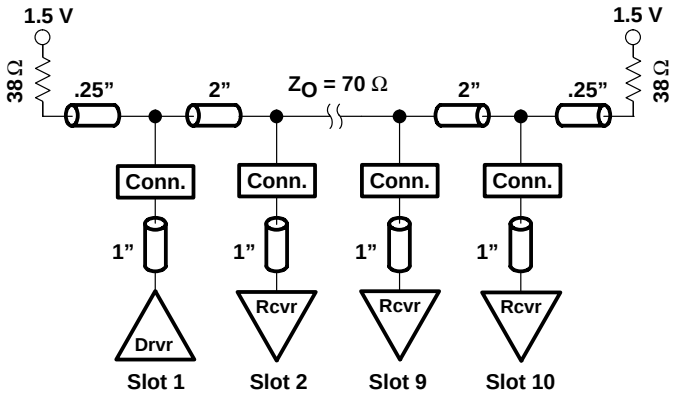


Figure 2. Medium-Drive Test Backplane

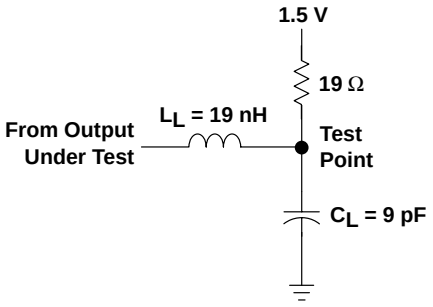


Figure 3. Medium-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	4.3	ns
t_{PHL}			4.3	
t_{en}	$\overline{OE}$	B	5	ns
t_{dis}			4.4	
t_r	Rise time, B outputs (20% to 80%)		1	ns
t_f	Fall time, B outputs (80% to 20%)		2	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

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