- **2-V to 5.5-V V_{CC} Operation**
- **Typical V_{OLP} (Output Ground Bounce)**
  <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
  >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- **Support Mixed-Mode Voltage Operation on All Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV05A . . . J OR W PACKAGE
SN74LV05A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

SN54LV05A . . . FK PACKAGE
(TOP VIEW)

Top pins: 1Y, 1A, NC, V_{CC}, 6A (pins 3 2 1 20 19)

2A	4	18	6Y
NC	5	17	NC
2Y	6	16	5A
NC	7	15	NC
3A	8	14	5Y

Bottom pins: 3Y, GND, NC, 4Y, 4A (pins 9 10 11 12 13)

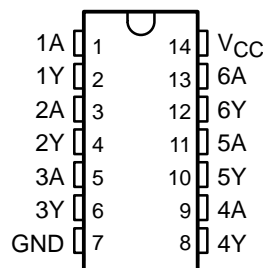NC – No internal connection

description/ordering information

The 'LV05A devices contain six independent inverters designed for 2-V to 5.5-V V_{CC} operation.

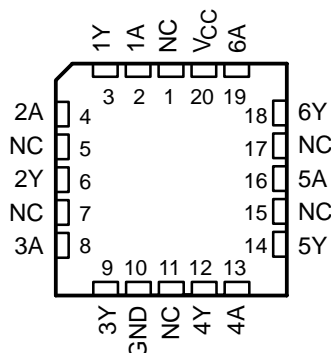These devices perform the Boolean function $Y = \overline{A}$.

The open-drain outputs require pullup resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – D	Tube of 50	SN74LV05AD	LV05A
		Reel of 2500	SN74LV05ADR	
	SOP – NS	Reel of 2000	SN74LV05ANSR	74LV05A
	SSOP – DB	Reel of 2000	SN74LV05ADBR	LV05A
	TSSOP – PW	Tube of 90	SN74LV05APW	LV05A
		Reel of 2000	SN74LV05APWR	
		Reel of 250	SN74LV05APWT	
	TVSOP – DGV	Reel of 2000	SN74LV05ADGVR	LV05A
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV05AJ	SNJ54LV05AJ
	CFP – W	Tube of 150	SNJ54LV05AW	SNJ54LV05AW
	LCCC – FK	Tube of 55	SNJ54LV05AFK	SNJ54LV05AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

SN54LV05A, SN74LV05A
HEX INVERTERS
WITH OPEN-DRAIN OUTPUTS

SCLS391G – APRIL 1998 – REVISED JULY 2003

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)
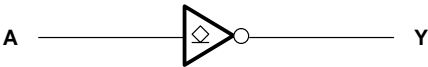
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V

Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V

Voltage range applied to any output in the high-impedance
  or power-off state, V_O (see Note 1) .... –0.5 V to 7 V

Output voltage range, V_O (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) .... –20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA

Continuous current through V_{CC} or GND .... ±50 mA

Package thermal impedance, θ_{JA} (see Note 3): D package .... 86°C/W

               DB package .... 96°C/W

               DGV package .... 127°C/W

               NS package .... 76°C/W

               PW package .... 113°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1.   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
      2.   This value is limited to 5.5 V maximum.
      3.   The package thermal impedance is calculated in accordance with JESD 51-7.

TEXAS INSTRUMENTS

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recommended operating conditions (see Note 4)

			SN54LV05A		SN74LV05A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	5.5	0	5.5	V
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 2.3$ V to 2.7 V		2		2	mA
		$V_{CC} = 3$ V to 3.6 V		6		6	
		$V_{CC} = 4.5$ V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200		200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100		100	
		$V_{CC} = 4.5$ V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV05A			SN74LV05A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	$I_{OL} = 50$ µA	2 V to 5.5 V			0.1			0.1	V
	$I_{OL} = 2$ mA	2.3 V			0.4			0.4	
	$I_{OL} = 6$ mA	3 V			0.44			0.44	
	$I_{OL} = 12$ mA	4.5 V			0.55			0.55	
I_I	$V_I = 5.5$ V or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	µA
I_{off}	V_I or $V_O = 0$ to 5.5 V	0			5			5	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.5			2.5		pF

TEXAS INSTRUMENTS

SN54LV05A, SN74LV05A
HEX INVERTERS
WITH OPEN-DRAIN OUTPUTS

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV05A		SN74LV05A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.6*	10.4*	1*	13*	1	13	ns
t_{PHL}					5.8*	12.2*	1*	15*	1	15	
t_{PLH}	A	Y	C_L = 50 pF		6.1	15.2	1	18	1	18	ns
t_{PHL}					8.1	16.6	1	19.5	1	19.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV05A		SN74LV05A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		2.9*	7.1*	1*	8.5*	1	8.5	ns
t_{PHL}					4*	7.1*	1*	8.5*	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		4.7	10.6	1	12	1	12	ns
t_{PHL}					5.8	10.6	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV05A		SN74LV05A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		2.2*	5.5*	1*	6.5*	1	6.5	ns
t_{PHL}					2.9*	5.5*	1*	6.5*	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		3.4	7.5	1	8.5	1	8.5	ns
t_{PHL}					4.2	7.5	1	8.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74LV05A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.55	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.04	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.12		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	2.5	pF
			5 V	3	

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PARAMETER MEASUREMENT INFORMATION
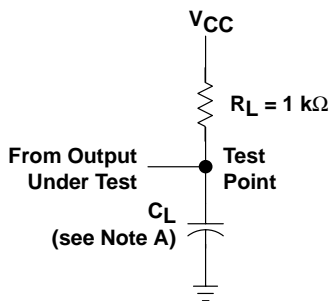
LOAD CIRCUIT FOR
OPEN-DRAIN OUTPUTS
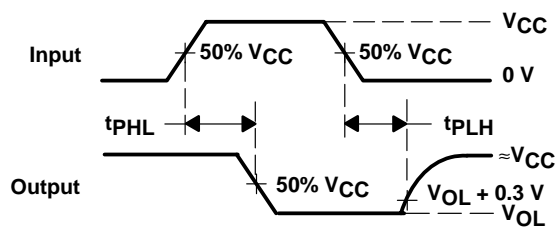
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

$\dfrac{0,23}{0,13}$ ⊕   0,07 Ⓜ

24   13

$\dfrac{4,50}{4,30}$ $\dfrac{6,60}{6,20}$

1   12

A

0,16 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

△ 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
   D. Falls within JEDEC: 24/48 Pins – MO-153
                     14/16/20/56 Pins – MO-194

D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14

8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F   07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

PW (R-PDSO-G**)　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:　A.　All linear dimensions are in millimeters.
　　　　B.　This drawing is subject to change without notice.
　　　　C.　Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　D.　Falls within JEDEC MO-153

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