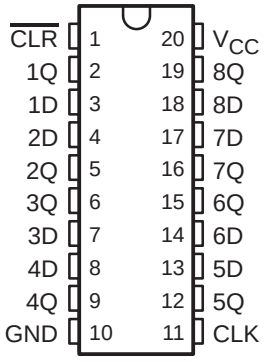
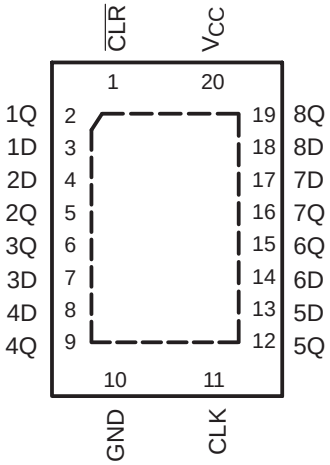
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 10.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

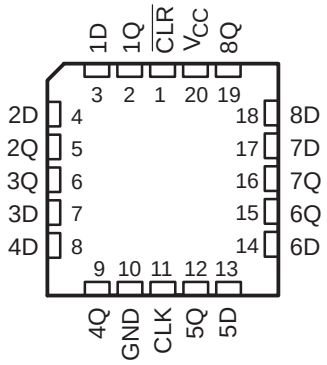
SN54LV273A . . . J OR W PACKAGE
SN74LV273A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV273A . . . RGY PACKAGE
(TOP VIEW)



SN54LV273A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The ’LV273A devices are octal D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV273ARGYR	LV273A
	SOIC – DW	Tube of 25	SN74LV273ADW	LV273A
		Reel of 2000	SN74LV273ADWR	LV273A
	SOP – NS	Reel of 2000	SN74LV273ANSR	74LV273A
	SSOP – DB	Reel of 2000	SN74LV273ADBR	LV273A
	TSSOP – PW	Tube of 70	SN74LV273APW	LV273A
		Reel of 2000	SN74LV273APWR	
		Reel of 250	SN74LV273APWT	
	TVSOP – DGV	Reel of 2000	SN74LV273ADGVR	LV273A
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV273AJ	SNJ54LV273AJ
	CFP – W	Tube of 85	SNJ54LV273AW	SNJ54LV273AW
	LCCC – FK	Tube of 55	SNJ54LV273AFK	SNJ54LV273AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information (continued)

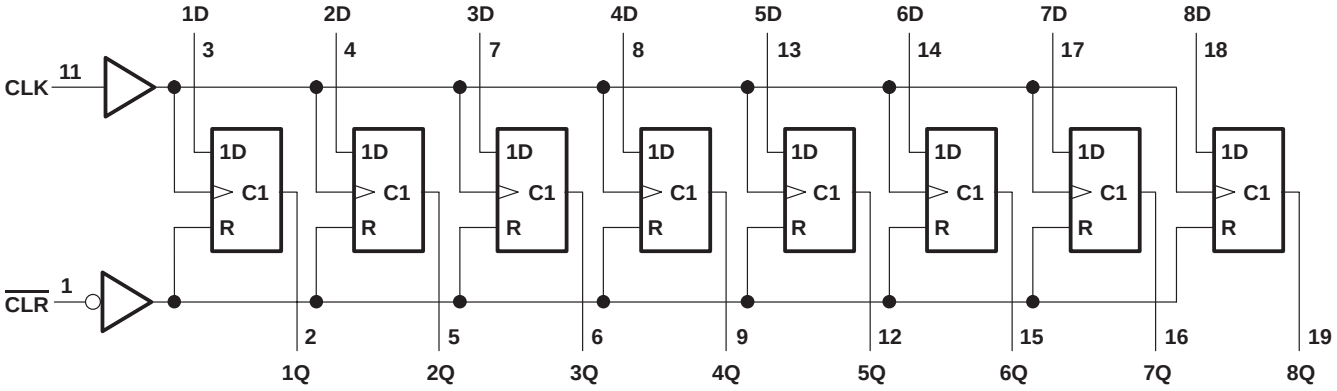
These devices are positive-edge-triggered flip-flops with direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	–20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DW package	58°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV273A		SN74LV273A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV273A			SN74LV273A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –6 mA	3 V	2.48			2.48			
	I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2			2		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV273A		SN74LV273A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	6.5		7		7		ns
		CLK high or low	7		8.5		8.5		
t_{su}	Setup time, data before CLK↑	Data	8.5		10.5		10.5		ns
		$\overline{CLR}$ inactive	4		4		4		
t_h	Hold time, data after CLK↑		0.5		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV273A		SN74LV273A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		6		6		ns
		CLK high or low	5		6.5		6.5		
t_{su}	Setup time, data before CLK↑	Data	5.5		6.5		6.5		ns
		$\overline{CLR}$ inactive	2.5		2.5		2.5		
t_h	Hold time, data after CLK↑		1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV273A		SN74LV273A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time, data before CLK↑	Data	4.5		4.5		4.5		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, data after CLK↑		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV273A		SN74LV273A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	55*	95*		45*		45		MHz
			C_L = 50 pF	45	75		40		40		
t_{pd}	CLK	Q	C_L = 15 pF		10.4*	18.3*	1*	20.5*	1	20.5	ns
t_{PHL}	$\overline{CLR}$	Q			10.3*	19*	1*	21*	1	21	
t_{pd}	CLK	Q	C_L = 50 pF		12.9	22.1	1	25	1	25	ns
t_{PHL}	$\overline{CLR}$	Q			13.1	22.8	1	25.5	1	25.5	
$t_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV273A		SN74LV273A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75*	140*		65*		65		MHz
			C_L = 50 pF	50	110		45		45		
t_{pd}	CLK	Q	C_L = 15 pF		7.1*	13.6*	1*	16*	1	16	ns
t_{PHL}	$\overline{CLR}$	Q			6.9*	13.6*	1*	16*	1	16	
t_{pd}	CLK	Q	C_L = 50 pF		9.1	17.1	1	19.5	1	19.5	ns
t_{PHL}	$\overline{CLR}$	Q			8.7	17.1	1	19.5	1	19.5	
$t_{sk(o)}$						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV273A		SN74LV273A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	120*	205*		100*		100		MHz
			C_L = 50 pF	80	160		70		70		
t_{pd}	CLK	Q	C_L = 15 pF		4.8*	9*	1*	10.5*	1	10.5	ns
t_{PHL}	$\overline{CLR}$	Q			4.7*	8.5*	1*	10*	1	10	
t_{pd}	CLK	Q	C_L = 50 pF		6.2	11	1	12.5	1	12.5	ns
t_{PHL}	$\overline{CLR}$	Q			6	10.5	1	12	1	12	
$t_{sk(o)}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

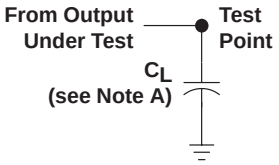
PARAMETER		SN74LV273A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

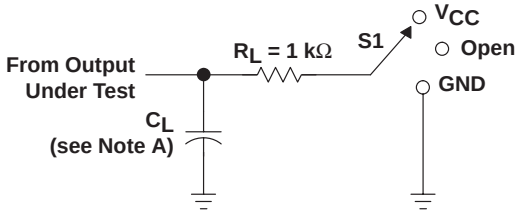
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	15.9	pF
			5 V	17.1	

PARAMETER MEASUREMENT INFORMATION

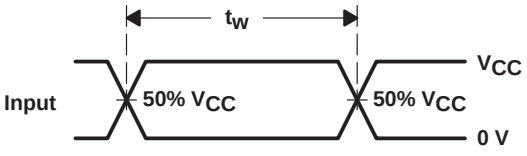


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

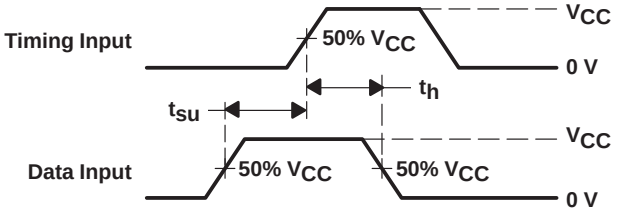


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

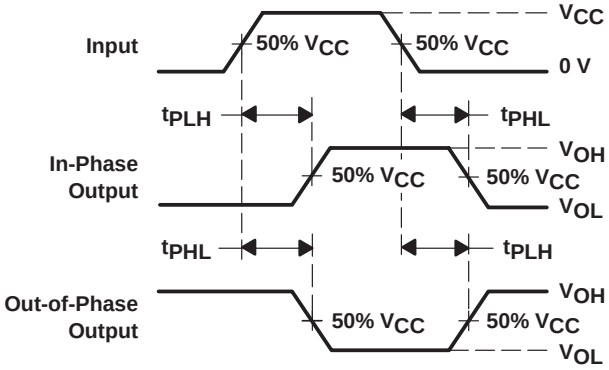
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



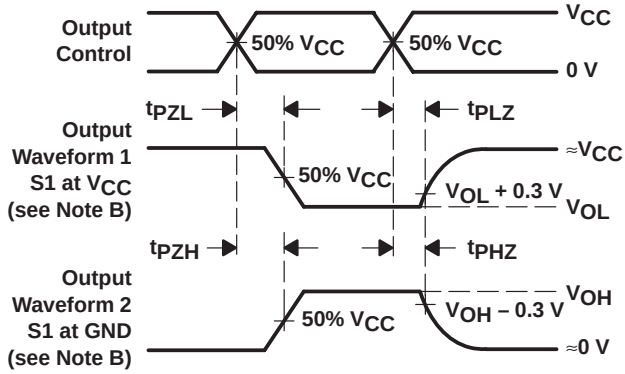
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



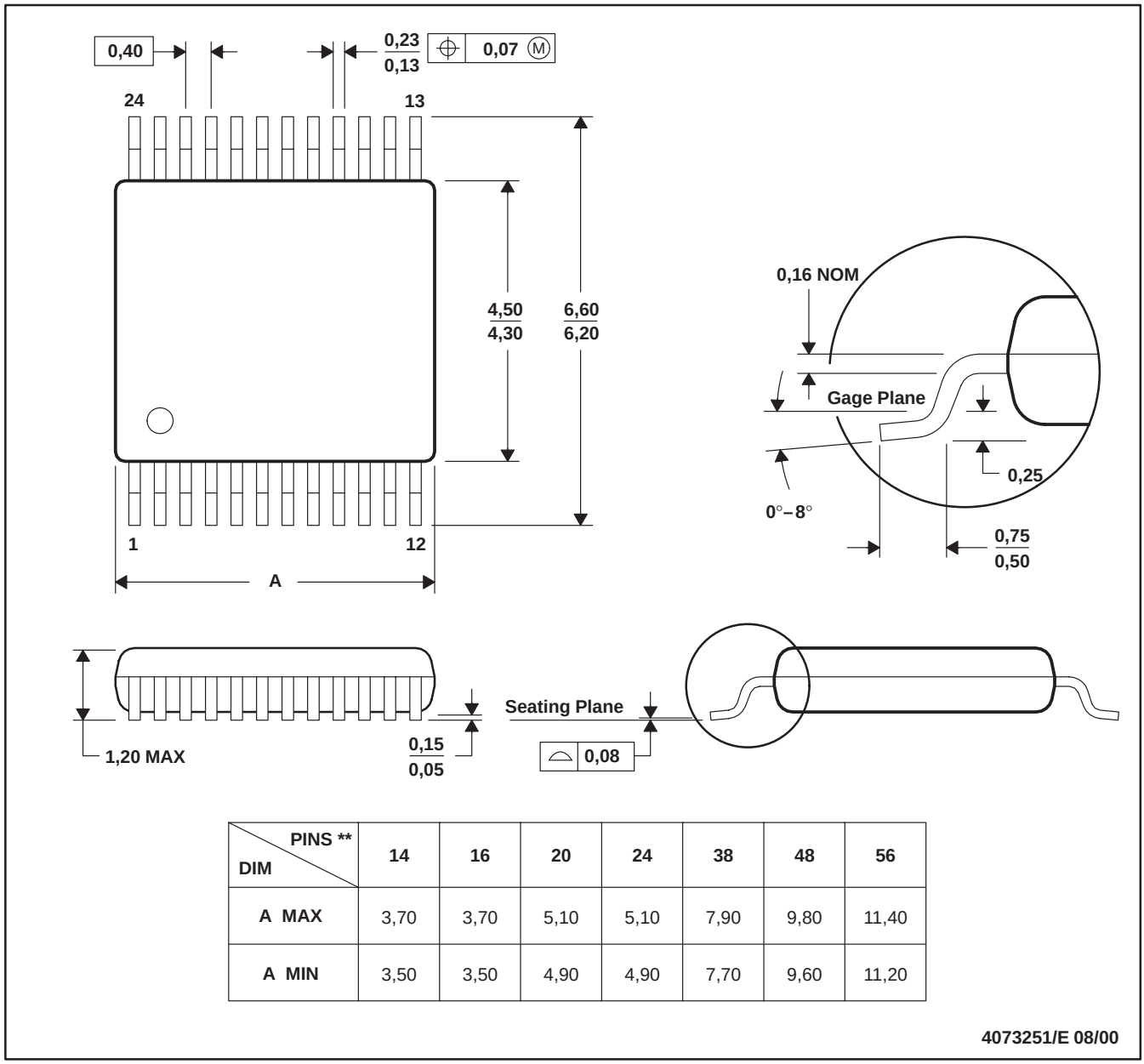
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

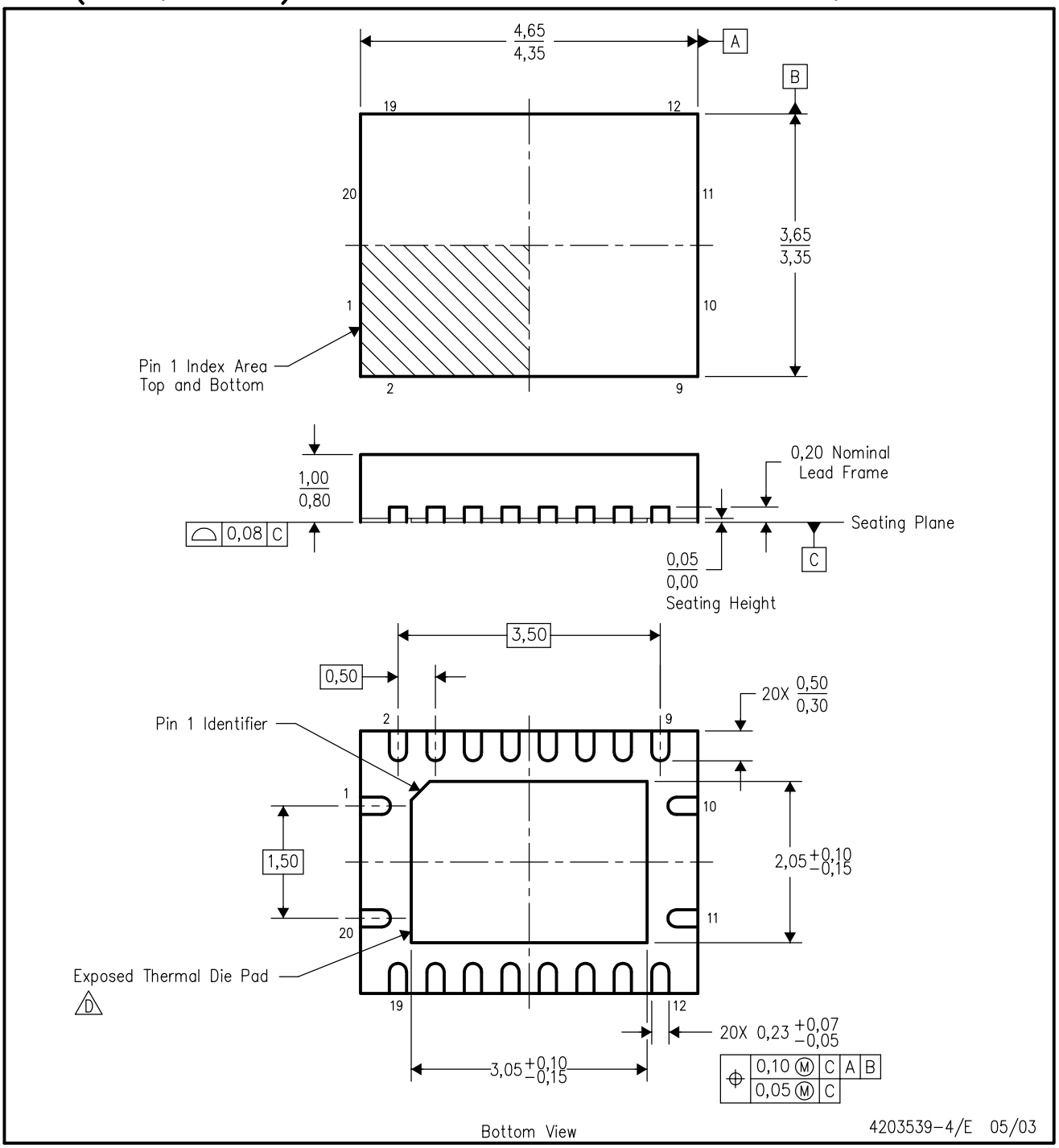


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
E. Package complies to JEDEC MO–241 variation BC.

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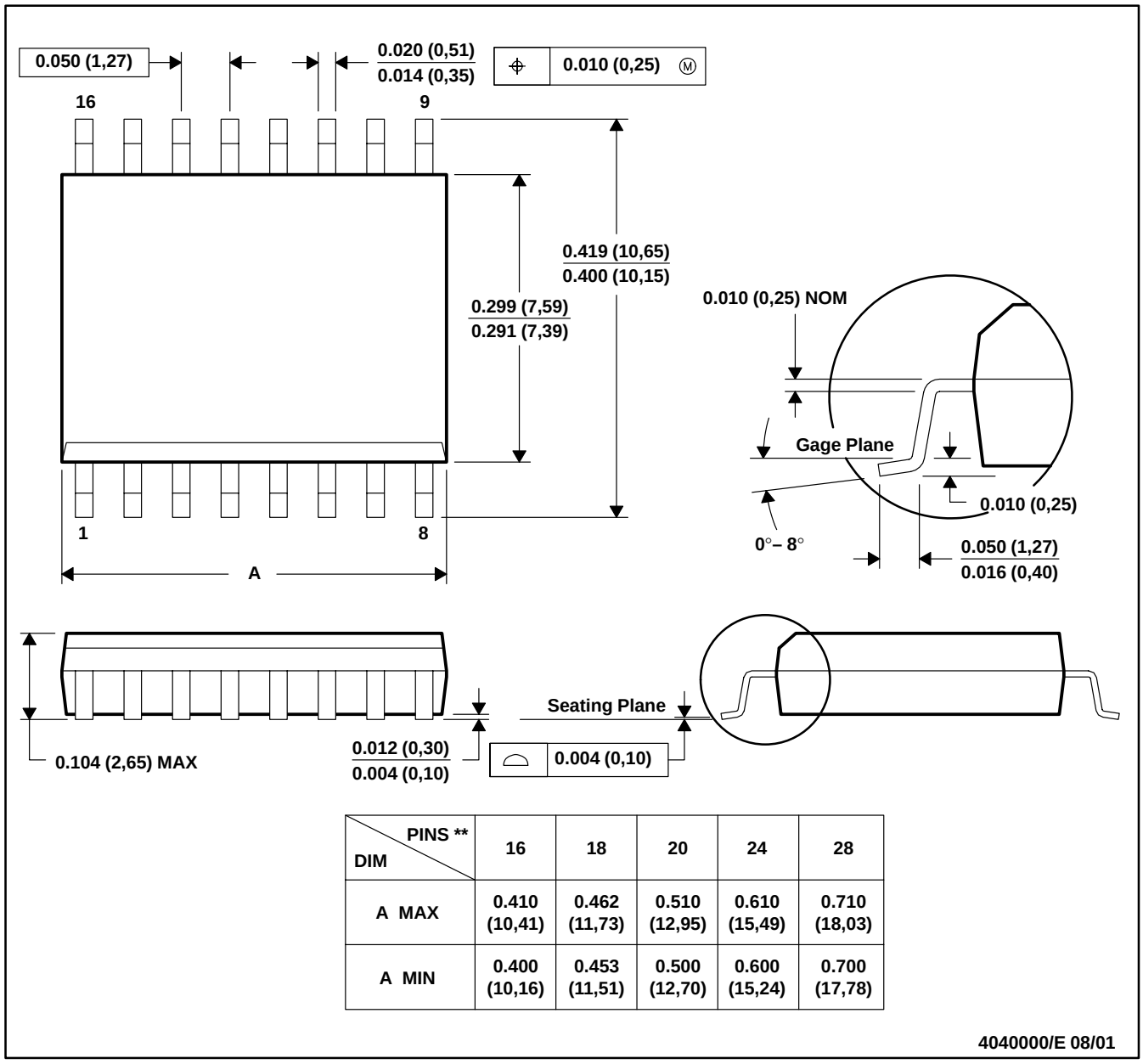
DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

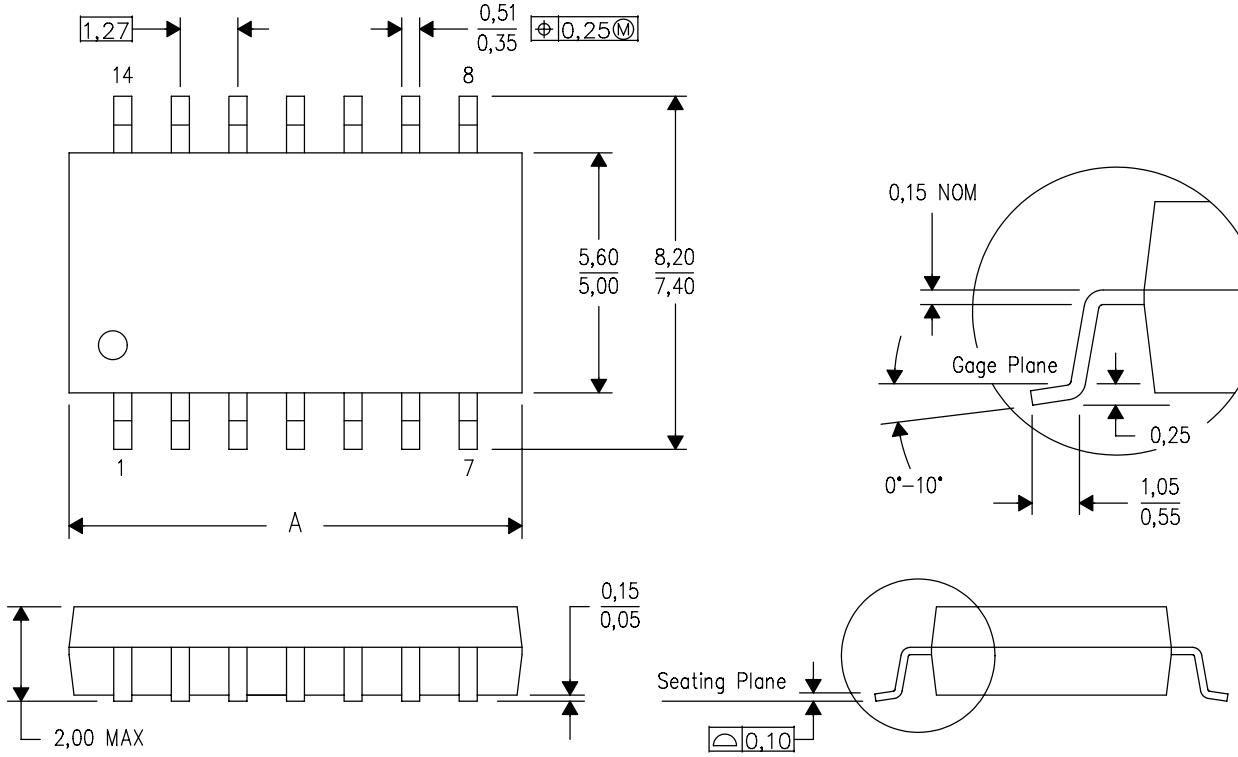
4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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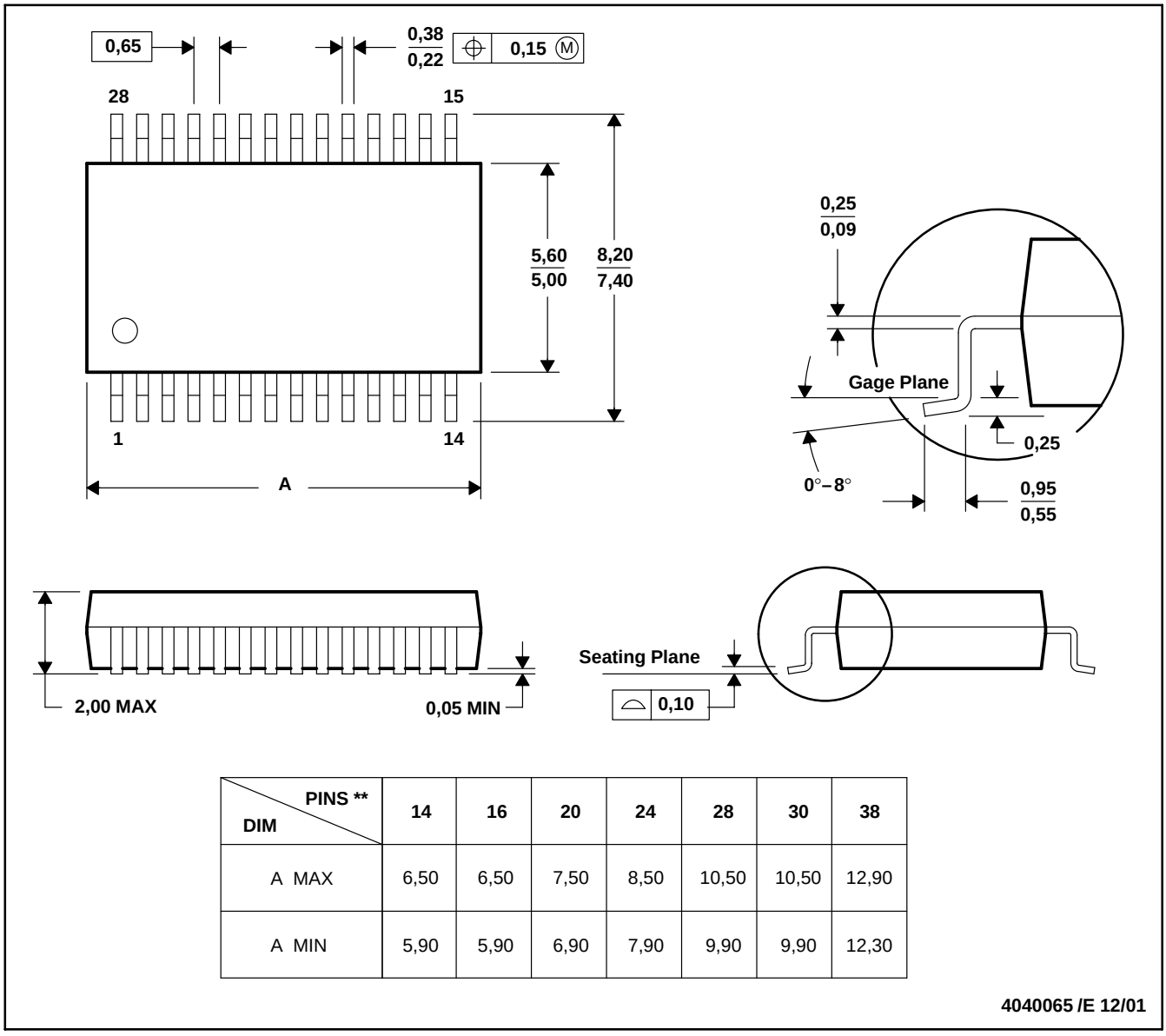
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



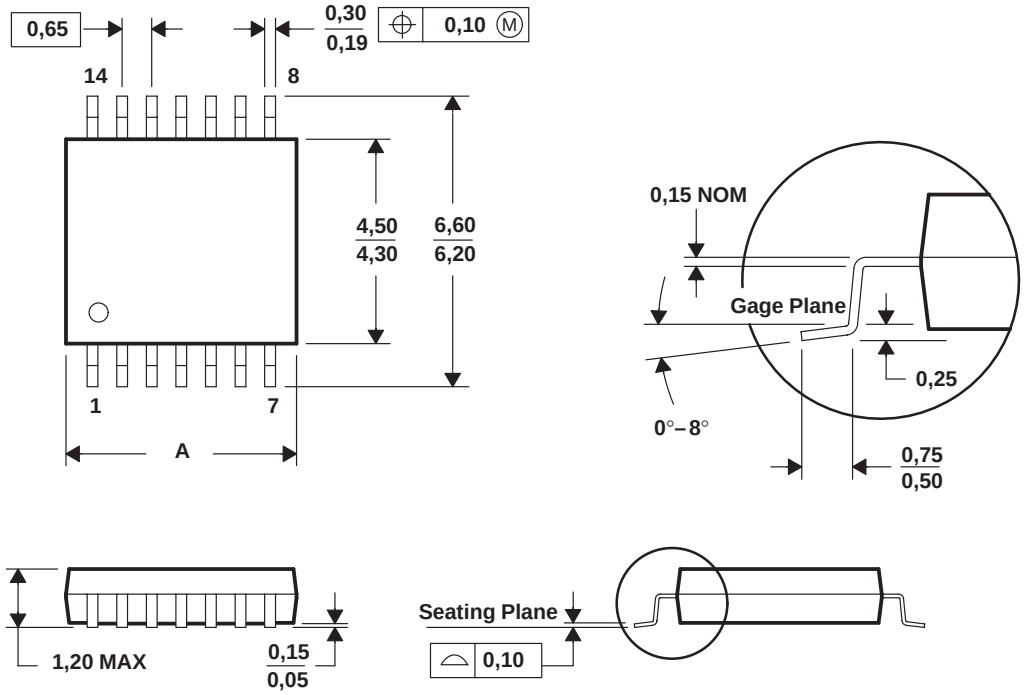
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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